Design of radiation tolerant readout system for integrated SRAM-based neutron detector

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ABSTRACT

This paper presents a design of a radiation tolerant readout system for a Static Random Access Memory (SRAM)-based neutron detector. The radiation tolerance has been achieved on the system level by applying Error Detection and Correction schemes. The constructed system involves using state machines immune to Single Event Upsets (SEUs) induced by neutron radiation.

Key words: Nanotechnology, Microelectronics, Single Event Upset, Hamming codes, Cyclic Redundancy Check, Static Random Access Memory, Neutron radiation

1 MOTIVATION

Neutron-induced Single Event Effects (SEEs) are a serious issue in electronic systems used in locations with elevated levels of radiation, be that equipment used at high altitudes or in the vicinity of particle accelerators. Thus, monitoring of radiation in such environments is of vital importance. Furthermore, designing error mitigation techniques for ensuring reliability of systems working in radiation environments is important, since it enables integration of sensors and control systems.
The Application Specific Integrated Circuit (ASIC) approach enables manufacturing the whole monitoring system in one technology. Moreover, the integrated system is more efficient in terms of silicon area usage and is much more compact in comparison to FPGA implementations [1], [3].

2 INTERACTION OF NEUTRON RADIATION WITH ELECTRONIC DEVICES

Being a neutral particle, a neutron penetrating a semiconductor material is not affected by the Coulombic forces. However, since it has a relatively large mass, it can reach large depths and deploy its energy due to absorption, elastic and inelastic scattering. All these mechanisms introduce changes to the state of the device, effects of which are different depending on the type of interaction [2].
Neutron hitting the surface has penetrating power and can form a displacement tree in the bulk of the device. Clusters of vacancies and interstitial atoms expand due to thermal diffusion and the lattice returns to stability according to the self-healing phenomenon known as annealing.
Diffusing vacancies can combine with interstitials or impurity atoms, and the interstitials can exchange a dopant atom, thus displacement damage can lead to degradation of performance of the device [2].
Other results of neutron radiation can be indirect ionization effects, also called Total Ionizing Dose (TID) effects. Irradiation triggers creation of electron-hole pairs, followed immediately by partial recombination. If electron-hole pairs have been created in the oxide of a MOS transistor, the difference in mobilities can cause hole trapping in the oxide, while the electrons that have not recombined leave this area. Such phenomenon causes creation of new interface states. This results in threshold voltage shifts, leakage currents and band bending near the oxide interface [2].
Single Event Effects are very often the reason for faults in electronic devices. If an energetic particle hits the sensitive node of a device, it can generate a path of electron-hole pairs. The gathered charge can cause a change of the device operation, for example a transistor, provided that the charge is greater than the critical charge of the device. Such current pulse can travel through the circuit and can be latched in a storage element. SEEs are commonly divided into hard and soft errors, the former ones being irreversible and usually destructive for the device, while the latter ones are reversible and can be overcome by resetting the device to its initial state. The most widely experienced soft errors are Single Event Transients (SETs), affecting the logic circuits, and Single Event Upsets [2], [5]. The particle strike can induce creation of electron-hole pairs, which in turn can create an abrupt pulse if the charge is gathered in the sensitive node of the circuit. Such pulse can change the state of the device and be propagated in the circuit. To calculate the number of electron-hole pairs created the Linear Energy Transfer (LET) value is used, which specifies the energy transferred to material by incident particles. The SEU is illustrated in the Figure 1.

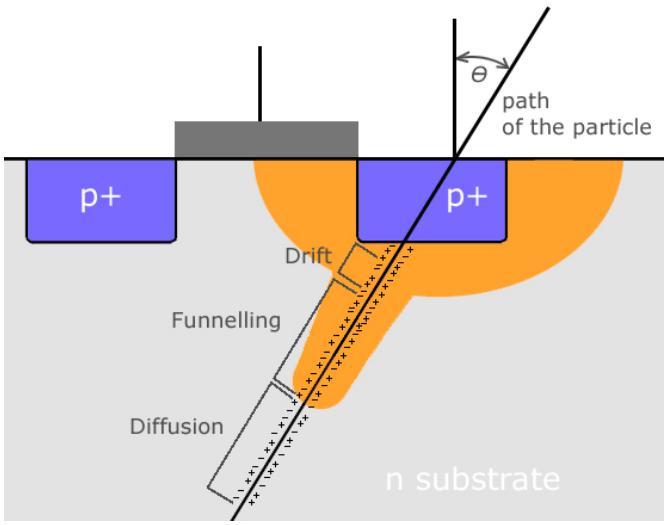

Figure 1. Single Event Upset phenomenon

3 SINGLE EVENT UPSETS MITIGATION

SEU mitigation techniques can be divided into hardware and software levels. The former refers to altering the design from the technological side, whereas the latter concerns only changes introduced to the design before implementation.

3.1 Rad-hard technology

Mitigation of radiation induced faults on the technology level has been proven to be very effective. Rad-hard technologies include adjustments of the process steps in order to optimize the device in terms of radiation sensitivity. Also the layout of the circuit can be modified to eliminate the parasitic devices and leakage currents, which is the feature of Enclosed Layout Transistors and designs using guard rings. The radiation induced latch-up can be prevented in the Silicon-On-Insulator (SOI) technology.

3.2 System hardening

Mitigation techniques can be implemented also on the system level. This is applicable when the technology cannot be altered or when the design rules do not allow for any layout modifications.

Error Detection And Correction

Error Detection And Correction (EDAC) codes can be used to protect storage elements (flip-flops, registers). The most commonly used types of coding are Hamming, Reed-Solomon and Cyclic Redundancy Check (CRC) codes. The implemented redundant parity check bits provide means for detecting and/or correcting the SEU induced bit flips. Using codes introduces an increase in the circuit size, which depends on the redundancy used and the implementation details.

Modular redundancy

Modular redundancy is another system level technique, concerning replication of selected modules of the design. The most popular are Double Modular Redundancy (DMR), which enables single error detection and Triple Modular Redundancy (TMR), enabling both error detection and correction. These design approaches introduce the voting module, which checks if the outputs from the considered modules differ. Modular redundancy techniques require large overhead in silicon area usage. They are implemented widely in the FPGA based designs.

Partial redundancy

An alternative for modular redundancy approaches in logic circuits are partial redundancy techniques. Based on the varying susceptibility to SEU of different nodes in the circuit, the ones most vulnerable to radiation-induced faults are chosen for replication. This greatly improves the area usage.

System refreshing

A very simple solution for mitigating radiation errors are refresh techniques. The system is equipped with a counter, which forces the system to return to the initial state. This is done regardless if any errors have occurred or not.

Memory scrubbing

Memory scrubbing can be implemented for storage elements. It consists in reading all bits or words in the memory and verifying if they are correct. If a bit or word differs from a predefined pattern, error correction has to be introduced.

4 RADIATION-TOLERANT READOUT SYSTEM FOR AN INTEGRATED SRAM-BASED NEUTRON DETECTOR

4.1 System description

The readout system has been designed to cooperate with an SRAM-based neutron radiation detector. The neutron fluence detector consists of two modules: radiation sensitive SRAM and radiation insensitive readout system.

The detector memory is designed as an Asymmetric SRAM optimized for storing ones and programmed with only zeroes to increase its vulnerability to SEUs [8]. The control system reads the memory contents and counts all disagreements between the read data and reference data that are supposed to be effects of SEUs. After reading, the memory is reprogrammed if SEU is detected, and the gathered information is sent to main computer and stored in a database. The system outputs the number of SEUs collected from the detector. Therefore, the measured number of SEUs in sensing memory can be recalculated to neutron fluence and displayed as a history of generated radiation. The readout system able to tolerate SEUs is based on a Finite State Machine (FSM) concept. Detected errors in the control modules are corrected and suitable information is send to main computer. This data can be used to verify the algorithms used to SEUs mitigation. Additionally, temperature sensor and gamma radiation sensor based on the Radiation-Sensitive Field Effect Transistor (RadFET) can be connected to readout system using standard serial transmission [1]. A block diagram of the system is shown in the Figure 2.

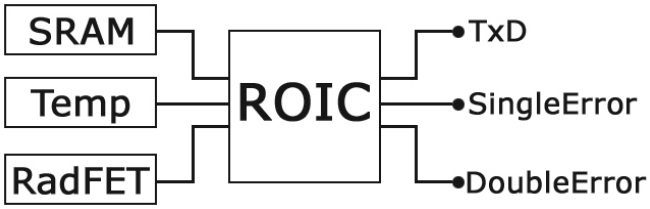

Figure 2. Block diagram of the designed system

ROIC stands for ReadOut Integrated Circuit. It is described in more detail in further sections of this paper.

4.2 Mitigation techniques

The design uses the standard AMS CMOS 0.35 μm technology for silicon, thus only system level mitigation techniques have been implemented. First Gray codes were used to explicitly specify the state values in the state machines. Then Hamming codes were applied to protect the state register. This concept is illustrated in the Figure 3. Functionality for single error detection and correction together with additional double error detection capability has been implemented. Since double error probability is relatively low, it is sufficient to provide means for refresh of the system in such case. Furthermore, Cyclic Redundancy Check codes were applied to protect the transferred to computer datagram [4], [6], [7].

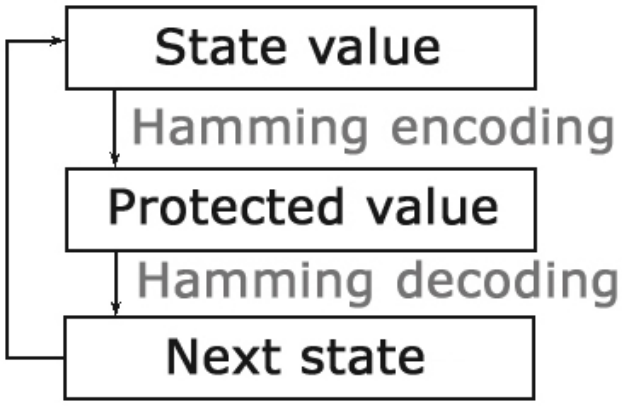

Figure 3. The algorithm of Hamming codes implementation

4.3 Implementation in silicon

The readout system has not been yet manufactured. However, a complete design path has been elaborated, covering all design stages from behavioral description in VHDL, through synthesis, Place and Route, layout generation and simulations. The comparison between the consumed silicon area after synthesis and after layout generation is given in Table 1.

Table 1. Comparison of consumed silicon areas

	Width [μm]	Height [μm]
Synthesis (chip core only)	550	550
Layout (core with pads)	2100	2100

Table 1 shows a significant difference between the core size and the chip size. Increase of the chip size in layout is due to a large number of ports used in the design. All used ports were necessary to obtain the desired functionality of the system. Furthermore, their dimensions are given in the technology specifications and cannot be changed. The size difference, however, gives a possibility of extending the system while preserving the silicon area used. Provided the same number of ports is used, the design can have some additional functions or additional protection mechanisms, like for example Triple Modular Redundancy. Generated layout view in Cadence Virtuoso Layout Editor is shown in the Figure 4 [1]. The area between core and Input/Output cells is a channel used for power rings and port connections, can however be used for extension of the core area.

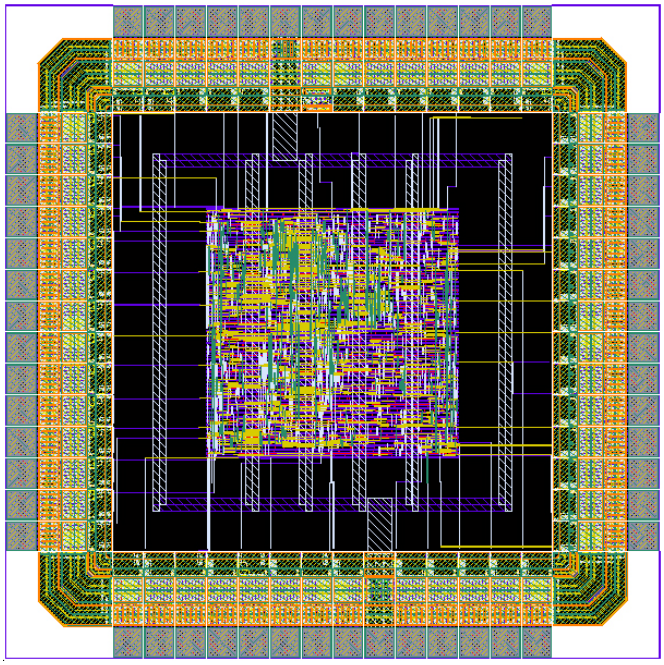

Figure 4. Layout generated using Cadence Virtuoso Layout Editor environment

4.4 Results

The controller has not been tested in the radiation environment. The behavioral and post-layout served as a verification of functionality. Additionally, some random single and double errors were injected using VHDL into the state registers to simulate the behavior of the system in the radiation environment. Single errors have been proven to be transparent to the state machines, whereas double errors caused a refresh of the system and jump to the initial state. Thus, the SEU mitigation in the state registers functionality has been confirmed in behavioral simulations. The delays introduced by Hamming encoder and decoder modules were shown to be negligible [1].

5 CONCLUSIONS

The readout system of neutron fluence SRAM-based detector has been targeted as an ASIC design. As a detector static random access memory sensitive to neutron induced SUEs were used [8]. A great advantage is the size of the chip and capability of integration with the sensing SRAM. The design is pads limited, thus there is a possibility of improving the system with for example Triple Modular Redundancy. Functionality of the system has been tested only on the behavioral level. However, the error mitigation method has been verified in VHDL simulations. Hamming codes have been shown to be an effective yet efficient way of protecting state registers in state machines. Single and double errors in the state registers are tolerated. It should be noted that not all parts of the system need to be radiation tolerant. For example the state of the address counter for the SRAM based detector can be altered with no effect on the system functionality. In the case of an error the memory is still being read, however different address is generated and data are read at a different location.

The design should be manufactured and then tested in environment with elevated level of radiation. The SRAM based neutron detector can be implemented either as a separate device, connected to the ports of the readout circuit or incorporated into the controller chip. This is possible due to implementation of both designs in the same technology. Thus, the readout system can be used in different configurations, with just slight changes to the original design.

ACKNOWLEDGMENTS

We acknowledge the support of the European Community-Research Infrastructure Activity under the FP6 "Structuring the European Research Area" program (CARE, contract number RII3-CT-2003-506395).

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