Unified Compact Model for Generic Double-Gate MOSFETs


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ABSTRACT

A generic double-gate (DG) MOSFET follows a generalized voltage equation from the first integral of Poisson equation and Gauss’ law at the two gates, which is implicit and, in general, non-integrable when the channel is doped. Only DG with undoped channel can be solved with implicit surface-potential solutions, or approximate surface-potential solutions for doped symmetric-DG (s-DG) structures. The most challenging task in DG compact modeling is the surface-potential solutions for the generic asymmetric-DG (a-DG) doped-channel device: scalable over oxide thickness (from DG to SOI), channel thickness and doping (from ultra-thin-body/fully-depleted to bulk-like/partially-depleted), and bias (a-DG to s-DG). Once it is conquered, the model will be able to cover different structures and operations with seamless transitions. In this paper, we present solution methods towards such a unified MOS compact model based on the unified regional approach. Regional implicit/explicit solutions are available for the generic doped s-DG/a-DG in accumulation, depletion, volume-inversion regions, and approximate solutions in strong-inversion region for the two gate’s surface potentials. The unified solutions can be obtained either iteratively or explicitly with use of smoothing functions, which contain the essential physics captured in the regional solutions that are otherwise impossible to obtain, and can be applied to terminal current/charge models with physical layer thickness and doping scalability. The results demonstrate a first step towards unification of MOS compact models for the existing (bulk/SOI) and emerging (multiple-gate) MOSFETs with seamless transitions and selectable accuracy.

Keywords: compact model, partially-/fully-depleted SOI, MOSFET, FinFET, symmetric/asymmetric double gate, ultra-thin body, unified regional surface potential

1 INTRODUCTION

With four decades of scaling of conventional bulk and silicon-on-insulator (SOI) CMOS technologies, non-classical MOSFET structures have been emerging, ranging from earlier (planar) partially-depleted (PD) or fully-depleted (FD) ultra-thin body (UTB) SOI MOSFETs, to emerging (vertical) symmetric/asymmetric double-gate (s-DG/a-DG) or tri-gate (TG) FinFETs either on SOI or bulk-Si, and to recent surrounding-gate (SRG) silicon-nanowires (SiNW) such as omega-gate (OG) or gate-all-around (GAA) MOSFETs, all implementable with compatible CMOS technologies. Structural and material parameters of these devices include gate workfunction, gate insulator thickness and dielectric constant, channel thickness and doping, in addition to device geometries such as channel length and width that, depending on device structure, are determined by lithography in planar devices or by process in vertical devices such as FinFET’s height and width or SiNW’s diameter. Operations of these devices are also different. Conventional bulk MOSFETs are four-terminal whereas SOI MOSFETs are essentially three-terminal devices, with a special concern for floating-body (FB) effect in PD SOI. FD/UTB SOI MOSFETs, however, are similar to a-DG with “independent-gate” bias (ia-DG) MOSFETs that have four terminals. On the other hand, s-DG, “common-gate” a-DG (ca-DG) (asymmetry due to gate workfunction and oxide thickness difference), and TG FinFETs as well as OG/GAA SiNWs are truly three-terminal devices in which the channel is only in contact with the source/drain terminals. All these various device types/operations can be called in general multiple-gate (MG) MOSFETs, and they are inter-related through variations in physical/structural parameters and terminal biasing.

To design integrated circuits using these current/future device building blocks, a compact model physically describing the terminal (large-signal DC and small-signal AC) characteristics, that is also scalable with geometry (channel length/width/depth) as well as terminal bias and temperature, is needed. One approach to developing the various models, which is currently being pursued by various modeling groups, is to develop a particular model for each of the specific device structure of interest. This approach mainly arises as a result of the complexity involved in formulating a “generic” model that can encompass all different types and operations of various MG MOSFETs. The limitations of these “specific” models, however, lie in their inability to extend beyond the region of validity in which the model is being formulated and,
moreover, they cannot switch from one device type/operation to another while for real devices transformation among various types/operations should really be seamless. For example, a model developed for undoped a-DG MOSFETs cannot be applied to devices when channel doping cannot be neglected. A model specifically for common-gate s-DG/ca-DG MOSFETs (including doped channel and even a third top-gate and corner transistors) can only be used for DG/TG FinFETs with one common-gate bias but not for ia-DG MOSFETs. A model developed in cylindrical coordinate for GAA SiNWs is simpler than using Cartesian coordinate and better suited for small-diameter SiNWs but cannot be extended to TG/OG FinFETs. In fact, assumptions for using “undoped,” “common-gate,” or “cylindrical-coordinate” are various simplifications of the complex problem for the most generic independent/asymmetric double-gate (ia-DG) MOSFET with doped channel.

Another approach to the generic MG-MOSFET modeling, which is presented in this paper, is to pursue a unified compact model for the most generic case, which encompasses various simplified devices within one core model. It starts with the most generic (and most difficult as well) structure of a long/width/thick ia-DG MOSFET with doped channel. Once conquered with physical scaling of all physical parameters (channel length, width, thickness, doping, oxide thickness and gate workfunction), the unified model will be able to cover common-gate s-DG operation, lightly (unintentional) or undoped channel, PD-SOI or even bulk MOSFETs, with seamless transitions among device types and operations. All short-channel/narrow-width/thin-body as well as gate-doping (GD) and quantum-mechanical (QM) effects can be extended from the core model. Even TG-FinFET can be viewed as a scaled version of a thick-body DG in parallel with a top “bulk-like” MOSFET plus corner transistors, which cannot be extended from a GAA model developed under cylindrical coordinate.

2 GENERIC DG MOSFET

2.1 Generic DG Structure

A generic DG/SOI n-channel MOSFET is shown in Fig. 1, with the physical and material parameters labeled, in which the subscripts ‘1’ and ‘2’ are associated with gates 1 and 2. The channel voltage \( V_{Ch} \) is equal to \( V_{g1} \) at the source end \( (y = 0) \) and \( V_{C} \) at the drain end \( (y = L) \). \( V_{r} \) is a reference voltage that is taken as the lowest voltage in the channel region (it is equal to \( V_{b} \) if there is a body contact biased at \( V_{b} \) as for bulk-MOS; or \( V_{b} \) when there is no body contact as for SOI/DG). All voltages are absolute with respect to (w.r.t.) ground. The source/drain junction depth \( X_{j} \) can be smaller than the channel thickness \( (T_{Si}) \) as in bulk/ PD-SOI MOSFETs or equal to \( T_{Si} \) as in DG/TG FinFETs.

The surface potentials along the channels of the two gates, which are the solutions of the voltage equations (first integral of Poisson equation plus Gauss’ law applied at the two gates). We define the “zero-field” potential \( \phi_{0} = \phi(X_{n}, y) \) where \( X_{n} \) is the location always having \( \phi_{n} = 0 \). In s-DG, \( \phi_{1} \) is always located in the middle of the channel \( (X_{c} = T_{Si}/2) \) and \( \phi_{1} = \phi_{2} \), and in ca-DG \( (V_{g1} = V_{g2} \) and \( \phi_{1} \neq \phi_{2}) \), \( \phi_{0} \) is usually located inside the channel. For ia-DG, however, \( \phi_{0} \) can be located outside the channel (i.e., no zero-field inside the channel). Since it is known [1] that the first integral of Poisson equation cannot be obtained for the generic a-DG with doped channel, we will treat the generic a-DG by extending the s-DG solution as two coupled solutions of the individual MOSFETs with their own \( \phi_{01} \) and \( \phi_{02} \).

![Figure 1: Generic DG MOSFET structure and coordinate.](image)

2.2 Generic Voltage Equation

In order to formulate a set of equations encompassing various device types/operations including extension to bulk-MOS, we take a long-, wide-, and thick-channel generic doped DG nMOSFET and start with gradual-channel approximation (GCA) and Boltzmann statistics. The electron and hole concentrations under non-equilibrium condition are given by

\[
\begin{align*}
n &= n_{i}e^{\phi_{n}/\phi_{th}} \\
p &= p_{i}e^{\phi_{p}/\phi_{th}}
\end{align*}
\]

where \( \phi_{n} \) and \( \phi_{p} \) are the electron and hole quasi-Fermi potentials (imref), respectively. \( n_{i} \) is the intrinsic carrier concentration and \( v_{th} \) is the thermal voltage. The “remote” charge neutrality demands that \( n_{0} - p_{0} = N_{D} - N_{A} \) where \( n_{0} \) and \( p_{0} \) are the electron and hole concentrations in the charge-neutral region, and \( N_{D} \) and \( N_{A} \) are the donor and acceptor concentrations (assuming complete ionization), respectively. Thus, in a thick-channel MOSFET, one always has

\[
\begin{align*}
N_{D} &= n_{i}e^{\phi_{n}/\phi_{th}} \\
N_{A} &= p_{i}e^{\phi_{p}/\phi_{th}}
\end{align*}
\]

which are the important “self-consistent” remote-charge boundary conditions in a bulk/DG MOSFET with source/drain injection, especially near the flat-band voltage [2]. This is due to the required assumption of x-
independent quasi-Fermi potentials (otherwise, first integral of Poisson equation cannot be obtained).

Under equilibrium conditions (i.e., no channel-voltage injection, like in an MOS capacitor),
\[ N_D = n_0 e^{-\phi / \phi_s} \]  
(3a)
\[ N_A = n_0 e^{\phi / \phi_s} \]  
(3b)
from which the bulk Fermi potential can be calculated \[ \phi_f = v_a \sinh^{-1} \left( \frac{N_A - N_D}{2n_i} \right) \]  
(4)
For \( N_A >> N_D \), (4) is given by
\[ \phi_f = v_a \ln \left( \frac{N_A}{n_i} \right) \]  
(4a)
The Poisson equation under GCA is written as
\[ \frac{d^2 \phi}{dx^2} = -\rho / \varepsilon_S = -q \frac{(p-n+N_D-N_A)}{\varepsilon_S} = \frac{q}{\varepsilon_S} \left( n_0 e^{\phi / \phi_s} - n_0 e^{-\phi / \phi_s} \right) \]  
(5)
\[ = \frac{qN_S}{\varepsilon_S} \left[ e^{\phi - \phi_s / \phi_s} - e^{-\phi - \phi_s / \phi_s} + 1 - e^{-\phi - \phi_s / \phi_s} \right] \]  
(5a)
\[ = \frac{qN_S}{\varepsilon_S} \left[ e^{\phi - \phi_s / \phi_s} - e^{-\phi - \phi_s / \phi_s} + 1 - e^{-\phi - \phi_s / \phi_s} \right] \]  
(5b)
\[ = \frac{qN_S}{\varepsilon_S} \left[ e^{\phi - \phi_s / \phi_s} - e^{-\phi - \phi_s / \phi_s} + 1 - e^{\phi - \phi_s / \phi_s} \right] \]  
(5c)
\[ = \frac{qN_S}{\varepsilon_S} G(\phi, V_c). \]  
(5d)
\[ V_{cr} = \phi_f - \phi_p. \]  
(6)
is the electron–hole quasi-Fermi potential difference (imref split) as a result of the voltages applied at the source/drain. In (5), the hole imref can be derived (see Appendix) as
\[ \phi_p = v_a \ln \left( \frac{N_A - N_D}{2n_i} \right) \right] + \left( \frac{N_A - N_D}{2n_i} \right) \right] + \left( \frac{N_A - N_D}{2n_i} \right) \right]. \]  
(7)

Based on \( E_x = -d \phi / dx \) and
\[ \frac{d^2 \phi}{dx^2} = -\frac{dE_x}{dx} \frac{d \phi}{dx} = E_x \frac{dE_x}{d \phi} \]  
(8)
as well as the boundary conditions (at \( x = 0 \) and \( x = X_{oa} \)):
\[ \phi(0, y) = \phi_s(y), \quad E_x(0, y) = E_{oa}(y) = -\phi_s(y), \]  
(8a)
\[ \phi(X_{oa}, y) = \phi_s(y), \quad E_x(X_{oa}, y) = E_{oa}(y) = -\phi_s(y), \]  
(8b)
(5) can be integrated out as
\[ E_{oa}^2 - E_{oa} = \int_{x=0}^{x=X_{oa}} E_d dx = \int_{\phi}^{\phi_s} d \phi \frac{d \phi}{E_x} \]  
(9)
\[ = \frac{qN_S}{\varepsilon_S} G(\phi, V_c) d \phi \]  
(9a)
\[ = \frac{qN_S}{\varepsilon_S} \left[ e^{\phi - \phi_s / \phi_s} - e^{-\phi - \phi_s / \phi_s} \right] \]  
(9b)
\[ + \int_{-\phi_s}^{\phi_s} \left[ e^{\phi - \phi_s / \phi_s} - e^{-\phi - \phi_s / \phi_s} \right] \]  
(9c)
\[ = \frac{2qN_S}{\varepsilon_S} \left[ \phi_s(\phi, \phi_s, V_c). \right] \]  
(9d)
As \( x = X_{oa} \) is always defined as the zero-field location with \( E_{oa} = -\phi_s = 0 \) (assuming due to \( V_{g1} \) alone), (9) can be written as a “normalized” (to \( \sqrt{2qN_S / \varepsilon_S} \)) surface field at gate 1:
\[ F_b(\phi_s, \phi_{oa}, V_{oa}) = \left[ \int_{\phi_s}^{\phi_s} G(\phi, V_c) d \phi \right]^{1/2} = \frac{E_{oa}}{\sqrt{2qN_S / \varepsilon_S}} \]  
(10a)
\[ = -\phi_s \left[ e^{(\phi_s - \phi_s) / \phi_s} - (\phi_s - \phi_s) \right] \]  
(10b)
in which \( \phi_s = \phi_s(V_{oa}), \quad \phi_{oa} = \phi_s(V_{oa}), \quad V_{oa} = V_{g1}/V_{th}, \quad \phi_F = \phi_{oa}/V_{oa} \), and
\[ V_{oa} = V_{g1}/V_{th} \]  
are the normalized (to \( v_a \)) surface potential, zero-field potential, hole imref, and channel voltage, respectively. \( \text{sgn}(x) \) is the sign function. Applying the Gauss law at gate 1 (\( x = 0 \)),
\[ E_{oa} = -\phi_s = \frac{e_{oa}}{\varepsilon_S} \]  
(11)
\[ V_{g1} = \int_{1}^{V_{g1}} \]  
(11a)
\[ V_{g1} = \int_{1}^{V_{g1}} \]  
(11b)
\[ C_{oa1} = \frac{\varepsilon_{oa1}}{\varepsilon_{oa1}} = K_{oa1} \]  
(11c)
where \( \phi_s \) is the gate workfunction, \( Q_{oa1} \) is the fixed oxide charge density, and \( K_{oa1} \) is the oxide dielectric constant at gate 1, it gives one (input) voltage equation for gate 1:
\[ V_{g1} = \phi_s = \text{sgn}(\phi_s) \int_{1}^{\phi_s} \frac{\phi_s(\phi, \phi_s, V_c)}{\varepsilon_S} \]  
(12a)
for the (coupled) \( \phi_s \) and \( \phi_s \) solutions, or in its normalized form:
\[ V_{g1} - \phi_s = \text{sgn}(\phi_s) \int_{1}^{\phi_s} \frac{\phi_s(\phi, \phi_s, V_c)}{\varepsilon_S} \]  
(12b)
in which \( v_{g1} = V_{g1}/V_{th} \) and \( Y_{f(1)} = \sqrt{2qN_S / \varepsilon_S} \) is a “normalized” (to \( \sqrt{2qN_S / \varepsilon_S} \)) body factor, with
\[ Y_{f(1)} = \sqrt{2qN_S / \varepsilon_S}, \]  
(13)
Under the coordinate of Fig. 1, the Gauss law at gate 2 (\( x = T_{oa} \)) is
\[ E_{oa} = -\phi_s = \frac{e_{oa}}{\varepsilon_S} \]  
(14)
which can be applied to the first integral of Poisson equation [similar to (9) integrating from \( x = 0 \) to \( x = T_{oa} \)]. However, the second integral of Poisson equation is not obtainable with doped channel. So, this boundary condition will not be used in our formulation of the generic surface-potential solutions. Instead, we apply the similar set of equations (9)–(13) developed for gate 1 to gate 2 by changing all the corresponding subscript ‘1’ to ‘2’, as if the two MOSFETs are independent and in parallel, each having
its own surface potential ($\phi_1$, $\phi_2$) and zero-field potential ($\phi_o$, $\phi_o$). This approach also converges to bulk-MOS solutions in which $\phi_1 = \phi_2 = 0$, since (12) converges to the conventional voltage equation.

### 2.3 Generic s-DG/a-DG $\phi_j/\phi_o$ Solutions

The relations between $\phi_j$ and $\phi_o$ ($j = 1, 2$) can be obtained from regional solutions. When the sum of the two maximum depletion widths ($X_{dm1}$, $X_{dm2}$) by each individual gate is smaller than the channel thickness, the two MOSFETs are indeed in parallel and independent. When the sum of the two (individual) depletion widths is larger than $T_S$, the link between $\phi_1$ and $\phi_2$ is to find the “full-depletion” gate voltages ($V_{g1,FD}$, $V_{g2,FD}$) that satisfies the condition

$$X_{d1,FD}(V_{g1,FD}) + X_{d2,FD}(V_{g2,FD}) = T_S$$

or its “normalized” (to $1/\sqrt{\epsilon_o}$) form

$$X_{d1,FD} + X_{d2,FD} = 1/\epsilon_o$$

where $X_{d,j,FD} = X_{d,j,FD}/\sqrt{\epsilon_o}$ and $X_{d,j,FD} = X_{d,j,FD}/\sqrt{\epsilon_o}$ are the normalized depletion widths at gates 1 and 2 at the onset of full depletion, and $T_S = T_S/\sqrt{\epsilon_o}$.

Based on full-depletion approximation, by integrating Poisson equation (consider only the $N_d$ term) twice due to $V_{g1}$ alone, one obtains the relation between $\phi_1$ and $\phi_o$:

$$\phi_1 - \phi_o = qN_d X_{d1}^2/2\epsilon_o$$

(16a)

where $X_{d1}$ is the zero-field location that depends on $V_{g1}$. Similarly, for gate 2 it is given (normalized form) by

$$\phi_2 - \phi_o = qN_d X_{d2}^2/2\epsilon_o$$

(16b)

The regional solution of (12) when only the $N_d$ term is considered is given for gate 1 alone by

$$\phi_1 - \phi_o = -Y_j/2 + \sqrt{Y_j^2/4 + V_{g1} - \phi_o}$$

(17a)

Similarly, for gate 2 alone, the (normalized) solution is

$$\phi_2 - \phi_o = -Y_j/2 + \sqrt{Y_j^2/4 + V_{g2} - \phi_o}$$

(17b)

Combining (16) and (17), the individual depletion width at each gate can be obtained at any gate voltage $V_{gj}$ ($j = 1, 2$)

$$X_{d,j} = 2\epsilon_o qN_d \left(-Y_j/2 + \sqrt{Y_j^2/4 + V_{gj} - \phi_o}\right)$$

(18a)

or in normalized form

$$X_{d,j} = 2\epsilon_o qN_d \left(-Y_j/2 + \sqrt{Y_j^2/4 + V_{g2} - \phi_o}\right)$$

(18b)

In particular, the onset of “full depletion” occurs at $V_{gj,FD}$ (at which $\phi_j = 0$), which defines the full-depletion potential when (15) is satisfied:

$$\phi_{g1,j} = qN_d X_{d1,FD}^2/2\epsilon_o = \left(-Y_j/2 + \sqrt{Y_j^2/4 + V_{g1,FD}}\right)^2$$

(19a)

$$\phi_{g2,j} = \phi_{d2,j} \left(X_{d2,FD}\right) = \left(-Y_j/2 + \sqrt{Y_j^2/4 + V_{g2,FD}}\right)^2$$

(19b)

### 2.4 Unified Regional ca-DG/s-DG Solutions

There are two practical, yet general, cases for formulating the two surface-potential solutions, which can be readily applied in “bulk-like” surface-potential-based drain-current and terminal-chARGE expressions. The first is ca-DG, as for (three-terminal) FinFETs, with two gates connected, and asymmetry can arise from differences in $V_{FB}$ (due to gate workfunction and/or fixed oxide charge) and/or $C_{ox}$ (due to oxide thickness and/or dielectric constant).

s-DG is a special case of ca-DG in which $X_{d1} = X_{d2} = X_{d} = T_S/2$. The second case is ia-DG, as for (four-terminal) SOI, with two independent gate biases, in addition to possible asymmetry in $V_{FB}$ and/or $C_{ox}$. In this paper, we present results for the first case of ca-DG MOSFETs.

For ca-DG FinFETs, $V_{g1} = V_{g2} = V_g$ since the two gates share the same electrode, but

$$V_{g1} - V_{g2} = -(V_{FB} - V_{FB}) = -\Delta V_{FB}$$

(20)

may not be zero, where the flat-band difference can be due to differences in gate workfunction and/or dielectric constant and layer thickness. Substituting (19) into (15) and solving together with (20), the full-depletion voltage $V_{FD} = V_{gj,FD} - V_{FB}$ ($j = 1, 2$) can be obtained as well as the full-depletion potentials in (19). For s-DG, $V_{FD}$ can be obtained directly from (19) with $X_d = T_S/2$, and there is no need to distinguish gates 1 and 2 which, without losing generality, will be used in the subsequent formulations.

The unified depletion (or weak-inversion) model can be constructed by smoothing the regional solutions $\phi_{d1}$ and $\phi_{o}$:

$$\phi_{dep} = \phi_{o} \{\phi_{sat}, \phi_{dep} \}$$

(21)

$$\delta_{\phi} \{x, x_{sat}; \sigma\} = x_{sat} - 0.5 \left[ x_{sat} - x - \sigma \right]$$

(21a)

in which $\phi_{sat}$ is the (bulk) subthreshold regional surface potential [4]

$$\phi_{sat} = \left(-Y_j/2 + \sqrt{Y_j^2/4 + V_{gj,FD}}\right)^2$$

(22)

$$\phi_{dep} = \phi_{sat} + \sqrt{\phi_{gj}^2 + 4\phi_{sat}}$$

(22a)

The transition from (bulk-like) depletion to volume inversion can be modeled by solving (12) with $\phi_{dep}$ in (21) replacing the $\phi - \phi_o$ term in (10):

$$\phi_{dep} = V_{gj} + \sqrt{\phi_{dep}}$$

(23)

which gives the unified regional solution from depletion through volume inversion. This solution can be smoothed...
with the strong-inversion piece ($\phi_{str}$) to obtain the unified regional solution from depletion to strong inversion:

$$\phi_{s} = \phi_{dep} + \phi_{dv} + \phi_{str}$$

(24)

$\phi_{str}$ is calculated similar to bulk-MOS (presented elsewhere) by solving (12) with only the electron ($n$) and $N_d$ terms and $\phi_{dep}$ to replace the $\phi_s$ term. The regional accumulation solution ($\phi_{acc}$) is obtained from (12) similar to bulk-MOS with only the hole ($p$) term and ignoring $\phi_s$:

$$\phi_{acc} = V_{th} + V_{g} \frac{W}{2\sqrt{V_h}}$$

(25)

$$W = \frac{r}{2\sqrt{V_h}} e^{-\frac{r}{2\sqrt{V_h}}}$$

(25a)

and $L\{W\}$ is the Lambert $W$ function. The unified regional accumulation solution ($\phi_{acc}$) is given by

$$\phi_{acc} = V_{th} + 2n_d L\{W\}$$

(26)

$$V_{th} = \partial_s \left[ V_{th} \sigma_s \right] = -0.5 \left( -V_{th} + \sqrt{V_{th}^2 + 4\sigma_s} \right)$$

(26a)

The final solution is obtained by the sum of $\phi_{acc}$ and $\phi_{ds}$:

$$\phi_{s} = \phi_{acc} + \phi_{ds}$$

(27)

3 RESULTS AND DISCUSSION

3.1 Unified Regional $\phi_s$ Solutions in s-DG

The regional $\phi_s$ solutions in an s-DG MOSFET is plotted in Fig. 2(a) together with the unified $\phi_{s eff}$ solution and compared to the Medici numerical solution of the same device (without any fitting), and the corresponding derivatives are shown in Fig. 2(b). The new model for the transition from (bulk-like) depletion to volume inversion is well and smoothly modeled by $\phi_{dep}$ and $\phi_{dv}$. Other regional solutions essentially follow our unified regional approach to bulk-MOS formulation [4].

Scaling with channel doping is shown in Fig. 3 for (a) the surface potentials and (b) their derivatives, and validated with Medici data. We have also verified other parameter scaling such as channel and oxide thickness as well as ca-DG with a difference in flat-band voltage.

3.2 Application to Drain-Current Model

The developed surface-potential model is applied to our surface-potential-based drain-current model similar to bulk-MOS formulations, and the results for the gate transfer characteristics are shown in Fig. 4 for (a) the linear and
saturation $I_d$ and (b) the transconductance, which demonstrate excellent match in all regions as compared to the same numerical device without any fitting.

![Figure 4: (a) Linear and saturation current and (b) transconductance on linear/logarithm scales using the modeled surface potentials, compared with Medici data.](image)

4 SUMMARY AND CONCLUSIONS

In conclusion, the unified regional approach is applied to the surface and zero-field potential solutions of a generic DG MOSFET with doped channel, which is viewed as two coupled “half” DG linked by a full-depletion voltage that determines the onset of volume inversion. The formulation resembles (and includes) bulk-MOS expressions and can be extended to independent asymmetric-DG SOI devices. The demonstrated results for the symmetric-DG show a one step closer towards unification of an MOS core model for all different device types and operations.

APPENDIX

In the charge-neutral region, it always has

$$n_{0}p_{0} = N_{D} - N_{A}$$  \hspace{1cm} (A1)

where

$$n_{0} = n_{0} e^{\phi_{p}}$$  \hspace{1cm} (A2a)

$$p_{0} = p_{0} e^{\phi_{n}}$$  \hspace{1cm} (A2b)

from Boltzmann statistics. (A2) gives

$$n_{0}p_{0} = n_{0}^{2} e^{(\phi_{p} - \phi_{n})} = n_{0}^{2} e^{-\phi_{v}}.$$  \hspace{1cm} (A3)

where

$$\phi_{v} = \phi_{p} - \phi_{n}$$  \hspace{1cm} (A4)

is defined as the (normalized) imref split. From (A2a), and expressing $p_{0}$ in terms of $n_{0}$ using (A1), (A2a), and (A4), one obtains

$$\phi_{p} = \ln \frac{p_{0}}{n_{0}} = \ln \left( \frac{n_{0} e^{\phi_{p}} e^{\phi_{n}} + N_{D} - N_{A}}{n_{0}} \right).$$  \hspace{1cm} (A5)

which can be re-written as

$$e^{\phi_{n}} = e^{\phi_{p}} e^{\phi_{n}} + \frac{N_{D} - N_{A}}{n_{0}}.$$  \hspace{1cm} (A6)

(A6) can be written in the form of a quadratic equation

$$\left(e^{\phi_{n}}\right)^{2} - 2 \sinh \phi_{p} \left(e^{\phi_{n}}\right) - e^{\phi_{v}} = 0$$  \hspace{1cm} (A7)

in which (4) has been used:

$$\sinh^{-1} \left( \frac{N_{D} - N_{A}}{2n_{0}} \right).$$  \hspace{1cm} (A8)

The solution of (A7) is given by (7):

$$\phi_{p} = \ln \left( \sinh \phi_{p} + \sqrt{\sinh^{2} \phi_{p} + e^{\phi_{v}}} \right)$$  \hspace{1cm} (A9)

$$= \ln \left( \frac{N_{D} - N_{A}}{2n_{0}} + \sqrt{\frac{N_{D} - N_{A}}{2n_{0}}^{2} + e^{\phi_{v}}} \right).$$

It can be seen that when $\phi_{v} = 0$ (MOS capacitor), (A9) becomes (A8) ($\phi_{p} = \phi_{n}$) based on the identity

$$\sinh^{-1} (x) = \ln \left( x + \sqrt{x^{2} + 1} \right).$$  \hspace{1cm} (A10)

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