Transition Point Consideration for

Velocity Saturating Four-terminal DG MOSFET Compact Model

T. Nakagawa^{*}, T. Sekigawa^{*}, T. Tsutsumi^{*,**}, M. Hioki^{*}, S. O'uchi^{*}, and H. Koike^{*}

*Electroinformatics Group Nanoelectronics Research Institute National Institute of Advanced Industrial Science and Technology 1-1-1 Umezono, Tsukuba, Ibaraki, 305-8568 Japan nakagawa.tadashi@aist.go.jp

**Meiji University 1-1-1 Higashi-mita, Tama, Kawasaki, Kanagawa, 214-8571, Japan

ABSTRACT

A compact model for four-terminal DG MOSFETs, with the velocity saturation, and with the introduction of the transition point that separates the transport-equation dominating region and the drain electric field dominating region, is discussed. Although this model describes transistor ON-state and near-threshold behaviors excellently, it fails to produce acceptable results in deep sub-threshold region. Main cause is that the transport equation does not properly model the diffusion saturation. To solve this problem, two modifications are made in this report. One is to redefine the equation to determine the transition point. Results are compared with the original equation. The other is to modify the transport equation that guarantees that the current is always smaller than qnv_{sat} .

Keywords: compact model, MOSFET, double-gate, electron transport.

1 INTRODUCTION

Ever since silicon planar MOSFETs have become the main building blocks of the LSI, they have not allowed other device structures to replace their position. Among many alternative device structures, the double-gate (DG) MOSFET, is now recognized as the future alternative of the planar MOSFET, because of its minimum short-channel effect. And consequently, constructing a compact model for DG MOSFETs became a pressing concern.

Usually the DG MOSFET has symmetrical structure with the same gate-insulator thickness and the identical gate electrode material. It is also supposed to be used as a threeterminal transistor with one common gate, resulting in symmetric potential profile. Compact modeling of this type has been extensively studied. The alternative four-terminal mode with electrically independent two gates enables new circuit styles [1]. Asymmetric gate structure is attractive when the additional gate is used to control the V_{th} , and even for three terminal devices, different gate material for each gate is attractive to control the V_{th} without cannel doping.

We proposed a compact model for four-terminal DG MOSFETs based on double charge-sheet model [2], with the velocity saturation effect as a function of carrier density profile inside the channel, with explicit handling of drain electric field, and with the introduction of the transition point that separates the transport-equation dominating region and the drain electric-field dominating region.

Although this model describes transistor ON-state and near-threshold behaviors excellently, it fails to produce acceptable results in deep sub-threshold region. In this paper, we discuss its cause, and propose modification of the model to alleviate the problem.

2 MODELING

2.1 **Basic Equations**

We chose a double charge-sheet model as the base model, where electrons (or carriers) in the channel is split into two charge-sheets of infinitesimally small thickness. Charge-sheets are placed at the mean position of the carriers, in stead of the silicon/insulator interface. Carriers at the source-end will be calculated by solving onedimensional Poisson equation along the channel depth. Carriers are then separated into two charge-sheets at the minimum point of the potential.

As for the transport equation, we adopted the driftdiffusion model. The channel is supposed to be undoped. By adopting several assumptions we write down the transport equation for each charge-sheet:

$$-\frac{I_{\rm D}}{q} = \frac{q\mu}{C} \frac{dn(y)}{dy} n(y) + D \frac{dn(y)}{dy},\tag{1}$$

where I_D is the drain current for the interested charge-sheet, *n* is the carrier density of the charge-sheet, *y* is the axis along the channel with the origin *y*=0 at the source-end, μ is the electron mobility, *C* is the effective capacitance, and *D* is the diffusion constant [3]. The first term is for drift current and the second term is for diffusion current.

2.2 Velocity Saturation

At high lateral electric field, carrier velocity saturates. This can be expressed as

$$\mu = \mu_0 \left/ \sqrt{1 + \left(\frac{E}{E_c}\right)^2} = \mu_0 \left/ \sqrt{1 + \left(\frac{q}{CE_c}\frac{dn}{dy}\right)^2} \right.$$
(2)

where E_c is the critical electric field that describes the velocity saturation, *E* is the lateral electric field caused by the carrier density gradient. The diffusion constant *D* is linked with the mobility through the Einstein relation, $D=\mu kT/q$, which is valid even at high electric field as far as carrier is in equilibrium. If we assume that the equation is also valid in non-equilibrium condition, the transport equation will be written as follows:

$$-\frac{I_{\rm D}}{q}\sqrt{1 + \left(\frac{q}{CE_{\rm c}}\frac{dn}{dy}\right)^2} = \mu_0 \left(\frac{q}{C}\frac{dn}{dy}n + \frac{kT}{q}\frac{dn}{dy}\right).$$
 (3)

2.3 Transition Point

Once we set the maximum carrier velocity, there should be lowest number of carriers which carries the designated drain current. This turns out that the drain voltage

$$V_{\rm D} = \frac{q}{C} \left(n(0) - n(L_{\rm G}) \right) + \frac{1}{\beta} \log \frac{n(0)}{n(L_{\rm G})} \,. \tag{4}$$

has the maximum limit. To cope with the voltage larger than the maximum, we should explicitly model the socalled pinch-off effect. In our model, the transition point, L_{TR} , that separates the transport-equation dominating region and the drain electric field dominating region is defined. The drain electric field exponentially decays by the shielding effect of two gate electrodes. When the dielectric constant of gate oxides and silicon is the same, the decay constant λ is T_{tot}/π , where T_{tot} is the distance of two gateelectrodes. As ε_{OX} becomes higher (lower) than ε_{Si} , λ becomes shorter (longer).

To define transition point, we supposed most smooth connection of the electric field at the point:

$$\frac{d^2n}{dy^2} \left/ \frac{dn}{dy} = \frac{1}{\lambda} \right.$$
(5)

This determines *n* at the transition point. From the integral of eq. (3) we can in turn obtain L_{TR} . Figure 1 describes the profile of lateral potential for this model. There are four regions: (I) the source built-in potential region, (II) the drift-diffusion region, (III) the drift-only region and (IV) the drain built-in potential region. In the model, the channel under the gate comprises region II and III. And L_{TR} is the length of region II.



Figure 1. Lateral potential of the DG MOSFET

3 EXISTING PROBLEMS

Although this model describes the drain current at transistor ON state and in near-threshold region, it sometimes failed to reproduce adequate drain current in sub-threshold region.

3.1 Too Low or Negative *n* at L_{TR}

From eq. (5), we obtain

$$\frac{\lambda\beta}{q\mu_0} I_{\rm D} n_{\rm th} \left(n_{\rm TR} + n_{\rm th} \right) = \left[\left(n_{\rm TR} + n_{\rm th} \right)^2 - n_{\rm sat}^2 \right]^{\frac{1}{2}}$$
(6)
$$n_{\rm th} = \frac{CkT}{q^2}, \qquad n_{\rm sat} = \frac{I_{\rm D}}{q\mu_0 E_{\rm c}}$$

where n_{TR} is the carrier density at L_{TR} . As I_{D} approaches zero, this gives approximate carrier density at L_{TR} :

$$n_{\rm TR} \approx n_{\rm th} \left(\sqrt{\frac{\lambda \beta}{q\mu_0} I_{\rm D}} - 1 \right),$$
 (7)

which is negative for sufficiently low $I_{\rm D}$. When the source carrier density is high enough, this is not a problem, because $L_{\rm TR}$ is larger than $L_{\rm G}$, and it only means that the

drain current is not in saturation region. But when the device is in deep sub-threshold region, there is a case where the calculated L_{TR} is inside the channel and still the carrier density there is too low or negative. This situation can be avoided to set the lower limit for n_{TR} , by overriding eq. (6). But the smoothness of the surface potential at L_{TR} will be lost and a kink appears in the surface potential, which will be reflected to a kink in *I-V* curve. In Figure 2, *I-V* characteristics of a 50nm DG MOSFET in sub-threshold region are shown where a distinct kink is observed, more eminent for lower gate voltages.



Figure 2. Drain current for one charge-sheet at subthreshold region. $L_{\rm G}$ is 50 nm, the oxide thickness is both 2 nm, and the channel thickness is 5 nm.

3.2 Large Diffusion Current

When strong velocity saturation takes place, eq. (3) approaches:

$$I_{\rm D} \approx q\mu_0 E_{\rm c} \left(n + n_{\rm th} \right) = q v_{\rm sat} \left(n + n_{\rm th} \right). \tag{8}$$

It states that the diffusion current approaches a constant value even when the carrier density is very low. This means that the carrier velocity is orders higher than the saturation velocity and also than the electron thermal velocity in deep sub-threshold region.

4 MODEL MODIFICATION

To solve these problems, we first modified eq. (5). In addition to this, we tested a modified transport equation.

4.1 Redefinition of *L*_{TR}

The first problem is caused by the fact that L_{TR} is only determined by considering the potential profile. On the

other hand, $V_{\rm D}$ calculated by eq. (4) has an additional term of relative quasi-Fermi level change between the source and the drain. To make $L_{\rm TR}$ consistent with eq. (4), smooth connection of quasi-Fermi level will be more adequate. Then eq. (5) and (6) will be replaced by

$$\frac{1}{\lambda} = \frac{d^2 \psi_{\rm F}}{dy^2} \left/ \frac{d \psi_{\rm F}}{dy} \right, \tag{9}$$

and

$$\frac{\lambda\beta E_{\rm c} n_{\rm sat} n_{\rm th}}{(n_{\rm TR} + n_{\rm th}) n_{\rm TR}} = \frac{\left((n_{\rm TR} + n_{\rm th})^2 - n_{\rm sat}^2\right)^{3/2}}{(n_{\rm TR} + n_{\rm th})^3 - n_{\rm sat}^2 n_{\rm th}}.$$
 (10)

When $I_{\rm D}$ is small, $n_{\rm TR}$ then approaches to

$$n_{\rm TR} \approx \lambda \beta E_{\rm c} \frac{I_{\rm D}}{q v_{\rm sat}}$$
 (11)

Given the surface mobility of 200-600, βE_c becomes 5-15 nm⁻¹. Therefore $\lambda \beta E_c$ with decent channel thickness will be 0.2-2. Although there is the case where the carrier velocity at L_{TR} is much higher than the saturation velocity, the deviation is not so serious. Figure 3 shows the calculated *I*-*V* characteristics for the same transistor as that for Figure 2. The sub-threshold characteristics are now completely normal for wider range of gate voltages.



Figure 3. Drain current for one charge-sheet in the sub-threshold region. $L_{\rm G}$ is 50 nm, the oxide thickness is both 2 nm, and the channel thickness is 5 nm.

4.2 New Transport Equation

In the conventional approach, D changes the same way to the change of mobility. This means that D is the function of lateral electric field, and not the function of carrier density gradient. Under equilibrium condition, this makes no difference, because the electric field is linked to the carrier density profile by the equation

$$E = \frac{kT}{qn} \frac{dn}{dy},\tag{12}$$

which is obtained by differentiating eq.(4). Under non-equilibrium condition, substituting D as

$$D = D_0 / \sqrt{1 + \left(\frac{kT}{qE_c n} \frac{dn}{dy}\right)^2}$$
(13)



Figure 4. Long (upper figure) and short (lower figure) channel characteristics. Broken (solid) lines is for modified (conventional) transport.

is necessary. The transport equation (1) with eq. (2) and (13) gives diffusion current smaller than $qv_{sat}n$ for large dn/dy which is in accordance to physics. The problem remained is that the equation cannot be solved analytically. To avoid this situation, we modify both eq. (2) and (3) as

$$\frac{\mu}{\mu_0} = \frac{D}{D_0} = \left(1 + \left(1 + \frac{n_{\rm th}}{n}\right)^2 \left(\frac{q}{CE_{\rm c}} \frac{dn}{dy}\right)^2\right)^{-1/2},\tag{14}$$

which is equivalent to replace dE/dy in eq. (2) to $d\psi_F/dy$. The transport equation then becomes as

$$-\frac{I_{\rm D}}{q} = \frac{q\mu_0}{C} \left(1 + \left(1 + \frac{n_{\rm th}}{n}\right)^2 \left(\frac{q}{CE_{\rm c}}\frac{dn}{dy}\right)^2 \right)^{-1/2} \left(n + n_{\rm th}\right) \frac{dn}{dy}.$$
(15)

Comparison of two models is shown in Figure 4. Although these models give similar results for longer L_G , the modified transport equation model smaller I_D at near-threshold condition, compared to the old model and also to the device simulator results. It is caused by the simplification to obtain eq. (14). Although this modification is attractive because of entirely physics-based diffusion current, further refinement is necessary to achieve the accuracy for short channel devices.

5 SUMMARY

The equation to determine the transition point has been discussed. It was found that the smooth connection of the quasi-Fermi level produces the better results, compared to the smooth connection of the electric potential. As for the velocity saturation, the model of identical degradation for μ and *D* causes too high diffusion current in deep sub-threshold region. Modified transport was tested. Although it gave good result for a longer channel, the drain current near threshold was low, implying the need of further refining of the model.

REFERENCES

- [1] T. Kawanami, M. Hioki, H. Nagase, T. Tsutsumu, T. Nakagawa, T. Sekigawa, and H. Koike, *IEICE Trans. Inf. & Syst.*, Vol. E87-D, pp. 2004-2010, 2004.
- [2] T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki and H. Koike, *Tech. Proc.*, *WCM 2005*, pp. 183-186, 2005.
- [3] T. Nakagawa, T. Sekigawa, M. Hioki, S. O'uchi, T. Tsutsumi, and H. Koike, *Tech. Digest IWCM'06*, pp. 15-21, 2006.