Analytical Modeling Framework for Short-Channel DG and GAA MOSFETs

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ABSTRACT

A modeling framework for nanoscale, short-channel DG and GAA MOSFETs that covers a wide range of operating conditions is presented. The device electrostatics in the subthreshold regime is dominated by the capacitive coupling between the electrodes, which, in the case of DG devices, is analyzed in terms of conformal mapping techniques. We show that these results can also be successfully applied to the GAA MOSFET, by performing an appropriate mapping to compensate for the difference in gate control between the two devices. Near and above threshold, the influence of the electronic charge is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson's equation. The models are verified by comparison with numerical device simulations.

Keywords: short-channel MOSFET, double-gate, gate-all-around, nanoscale, self-consistency, conformal mapping.

1 INTRODUCTION

To achieve sufficient accuracy in the analytical modeling of short-channel, nanoscale double gate (DG) and gate-all around (GAA) MOSFETs, the multi-dimensionality of the body potential and the electronic charge distribution has to be accurately accounted for. In sub-threshold, the device electrostatics is dominated by capacitive coupling between the electrodes. For the DG MOSFET, the 2D Laplace's equation can be conveniently solved by conformal mapping techniques, yielding analytical results [1-5]. We have shown that the DG results can be successfully applied to the GAA MOSFET as well, by performing an appropriate device scaling to compensate for the difference in gate control between the two devices [6]. This mapping is described in terms of the characteristic longitudinal field penetration lengths of the DG and GAA geometries.

Near and above threshold, the influence of the electronic charge on the electrostatics is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson's equation. For finite drain voltages, the self-consistency also extends to a calculation of the quasi-Fermi potential and the drain current. In strong inversion, where the electronic charge dominates the device electrostatics, the device behavior approaches that of long-channel devices.

The DG and GAA devices considered have gate length L=25 nm, silicon substrate thickness/diameter t_{si}=12 nm, insulator thickness t_{ox}=1.6 nm, and insulator relative dielectric constant ε_{ox}=7. The doping density of the *p*-type silicon body is $1\text{x}10^{15}\text{cm}^{-3}$. As gate material, we selected a midgap metal with the work function 5.53 eV (corresponding to that of molybdenum). Idealized Schottky contacts with a work function of 4.17 eV (corresponding to that of *n*+ silicon) are assumed for the source and drain. This ensures equipotential surfaces on all the device contacts. Note the device dimensions considered are such that a classical treatment of the electron distribution is warranted.

2 CAPACITIVE COUPLING

2.1 GAA MOSFET

The contribution to the potential distribution in the device body arising from the capacitive coupling between the device contacts can be determined from Laplace's equation. We have previously discussed an approach based on 2D conformal mapping for the DG MOSFET [1-5]. In the subthreshold regime, this contribution is dominant and provides a suitable basis for the DG device modeling.

Cylindrical GAA MOSFETs are 3D structures that cannot be analyzed the same way. However, we observe that many structural similarities exist between the 2D potential distribution obtained for the DG MOSFET and that of a longitudinal cross-section through the axis of the GAA device. In fact, the major difference between the two is the field strength of the gate electrode. This effect can be expressed in terms of the so-called characteristic length, which is a measure of the penetration depth of the contact electrostatic influence along the source-to-drain symmetry axis. The characteristic lengths for the DG and GAA MOSFETs are given by,

$$\lambda_{DG} = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right)t_{si}t_{ox}} \tag{1}$$

$$\lambda_{GAA} = r_{si}\sqrt{\frac{1}{4}+\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\ln\left(1+\frac{t_{ox}}{r_{si}}\right)} \tag{2}$$

respectively [7,8], where $r_{si} = t_{si}/2$ is the radius of the GAA silicon substrate.

The potential distribution φ_{GAA} in the longitudinal cross-section of the GAA device is then obtained as follows [8]: First, we calculate the potential φ_{DG} of a DG MOSFET with an expanded gate length given by

$$L_{DG} = \frac{\lambda_{DG}}{\lambda_{GAA}} L_{GAA} \quad (3)$$

where L_{GAA} is the true length of the cylindrical device. Next, this DG potential is mapped into the GAA device by compressing it uniformly in the longitudinal direction using the scaling factor $\lambda_{GAA}/\lambda_{DG}$ (= 0.69 for the present device). This procedure is indicated in Fig. 1.

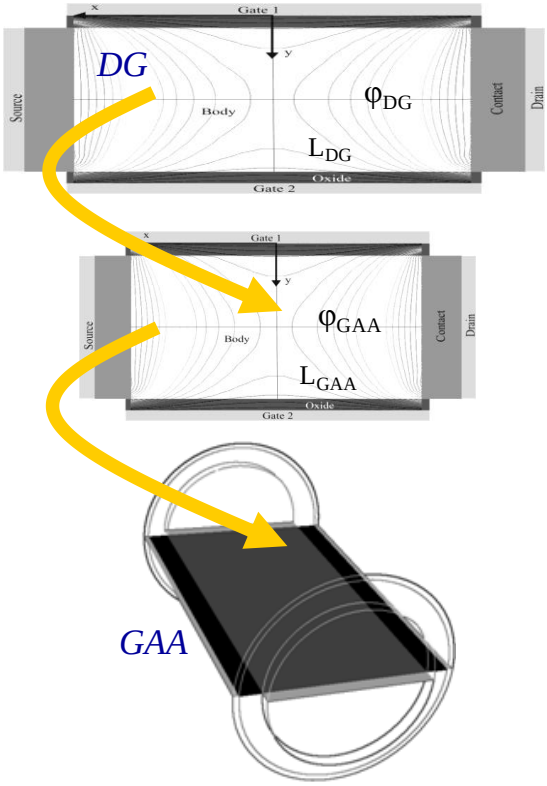

Figure 1: Schematic view of the mapping of a DG MOSFET potential distribution for an extended device of length L_{DG} (top) into the longitudinal cross-section of a GAA device of length L_{GAA} (bottom).

2.2 Verification

Figure 2a shows several subthreshold gate-to-gate potential cut lines for GAA MOSFET between the device center and the drain contact modeled with the above mapping procedure. The applied gate-source and drain-source bias voltages are V_{GS} = V_{DS} = 0 V. In Fig. 2b, modeled potential distributions along the cylinder axis are shown for V_{GS} = 0 and V_{DS} = 0 V, 0.25 V, and 0.5 V. The results are compared with numerical simulations obtained with the Atlas device simulator (symbols). An excellent overall fit between the modeled and simulated potential distributions are found.

In order to check the scaling properties of the GAA modeling scheme, the potential at the device center was modeled for a range of gate lengths, keeping all other dimensions fixed at the values used above. As shown in Fig. 2c, the modeled values agree very well with numerical simulation down to a gate length of at least 15 nm, demonstrating the good scaling properties the present modeling scheeme.

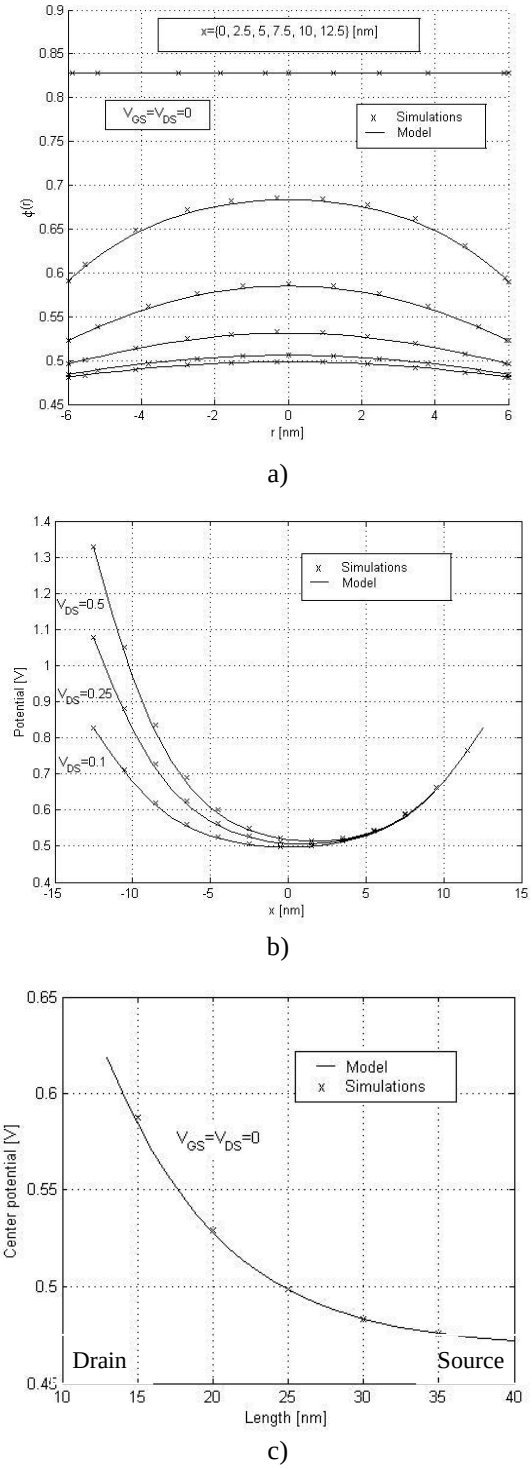

Figure 2: Modeled subthreshold potential profiles of GAA MOSFET along gate-to-gate cutlines (a) and the cylinder axis (b). Modeled center potential for devices with different gate lengths (c). Numerical simulations performed with the Atlas device simulator are shown as symbols.

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3 SELF-CONSISTENCY

3.1 Modeling procedure

Near and above threshold, the carrier contribution to the body potential cannot be neglected. In this case, Poisson's equation is divided into two superimposed parts, the first of which is the 2D capacitive coupling described by Laplace's equation, as discussed above. The second part accounts for the electrostatic effects associated with the charge carriers, which must be derived in a self-consistent manner in agreement with Poisson's equation.

Within the present framework, the self-consistent modeling of the DG MOSFET proceeds by first establishing the potential distributions along the gate-to-gate (G-G) and source-to-drain (S-D) symmetry lines. This procedure can briefly be described as follows:

Initiation:

- An estimate of the potential φ_c at the device center is made, for example, using the corresponding potential in the long-channel limit [9].
- Based on this, an approximate G-G potential distribution is introduced, such as a parabolic form or using the shape derived in the long-channel limit.
- A physics-based modeling expression is established for the potential distribution along the S-D symmetry axis. Its parameters are determined from the boundary conditions at the source and drain (the potential and its first and second derivatives), and at the device center (potential and, for example, its second derivative).
- Using the S-D potential distribution, approximate G-G distributions at different cutlines can be established, using, for example, the shapes discussed above for the central G-G cut.
- When a drain bias is applied, an initial value of the quasi-Fermi potential at the device center is also estimated, for example, $V_{Fc} = V_{DS}/2$.

Processing:

- In case of an applied V_{DS}, an update of V_{Fc} is made by first calculating the drain current (see below) based on the initial estimates.
- Next, φ_c is updated by invoking Poisson's equation at the device center, using the S-D model expression to estimate the longitudinal curvature of the potential.
- Based on this, the G-G and S-D potential distributions are updated.
- These steps can be repeated until a satisfactory accuracy is obtained.

Comments:

- We define the threshold voltage V_T as the value of V_{GS} for which the potential distribution in the central G-G cutline becomes flat at zero drain bias.
- Below threshold, the current predominantly flows near the S-D axis. Above threshold, the current shifts towards the silicon/insulator interface.
- In strong inversion, the modeling accuracy near the silicon/insulator interface must be more carefully evaluated, especially near source. This is done by introducing G-G potential distributions in this region that better reflect the proximity to the contact, i.e., that the curvature in the transverse direction should vanish at the contact.

For the GAA MOSFET, the modeling procedure is basically the same as for the DG MOSFET, using the capacitive coupling contribution to the potential obtained by the mapping technique discussed in Section 2.1. Also, when considering the contribution from the charge carriers, the axial symmetry of the GAA device must be taken properly into account.

3.2 Electrostatics

Modeled and simulated potential distributions in DG and GAA MOSFETs are compared below for the near-threshold and strong inversion regimes. Figure 3 shows the potential distributions along the S-D symmetry axis for a three combinations of V_{GS} and V_{DS}, along with the corresponding variations in the quasi-Fermi potential. In Fig. 4, examples of the strong-inversion potential distribution along the silicon/insulator interface of the DG MOSFET are presented for three different values of drain bias. In all cases, the maximum difference between the modeled potentials and the numerical simulations lies within a few millivolts. This is an excellent fit, considering that no adjustable parameters are used in the modeling.

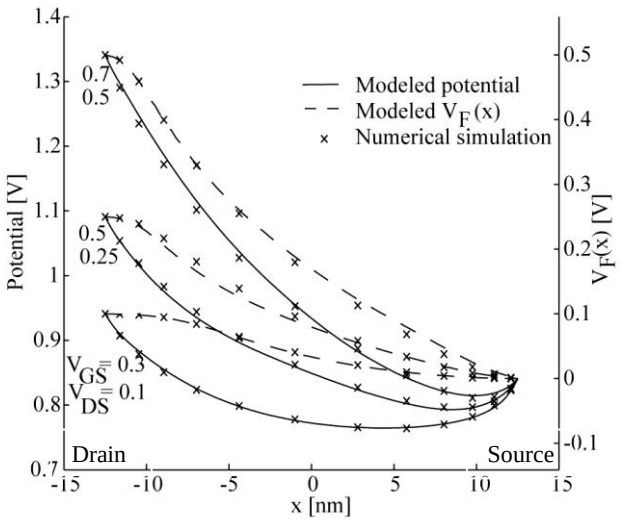

Figure 3: Modeled near-threshold and strong inversion potential profiles (solid curves) and quasi-Fermi potential profiles (dashed curves) of DG MOSFET along source-drain symmetry (a). The symbols indicate numerical simulations performed with the Atlas device simulator.

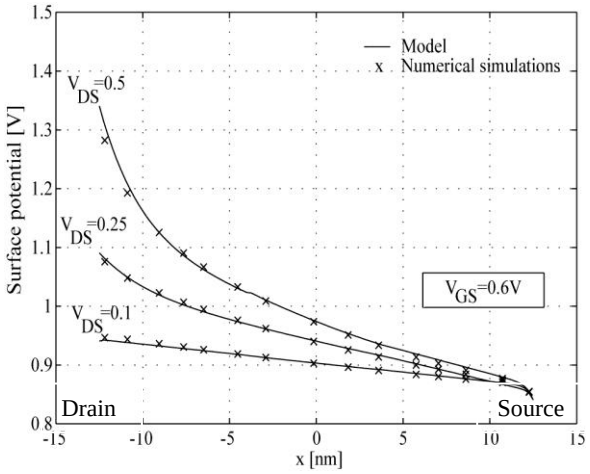

Figure 4: Modeled strong inversion potential profiles (solid curves) of DG MOSFET along the Si-SiO_2 interface (a). The symbols indicate numerical simulations performed with the Atlas device simulator.

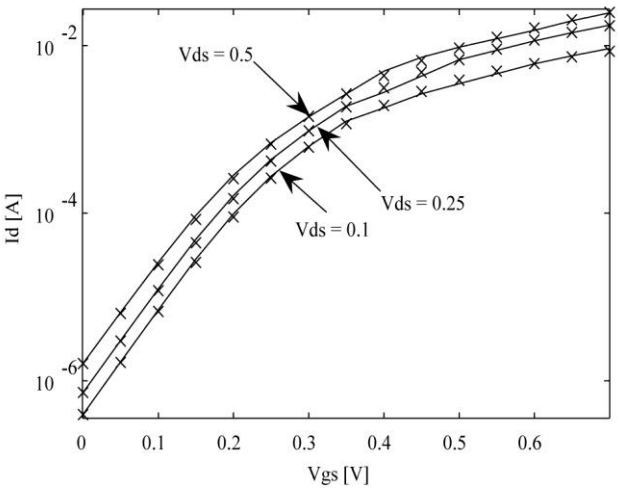

Figure 5: Modeled transfer characteristics of the drain current of the DG MOSFET for three values of drain bias (solid curves). The symbols indicate numerical simulations performed with the Atlas device simulator.

3.3 Drain Current

The small dimensions of the present devices indicate that the drain current will have the character of both drift-diffusion and ballistic/quasi-ballistic transport. Here, we discuss a drain current model based on the classical drift-diffusion formalism. For the sake of simplifying the comparison between the modeled and simulated currents, we neglect velocity saturation, in which case the drain current can be expressed as [10]

$$I_d = q\mu_n n_s(x)\frac{dV_F(x)}{dx} = q\mu_n V_{th}\frac{1-e^{-V_{DS}/V_{th}}}{\int_0^L \frac{dx}{n_{so}(x)}} \qquad (4)$$

Here, μ_n is the electron mobility in silicon, $n_s(x)$ is the sheet electron density of the channel, and $n_{so}(x)$ is the corresponding density assuming a constant V_F from source to drain. Note that once I_d is determined, the real $V_F(x)$ can be determined from (4). In the case of a DG MOSFET, we also note that I_d expressed by (4) is the current per unit width of the device.

In practice, I_d and $V_F(x)$ are determined as part of the self-consistent procedure outlined in Section 3.1

The modeled and simulated drain currents are shown in the I_d-V_{GS} characteristics of Figs. 5 and in the I_d-V_{DS} characteristics of Figs. 6. Again, an excellent agreement is observed between the modeling and the simulation results within the full range of bias conditions from subthreshold to strong inversion. The slight undulations in the modeled curves result from transitions between different modeling regimes.

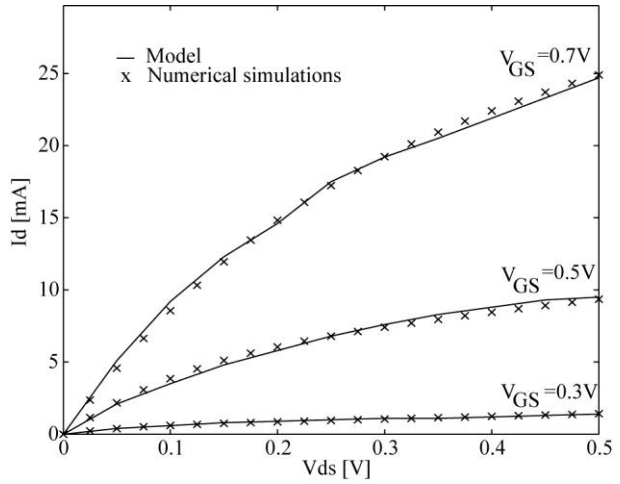

Figure 6: Modeled above threshold I_d-V_{ds} characteristics of the DG MOSFET for three values of drain bias (solid curves). The symbols indicate numerical simulations performed with the Atlas device simulator.

4 SPICE-TYPE MODELING

The above modeling framework may serve as an excellent starting point for the development of more compact modeling expression suitable for use in circuit simulators. One possibility is to use a set of generic, semi-empirical expressions for the *I-V* characteristics with parameters that can be extracted to any desired accuracy from the framework.

Typically, such a model may be based on explicit subthreshold and strong-inversion limits that are readily available from the modeling framework, and on the bias dependences of I_d near threshold expressed in terms of extractable parameters.

5 CONCLUSION

We have developed a precise, compact 2D modeling framework for calculating the electrostatics as well as the drain currents in nanoscale, short-channel DG and GAA MOSFETs. The 2D modeling is based on conformal mapping techniques and a self-consistent analysis of the energy barrier topography, that include the effects of both the capacitive coupling between the contacts and the presence of inversion electrons. Short-channel effects, including DIBL, are inherently contained in this analysis, and no adjustable parameters are used. The modeling framework covers the full range of bias voltages from subthreshold to strong inversion. Assuming a drift-diffusion transport mechanism, the drain current calculated from the present models and from numerical simulations (Silvaco Atlas) show excellent agreement.

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