Modeling of FET Flicker Noise and Impact of Technology Scaling

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ABSTRACT

In this paper, TCAD simulation tools have been developed and adopted to investigate the flicker noise performance of field effect transistors (FETs) based on advanced high-k gate oxide or SiGe/Si hetero-structure technologies. In particular, an improved impedance field method has been implemented to account for the unified carrier number-mobility fluctuation mechanisms, which are found to be important to explain the gate bias dependence of drain current noise in p-type SiGe/Si hetero-structure devices. Numerical simulations are carefully correlated with measured data. In addition, an improved compact model has been developed to account for the body bias effect that is evident in SiGe/Si devices.

Keywords: flicker noise, impedance field method, SiGe, hetero-structure FETs, high-k

1 INTRODUCTION

Ongoing scaling of device dimensions, including the introduction of new channel materials and device structures, as well as the incorporation of novel gate-stack materials, has major implications on noise performance metrics. In particular, flicker noise is intrinsically related to the interface properties and expected to be affected by new choices in technology. This paper addresses fundamental issues in flicker noise, including technology dependencies, with developed advanced TCAD capabilities. The implication of these simulations is also projected in terms of compact models.

In essence, flicker noise in FETs originates from the fluctuations of channel conductivity. Two sources contribute to this noise: the channel carrier number fluctuations (ΔN theory) and the channel mobility fluctuations ($\Delta \mu$ theory), which are both extensively reviewed in [1]. The former is induced in turn by the trapping/detrapping of oxide traps with energies close to the channel quasi-Fermi level. Recently, the correlations between these two mechanisms were discussed and a unified model is proposed ($\Delta \mu$-ΔN theory) [2].

From a TCAD perspective, the device-level numerical analysis of thermal noise in FETs is achieved by adopting the Impedance Field Method (IFM) [3], which essentially computes the noise propagation from a local source to the terminals of interest. The extension of the IFM for flicker noise simulations is based on the modeling of tunneling-based non-local charge trapping/de-trapping [4] whereby the number fluctuations are quantitatively modeled. In the previous work [5], this method was implemented in a general device simulator, PROPHET [6], with an additional post-processing step to take into account the correction term due to mobility fluctuations according to the unified model. Detailed numerical analysis based on this physical approach was conducted for high-k devices with hafnium-based gate dielectrics [5]. In this work, the mobility fluctuation correction is incorporated in the impedance field method implementation. This is necessary to simulate the observed gate bias dependence of flicker noise in SiGe/Si HMOS, because the model needs to reflect the distinctive interface properties of the buried SiGe channel and the parasitic Si surface channel. Another interesting effect that is unique in HMOS device structures is the dependence of flicker noise on body bias [7]. The re-distribution of carriers between the dual channels is responsible for the flicker noise. An improved compact model that includes this dependence is also presented.

In the following sections, we firstly describe the models that are developed for flicker noise simulations in this work. The numerical simulation results are then presented as well as correlations with experimental data. An emphasis has been placed upon the analysis of SiGe/Si HMOS devices. Following this discussion, a compact model to account for the HMOS body bias effect is briefly introduced.

2 MODELING APPROACH

As illustrated in [3], the basic idea of the IFM is to numerically calculate the noise propagation strength from a local point to the terminals of interest. Combined with the proper modeling of the local noise source, the integrated terminal noise can be obtained. Yet, The use of the IFM approach for flicker noise simulations requires some additional modifications [4]. The microscopic noise source is modeled so as to originate from the traps inside the oxide layers. In addition to the Poisson and continuity equations, a rate equation for the trapped electron density is solved self-consistently:

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$$dn_t / dt = G - R$$
$$= [(N_T - n_t)/\tau - n_t \exp(E_T - E_F / k_B T)/\tau] \quad (1)$$

where n_t is the trapped carrier density, N_T is total trap density, τ is the tunneling time calculated based on WKB method, and E_T and E_F are the trap energy level and quasi-Fermi level respectively. It is noted that this approach is non-local from a simulation viewpoint. The impedance field is then solved with the inclusion of this additional equation. According to [8], the microscopic noise source is modeled as white G-R noise in Eq. (2):

$$S_{nt}(\bar{r}) = 2(G + R) \quad (2)$$

As discussed in [5], this physical modeling approach is essential to correctly simulate the gate bias dependence of drain current noise, Sid, in the sub-threshold regime.

In order to explain the flicker noise behavior in MOS transistor devices, both carrier number fluctuation and mobility fluctuation theories were proposed [1]. The two theories predict different gate bias dependencies. In reality, correlations between these two mechanisms are often observed and unified models have therefore been developed and discussed [2]. In the previous work, a post-processing step was adopted; the noise contribution is multiplied by a correction term:

$$\eta = (1 + \mu\sqrt{n_{2D}} / \mu_{c0})^2 \quad (3)$$

where n_{2D} is the 2-D inversion carrier density and u_{c0} is a fitting Coulomb scattering parameter. In that approach, the correction applies to the sheet of 2D inversion carriers and produces satisfactory results for high-k bulk devices, where only a surface channel is present but reveals problems in the modeling of HMOS structures (a schematic plot shown in Fig.1), where both surface and buried channels exist and possess quite different interface properties. Fig. 2 shows the carrier density for both surface and buried channel as a function of gate voltage. The surface channel in general incurs much higher mobility fluctuations compared to the buried channel, due to the fact that it is closer to the Si/oxide interface. Therefore, the mobility fluctuation model has been improved in this work using a corrective as applied to the 3D carrier density in which:

$$\eta = (1 + \mu\sqrt{n_{3D}} / \mu_{c0,3D})^2 \quad (4)$$

where n_{3D} is the 3-D carrier density and μ_{c0_3D} is a function of the vertical position and assigned to a smaller value in the surface channel than that in the buried channel.

3 RESULTS & DISCUSSIONS

The proposed model has been used to numerically investigate the flicker noise performance in hafnium-based devices with 2.3 nm EOT (physical thickness 5.5 nm), 1 nm interfacial SiO_2 layer and 0.18 um gate length. As shown in Fig. 3, for a given frequency, the major noise contribution comes from traps at a certain depth into the oxides. As the frequency decreases, the peak of the noise contribution moves deeper into the oxides, because those traps correspond to longer tunneling times. At the same time, the height of the noise peak increases by about four orders of magnitude, leading to the 1/f type behavior. It should be noted that the microscopic noise source is white. This frequency dependence is produced implicitly by the impedance field computation. Based on this numerical model, the effects of the gate bias, halo doping, and trap energy distributions have been extensively investigated [5]. In Fig. 4, the simulated normalized drain noise is compared with experimental data [9] at various gate biases. By assuming an exponential trap energy distribution instead of a uniform distribution, the simulations can reproduce the correct trend of gate bias dependence.

In the study of SiGe HMOS flicker noise, a p-type device with 6 nm Si cap layer and 14 nm $Si_{0.7}Ge_{0.3}$ buried channel is simulated, together with a p-type Si bulk control device. The EOT is 8 nm and the gate length is 10 um for both devices. The I_d-V_g curves of the two devices are firstly simulated and compared with experimental data (Figs. 5(a) & (b)). In the simulations, the Darwish mobility model [10] is used with the parameters calibrated for both Si and SiGe materials. Very good agreement has been obtained for both devices and three different drain biases.

The simulated and measured noise spectra are given in Figs. 6 (a) and (b) for Si and SiGe devices, respectively. Three different gate biases are applied, ranging from sub-threshold to strong inversion for each device. In the simulations, the oxide trap density N_T is set to 3×10^{17} $1/cm^3eV$ and 4.5×10^{17} $1/cm^3eV$ for Si and SiGe devices, respectively. In the mobility fluctuation model, the scattering parameter μ_{c0_3D} is set to 1.4×10^{19} and 1×10^{20} $\sqrt{cm}/Vs$, for the surface (Si) and buried (SiGe) channels, respectively. As can be seen in the analysis, the simulation results in general agree with the measured data quite well, except for the sub-threshold gate bias where the simulated curve is about an order of magnitude smaller than the data. This discrepancy could possibly be due to the measurement accuracy, considering the small magnitude and background noise distortions observed in the measurement spectra for sub-threshold. The normalized drain current noise, S_{id}/I_d^2, at 10Hz is plotted as a function of the gate voltage in Fig. 7. The normalized noise decreases at higher overdrive voltages, in agreement with the unified noise model and saturates at the sub-threshold regime, as predicted by Reimbold's theory [11].

The importance of accounting for the different magnitudes of correlated mobility fluctuations in the surface and buried channels is illustrated in Fig. 8. In this figure, two simulated curves are shown: a) the scattering parameter u_{c0} is set to be large for both channels, resulting in a very small mobility fluctuation correction term according to Eqn(4); b) μ_{c0_3D} in surface channel is smaller than that in buried channel, which models higher mobility fluctuations in the surface channel. It is evident that in case

a), S_{id} decreases as the overdrive voltage rises above the threshold because more holes are spilled over into the surface channel as overdrive voltage increases, which is illustrated in Fig. 2. The surface channel has much lower mobility and therefore the simulations lead to a reduction of S_{id} if only number fluctuations are modeled (case (a)).Conversely, only when the significant mobility fluctuation in the surface channel is accounted (case (b)), can simulations predict a small dip followed by an increase in S_{id}, in agreement with the measured data.

In Fig.9, the normalized drain current noise, S_{id}/I_d^2, is plotted against the drain current. Both simulation results and measured data are shown for the two devices. At the same time, another quantity, $(g_m/I_d)^2$, is also plotted against the drain current. As can be seen from the figures, S_{id}/I_d^2 and $(g_m/I_d)^2$ exhibit very good correlations for both devices. This is regarded as additional evidence to support the applicability of the unified mobility model, as discussed in [9,12].

Fig. 10 shows the drain current noise as a function of body-source voltage. From the measurement results, S_{id} decreases as the body–source junction is forward biased and vice versa. This observation is consistent with the work previously reported in [7]. Such a body bias dependence is found to be unique to HMOS structures. The underlying reason for this effect is the significant contribution of mobility fluctuation to flicker noise and the re-distribution of charge between the two channels. In this work, the BSIM3v3 flicker noise compact model can be improved to take into account this body bias effect. The conventional BSIM3v3 model is shown in Eqn.(5) and the corrected BSIM3v3 model is shown in Eqn.(6).

$$Sid[A^2/Hz] = K_F \frac{Id^{A_F}}{C_{ox} L^2 f^{E_T}} \qquad (5)$$

$$Sid[A^2/Hz] = \frac{K'_F \cdot \exp(Vb_F \cdot Vb) \cdot Id^{A_F}}{Cox \cdot L^{L_F} \cdot W^{W_F} \cdot f^{E_F}} = \left(\frac{K'_F \cdot \exp(Vb_F \cdot Vb}{W^{W_F} \cdot L^{L_F - 2}}\right) \cdot \frac{Id^{A_F}}{Cox \cdot L^2 \cdot f^{E_F}} \qquad (6)$$

where C_{ox} is the unit-area capacitance, S_{id} is the drain current noise power spectral density, Id is the drain current, f is the frequency. K_F , E_F and A_F are fitting parameters. W is the channel width and L is the channel length. Vb is the body bias and Vb_F, L_F, W_F are additional fitting parameters for describing the body bias effect of SiGe pHMOS devices. As can be expected from equation (6), conventional BSIM3v3's equation (5) can be used without modification. In Fig. 11, the comparison between the improved compact model and the measurement data is given for a SiGe device. The drain bias is fixed and the gate bias is varied to give two different drain current, I_d, of 100 uA (blue) and 300 uA (red), respectively. Fig.11(a) shows the case of Vb=0V and Fig.11(b) Vb=-0.4V. The improved flicker noise compact model can predict the body bias effects for flick noise and fits well the measurement results.

4 SUMMARY

In this paper the flicker noise performance in FET devices based on high-k gate materials or SiGe/Si hetero-structures have been numerically investigated. The numerical approach is based on impedance field method (IMF) and physical modeling of the local noise sources. In particular, this paper has improved upon the noise source model to account for the strong and weak mobility fluctuations in the surface and buried channels, respectively. The simulation results are correlated with experimental data, suggesting the applicability of the unified model for SiGe pHMOS devices. The body bias dependence of the SiGe HMOS devices are also observed experimentally. An improved compact model is also proposed to account for this body bias dependence.

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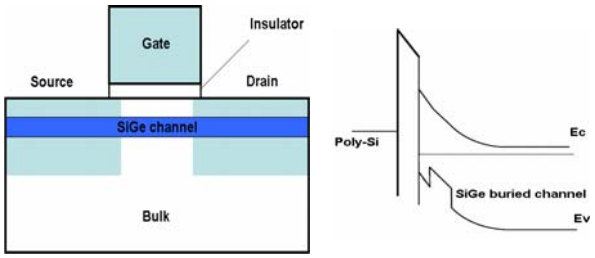

Fig.1: Schematic plots of a SiGe/Si HMOS device structure and a band diagram along the vertical direction.

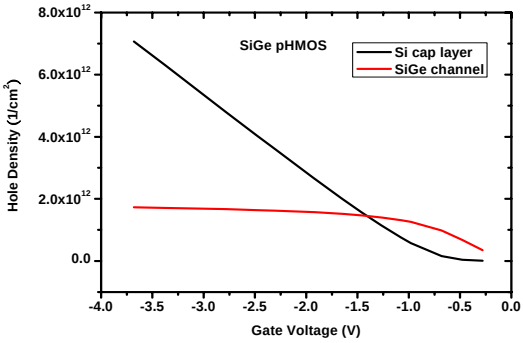

Fig.2: Simulated SiGe pHMOS carrier density for both surface and buried channel as a function of gate voltage

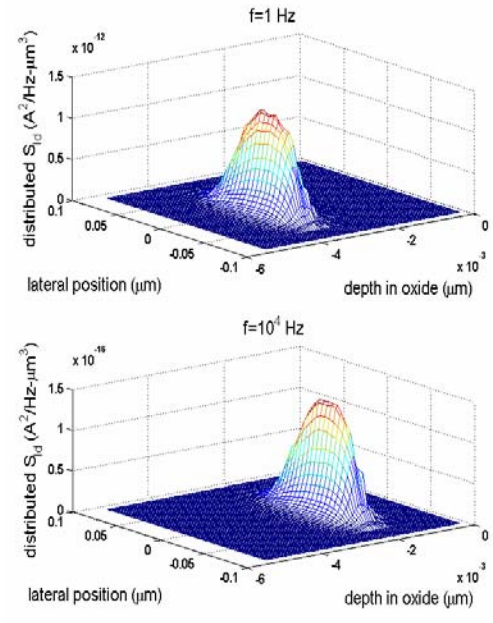

Fig. 3: Simulated profiles of distributed drain noise contributions at inside the gate oxides using the physical model. Two frequencies are simulated: (a) 1Hz; (b) 10KHz. The device gate length is 0.18μm. Vd=50mV and Vg-V_T=0.3V.

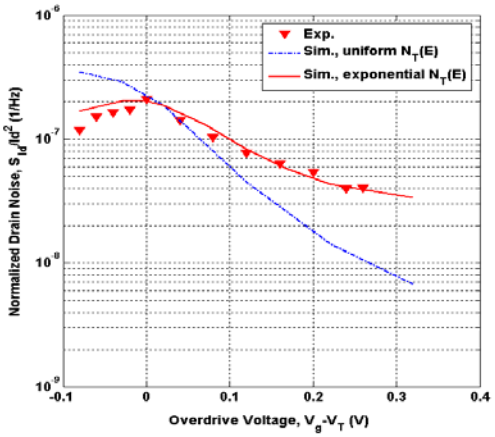

Fig. 4: Measured [9] and simulated normalized drain noise as a function of overdrive voltage. The simulations are based on the physical model with both the uniform and exponential trap energy distributions. The device gate length is 0.18μm and Vd=50mV.

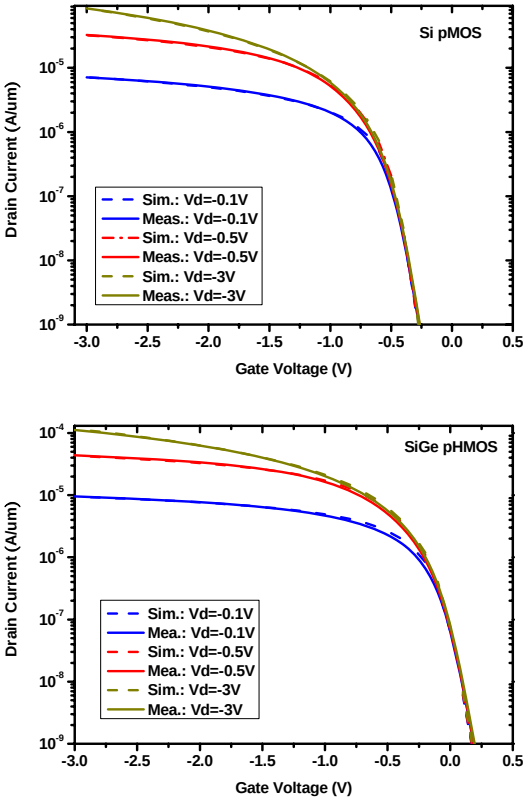

Fig.5: Measured and simulated Id-Vg characteristics for a $Si_{0.7}Ge_{0.3}$ pHMOS and a control Si pMOS. The gate length is 1 um and EOT is 8 nm. For HMOS, the Si cap thickness is 6 nm and SiGe channel thickness is 14 nm.

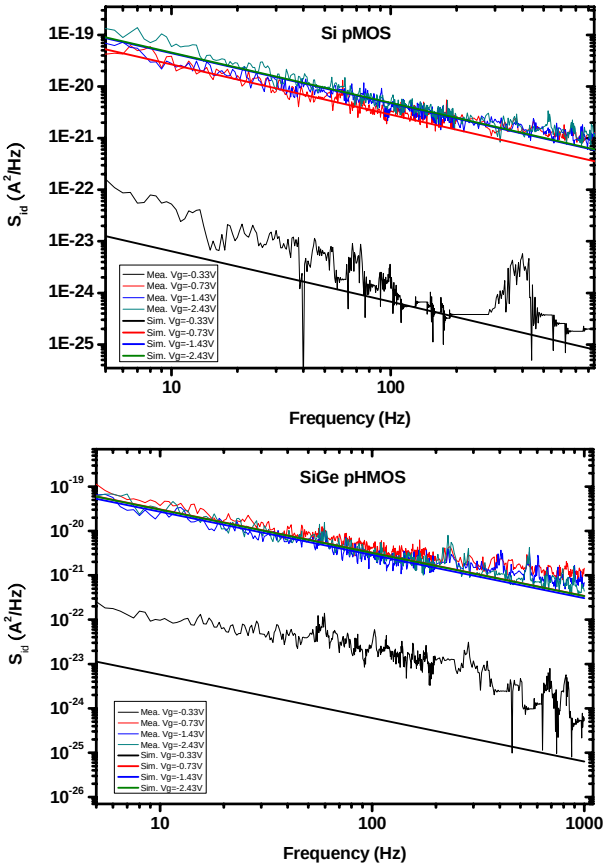

Fig.6: Measured and simulated drain current noise spectra for both the Si pMOS (a) and SiGe pHMOS (b). The frequency range is 1Hz to 1kHz. Three gate biases are used ranging from sub-threshold to strong inversion.

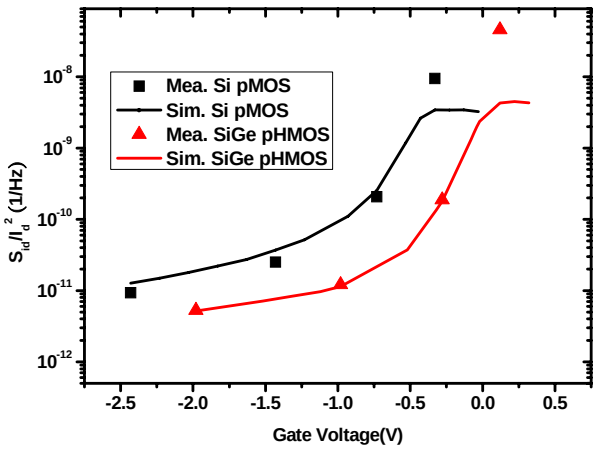

Fig.7: Measured and simulated normalized drain current noise, Sid/Id^2, at 10Hz as a function of the gate voltage. Data for both devices are shown.

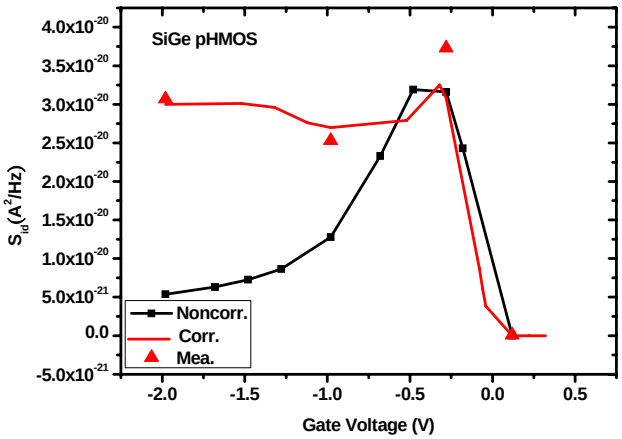

Fig.8: Measured and simulated Sid as a function of gate bias of the SiGe HMOS. Simulations include two cases: the non-corrected case neglects the contribution of mobility fluctuation, while the corrected case includes the strong contribution of mobility fluctuation from the surface channel.

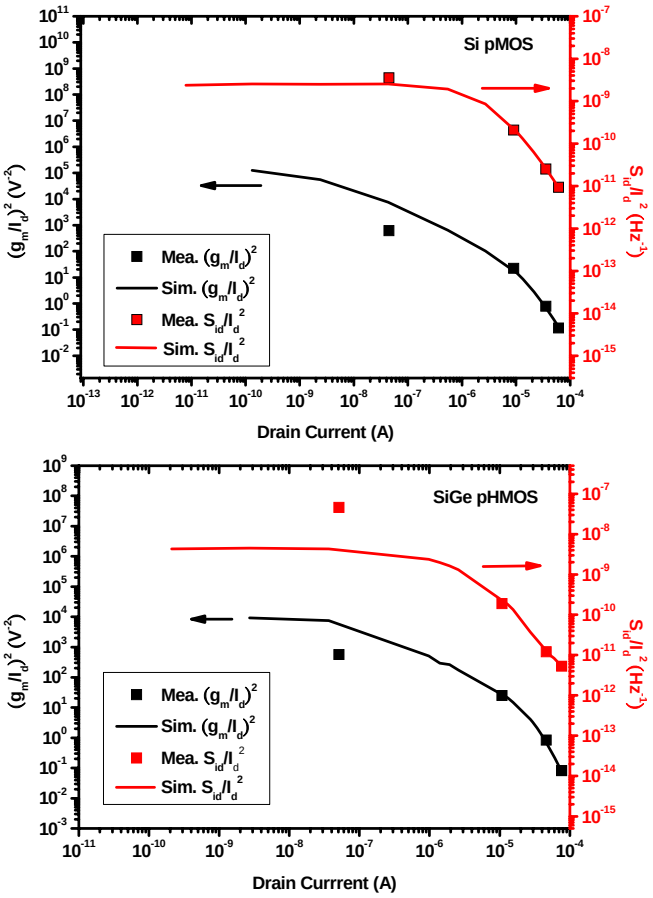

Fig.9: Measured and simulated normalized drain noise, Sid/Id^2 at 10Hz (right y-zxis), together with (gm/Id)^2 (left y-axis), as functions of the drain current. Data for both Si pMOS (a) and SiGe pHMOS (b) are shown.

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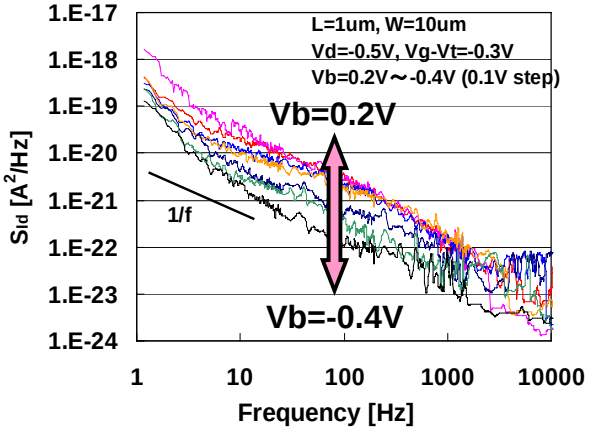

Fig.10: Measured body bias dependence of drain current noise spectrum for a SiGe pHMOS. The body bias ranges from -0.4 to 0.2 V.

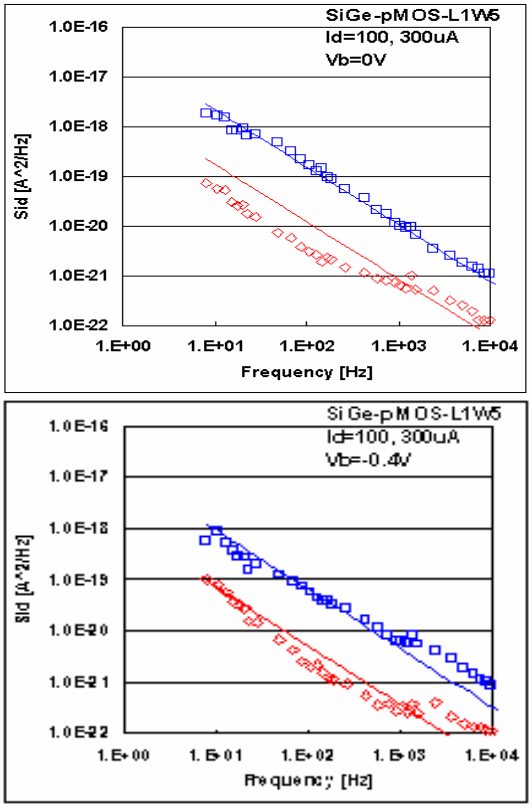

Fig.11: Comparison of improved compact model and measured noise spectra for a SiGe HMOS. Different body bias is used: 0V for (a) and -0.4V for (b), each with Id=100 uA (red) and 300 uA (blue), respectively.