Explicit Short Channel Compact Model of Independent Double Gate MOSFET

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Abstract:
This paper describes an explicit short channel compact model of an Independent Double Gate (IDG) MOSFET with an undoped channel. The validity of this model is demonstrated by comparison with Atlas numerical simulations. The model was implemented in circuit simulator in Verilog-A language to design digital and analog circuits using the independent gate structures.

Introduction:

IDG MOSFET is a particularly promising device, which is expected for sub-32nm node. This device has numerous advantages like a quasi ideal subthreshold slope and a better I_{on} current. The new flexibility offered thanks to a second gate which can be independently driven, is another one. Consequently, to design new circuits and to take advantage of this new structure, a compact model including Short Channel Effects (SCE) is crucial.

In this paper, an explicit short channel compact model of IDG MOSFET is presented. Our model includes threshold voltage roll-off, degradation of the subthreshold slope and DIBL (Drain Induced Barrier Lowering) effect.

The first part presents our explicit threshold voltage based compact model for a long channel device. Then, the explicit short channel model is explained. Finally, the model was validated by confrontation with Atlas numerical simulations [1] and was implemented in simulator in Verilog-A language.

Explicit V_{th} model for a long channel device:

Fig. 1 shows the IDG MOSFET structure. L is the gate length, T_{si} is the silicon film (or body) thickness, T_{ox1} and T_{ox2} are the front and the back gate oxide thicknesses. V_{g1} and V_{g2} are the front and the back gate voltages, respectively. $\Delta\Phi_{m1}$ and $\Delta\Phi_{m2}$, which are the work function differences between the front (respectively back) gate and the intrinsic silicon are supposed zero. The silicon film is supposed undoped.

To model this device, some assumptions were taken into account: Boltzmann statistics was chosen, the current is the sum of the diffusion and drift currents as in the Pao and Sah model [2], no quantum effect and no ballistic transport are considered for the moment.

1D Poisson equation is solved to derive the drain current I_{ds}. Boundary conditions, electrical neutrality and physical assumptions allow getting explicit $I_{ds.}$ Consequently, the explicit drain current I_{ds} is given as [3]:

$$I_{ds} = I_{ds1} + I_{ds2} \tag{1}$$

$$I_{ds1} = \frac{W}{L}\mu\, C_{ox1}\, V_{gt1,eff}\left(1 - n_{1,eff}\frac{V_{ds1,eff}}{2\left(V_{gt1,eff} + 2u_t\right)}\right)V_{ds1,eff} \tag{2a}$$

$$I_{ds2} = \frac{W}{L}\mu\, C_{ox2}\, V_{gt2,eff}\left(1 - n_{2,eff}\frac{V_{ds2,eff}}{2\left(V_{gt2,eff} + 2u_t\right)}\right)V_{ds2,eff} \tag{2b}$$

Where W is the gate width, μ the mobility (assumed constant), u_t the thermal voltage and, C_{oxj} the front and the back gate oxide capacitances respectively. Index j is for 1 or 2.

$V_{gtj,eff}$ (which have the same form as in [4]) represent the effective gate voltages and $n_{j,eff}$ are the effective coupling factors. They allow continuity between weak and strong inversion. $V_{gtj,eff}$ are defined thanks to the explicit threshold voltage, which takes into account interface coupling between front and back interfaces.

$V_{dsj,eff}$ correspond to the effective drain voltages. They allow a good modeling of the drain saturation voltage and continuity between linear and saturation regimes.

All these parameters are analytical and explicit.

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Explicit SCE model:

2D Poisson equation is analytically solved in weak inversion. The evanescent-mode analysis is used as in [5] to get the channel potential distribution:

$$\psi(x,y) = \psi_{1D}(x) + \Delta\psi(x,y) \tag{3a}$$

$$\Delta\psi(x,y) = \frac{b_1 \, sh\left(\frac{\pi}{\lambda_1}(L-y)\right) + c_1 \, sh\left(\frac{\pi}{\lambda_1} y\right)}{sh\left(\frac{\pi}{\lambda_1} L\right)} \cos\left(\frac{\pi}{\lambda_1} x\right) \tag{3b}$$

$\psi_{1D}(x)$ is the 1D surface potential and $\Delta\psi(x,y)$ the 2D correction term. λ_1, b_1 and c_1 are given in [5]. These parameters are totally explicit and depend only on the geometry of the device and on the different voltages.

Consequently, the drain current for a short channel device in weak inversion is expressed as:

$$I_{ds} = \mu W u_t \left(1 - \exp\left(-\frac{V_{ds}}{u_t}\right)\right) \frac{1}{\int_0^L \frac{dy}{\int_{-\frac{T_{si}}{2}}^{\frac{T_{si}}{2}} q \, n_i \exp\left(\frac{\psi(x,y)}{u_t}\right) dx}} \tag{4}$$

V_{ds} is the drain voltage, q the electronic charge and n_i the intrinsic carrier concentration. Due the double integral, this expression can not be considered as explicit. In order to obtain an explicit compact model, for the correction term, we assume that the equivalent potential in the channel is defined in x_{max}, the maximum potential in the x direction and in y_{min}, the minimum potential in the y direction. It is the point where the electron density is maximal. x_{max} and y_{min} are obtained when the respective derivative is zero. Thus, we get the following explicit expression of I_{ds} in weak inversion:

$$I_{ds} = -\mu \frac{W}{L} q \, n_i \, T_{si} \, u_t^2 \frac{\exp\left(\frac{\psi_{s1}}{u_t}\right) - \exp\left(\frac{\psi_{s2}}{u_t}\right)}{(\psi_{s1} - \psi_{s2})} \exp\left(\frac{\Delta\psi(x_{max}, y_{min})}{u_t}\right)\left(\exp\left(-\frac{V_{ds}}{u_t}\right) - 1\right) \tag{5}$$

$$x_{max} = \frac{\lambda_1}{\pi} \arcsin\left(\frac{\lambda_1}{\pi} \frac{sh\left(\frac{\pi L}{\lambda_1}\right)}{\sqrt{2 \, b_1 \, c_1 \, ch\left(\frac{\pi L}{\lambda_1}\right) - b_1^2 - c_1^2}}\right) \tag{6a}$$

$$y_{min} = \frac{\lambda_1}{\pi} \ln\left(\frac{\frac{b_1}{c_1}\exp\left(\frac{\pi L}{\lambda_1}\right) - 1}{1 - \frac{b_1}{c_1}\exp\left(-\frac{\pi L}{\lambda_1}\right)}\right) \tag{6b}$$

ψ_{s1} and ψ_{s2} are the front and the back gate surface potentials, derived considering the DG MOSFET as a capacitive divider. Thus, we obtain:

$$\Delta\psi(x_{max}, y_{min}) = \frac{\sqrt{2 b_1 c_1 \cosh\left(\pi \frac{L}{\lambda_1}\right) - b_1^2 - c_1^2}}{\sinh\left(\pi \frac{L}{\lambda_n}\right)} \cos\left(\arcsin\left(\frac{\lambda_1}{\pi} \frac{sh\left(\frac{\pi L}{\lambda_1}\right)}{\sqrt{2 b_1 c_1 ch\left(\frac{\pi L}{\lambda_1}\right) - b_1^2 - c_1^2}}\right)\right) \tag{7}$$

Eq. (5) should be written as the sum of the front drain current I_{ds1} and the back one I_{ds2}, with I_{dsj} given by:

$$I_{dsj} = -\mu \frac{W}{L} n_j \, c_{oxj} \, u_t^2 \left(e^{\left(-\frac{V_{ds}}{u_t}\right)} - 1\right) e^{\left(\frac{V_{gj} - V_{thj}}{n_j \, u_t}\right)} e^{\left(\frac{\Delta\psi(x_{max}, y_{min})}{u_t}\right)} \tag{8}$$

V_{thj} is the 1D threshold voltage and n_j the 1D coupling factor.

This way of writing the front and the back drain current in weak inversion at both interfaces was already used in [3], without taking into account SCE.

To include SCE in our compact model, we want to express I_{dsj} as:

$$I_{dsj} = -\mu \frac{W}{L} n_j \, c_{oxj} \, u_t^2 \left(e^{\left(-\frac{V_{ds}}{u_t}\right)} - 1\right) e^{\left(\frac{V_{gj} - V_{thj,sce}}{n_{j,sce} \, u_t}\right)} \tag{9}$$

The 2D threshold voltages $V_{thj,sce}$ and coupling factors $n_{j,sce}$ will be obtained by identification of (8) and (9). Then, expressions (10a, b, c, d and e) and (11) are obtained.

$$V_{thj,sce} = V_{thj} + \frac{-V_{tb} + \sqrt{\Delta}}{2\alpha} \tag{10a}$$

$$\Delta = V_{tb}^2 - 4\alpha V_{dq} \tag{10b}$$

$$\alpha = \frac{1}{n_j^2} sh^2\left(\frac{\pi L}{\lambda_1}\right) - \frac{\chi^2}{2}\left[ch\left(\frac{\pi L}{\lambda_1}\right) - 1\right] \tag{10c}$$

$$V_{tb} = \chi^2\left(2\left(\frac{E_g}{2} - \frac{V_{thj} + V_{gj'}}{2}\right) + V_{ds}\right)\left[ch\left(\frac{\pi L}{\lambda_1}\right) - 1\right]$$

$$V_{dq} = -2\chi^2\left(\frac{E_g}{2} - \frac{V_{thj} + V_{gj'}}{2}\right)\left(\frac{E_g}{2} - \frac{V_{thj} + V_{gj'}}{2} + V_{ds}\right)\left[ch\left(\frac{\pi L}{\lambda_1}\right) - 1\right] + V_{ds}^2 \tag{10d}$$

$$\chi = \frac{2\lambda_1^2 \tan\left(\pi \frac{T_{oxj}}{\lambda_1}\right) \sin\left(\pi \frac{T_{si}}{2\lambda_1}\right)}{\pi^2 T_{oxj}\left[\frac{T_{si}}{2} + \frac{\sin\left(\pi \frac{T_{si}}{\lambda_1}\right)}{\sin\left(\pi \frac{T_{oxj} + T_{oxj'}}{\lambda_1}\right)} T_{oxj}\right]} \tag{10e}$$

E_g is the band gap. j' represents the opposite gate: if j=1 (for the front gate), so j'=2 (for the back one) and if j=2 then j'=1.

$$n_{1,sce} = \frac{1}{\frac{1}{n_1} + \frac{\chi\left(1 - ch\left(\frac{\pi L}{\lambda_1}\right)\right)\left(\frac{E_g}{2} + \frac{V_{ds}}{2} - \frac{V_{th1,sce} + V_{g2}}{2}\right)}{sh\left(\frac{\pi L}{\lambda_1}\right)\sqrt{\left(ch\left(\frac{\pi L}{\lambda_1}\right) - 2\right)\left(\frac{E_g}{2} - \frac{V_{th1,sce} + V_{g2}}{2}\right)\left(\frac{E_g}{2} + V_{ds} - \frac{V_{th1,sce} + V_{g2}}{2}\right) - V_{ds}^2}}} \quad (11)$$

These bidimensional expressions (10a, b, c, d and e and 11) are replaced in (2a) and (2b) to get a unified model.

We also add an expression of the Early voltage (BSIM-like adapted to the DG MOSFET) to take into account the channel length modulation and the DIBL. Finally, a mobility model which considers the velocity saturation of the carriers was included.

Implementation:

This compact model was written in Verilog-A to allow simulations with Eldo (Mentor Graphics) or ADS (Agilent) circuit simulators. Comparisons between Atlas and ADS numerical simulations are shown in Fig. 2 to 8.

These figures are for an effective 30nm-channel length, the silicon film thickness is 10nm and the front and the back equivalent gate oxide thicknesses are 1nm. The carrier mobility was assumed constant.

Figure 2 represents the drain current versus the front gate voltage, for different back gate voltages from 0V to 1.2V by step of 0.2V, in linear and in logarithmic scale. The drain voltage is 5mV. Figure 3 is almost the same graphic, only the drain voltage changes: 1.2V, to prove the agreement in the saturation region. Curves in Fig. 4 show the drain current versus the drain voltage for different front gate voltages (from 0V to 1.2V) at low back gate voltage (0V). Figure 5 is almost the same graphic for a high back gate voltage (1.2V). The drain conductance is presented in Fig. 6 for different front gate voltages (from 0 to 1.2V) for a back gate voltage in weak inversion. All these figures agree very well with numerical simulations.

Finally, figures 7 and 8 prove the accuracy of our model in the case of a symmetrical device.

Conclusion:

In this work, an explicit compact model was developed for undoped IDG MOSFET. This model is valid for all operating modes: in weak and in strong inversion, in linear and in saturation region. This model can be used for a long and a short channel MOSFET. Moreover, as this model is valid for the most general case of a DG MOSFET, it means when gates are independently driven, the model can also be used for a symmetrical or an asymmetrical DG MOSFET. Comparisons with numerical simulations prove the validity and accuracy of this model. Moreover, the model was implemented in Verilog-A and circuits were simulated. The robustness of the model is excellent.

References

[1] ATLAS User's Manual – Device Simulation Software, SILVACO International Inc.

[2] H. C. Pao *et al.*, Solid State Elect., vol.9, 1966.

[3] M. Reyboz *et al.*, NSTI Nanotech, WCM 2006.

[4] BSIM4.5.0 MOSFET Model User's Manual –University of California, Berkeley.

[5] X. Liang *et al.*, IEEE Trans. Electron Devices, n°9, 2004.

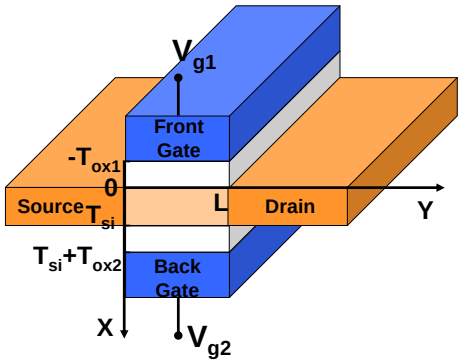

Figure 1: IDG MOSFET.

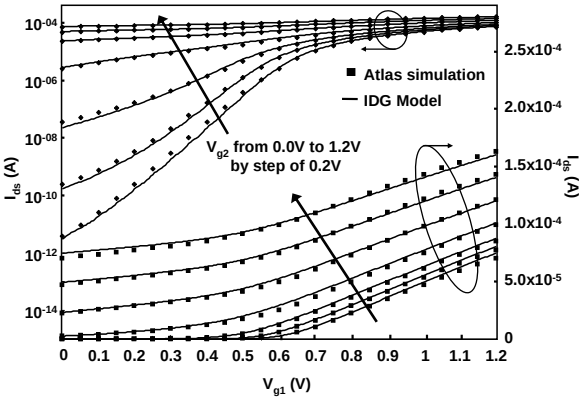

Figure 2: Drain current versus front gate voltage for several back gate voltages at low drain voltage (V_{ds}=5mV) in logarithmic and linear scales for an nMOSFET with L=30nm and W=1µm.

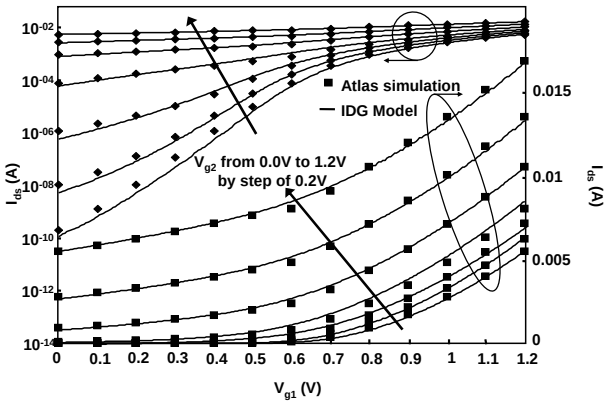

Figure 3: I_{ds} versus V_{g1} for several V_{g2} at V_{ds}=1.2V for an IDG MOSFET.

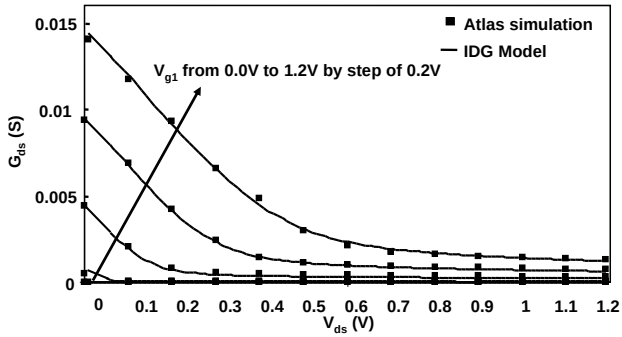

Figure 6: Drain conductance versus V_{ds} for several V_{g1} at V_{g2}=0V for an nMOSFET with L=30nm and W=1μm.

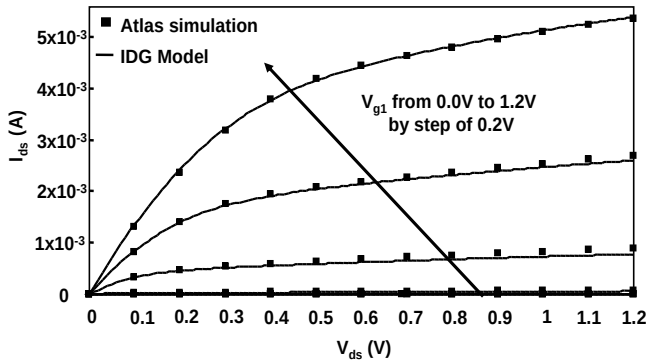

Figure 4: Comparison between Atlas numerical simulation and our compact model of the drain current versus the drain voltage for several front gate voltages at V_{g2}=0V.

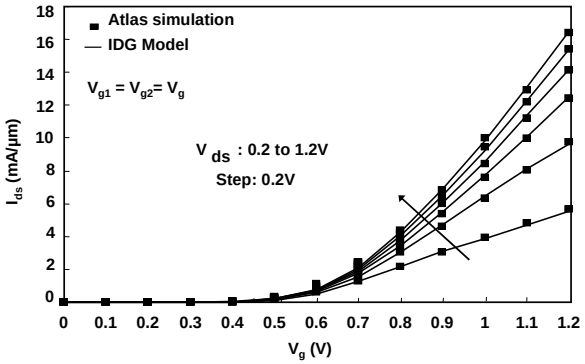

Figure 7: I_{ds} versus V_g for different V_{ds} from 0.2V to 1.2V for a symmetrical DG nMOSFET with L=30nm and W=1μm.

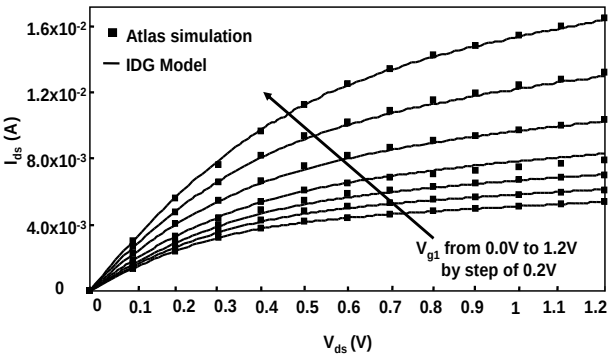

Figure 5: I_{ds} versus V_{ds} for several V_{g1} at V_{g2}=1.2V for an nMOSFET with L=30nm and W=1μm.

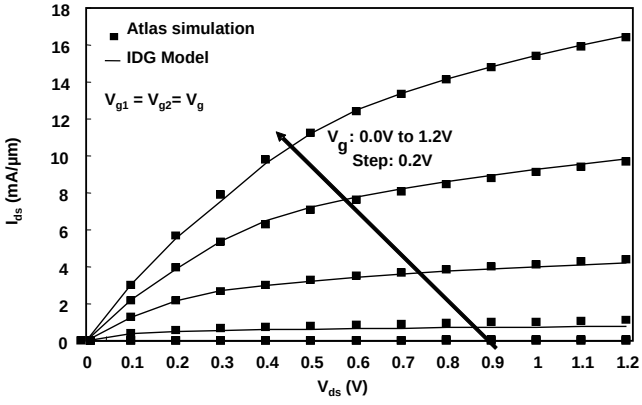

Figure 8: Comparison between Atlas numerical simulation and our model of I_{ds} versus V_{ds} for different V_g from 0 to 1.2V for a symmetrical DG nMOSFET with L=30nm and W=1μm.