A Compact Model for Temperature and Frequency Dependence of Spiral Inductor

Y.Z. Xu, and J.T. Watt

Abstract—**Spiral inductors fabricated using a 90nm CMOS process have been characterized and analyzed. The extracted series resistance increases with frequency and temperature. The extracted resistance temperature coefficient exhibits a strong dependence on operating frequency. It gradually decreases with frequency and is different from the results using DC temperature coefficients. A single π-model is used to model the measured high frequency characteristics. Two resistors and a transformer are used to model the observed temperature coefficient. One resistor has temperature coefficient around DC value, while the other one is less dependent on temperature and connected through the other side of the transformer. The model shows good fitting to all parameters, such as series resistance, temperature coefficient, inductance, quality factor and s-parameters across a wide frequency range and from room to high temperature. Discussion of process variation and corner models is also given.**

Keywords— **RF, Spiral inductor, Compact Model**

I. Introduction

WITH rapid CMOS technology scaling, transistor high frequency performance (f_t) improves and it offers opportunity to implement CMOS Radio Frequency (RF) circuits on chip with low cost and high reliability. For some RF circuits, passive components, such as on-chip spiral inductor and varactor may limit circuit performance. For example, in the circuit blocks of Voltage-Controlled Oscillator (VCO) and filters, high performance inductors are key component. For on-chip spiral inductor, metal series resistance limits quality factor (Q factor). To reduce metal series resistance, spiral inductors are normally formed by top thick metal layers. Additionally, the electrically conductive silicon substrate forms a loss source, which degrades Q factor. The degradation can increase phase noise for VCO. To improve the spiral inductor performance, extensive research has been carried out in recent years[1] [2] [3]. A few examples using process to improve inductor performance include: (a) patterned ground shield [4], (b) thick top metal using "add-on" module [5], (c) using air gap [6] and a plastic substrate layer[7].

In addition to process solutions, accurate modeling of spiral inductor helps to gain design margin, maintain good yield and avoid over design. For a practical design, it is critical to ensure the corner silicon meets design goal at high temperature. It is important to characterize the spiral inductor at high temperature and to correctly predict the statistical distribution of parameters, so that chip yield is not compromised due to inductor performance change with process and temperature.

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In this paper, we report the characterization and modeling results of a spiral inductor fabricated using a 90nm CMOS process. The extracted inductor parameters repeat the features reported recently by other researchers [8]. Specifically, the extracted series resistance [9] increases rapidly with frequency. We found that other features, such as the high frequency temperature coefficient (TC) of series resistance, is different from DC TC and has not been reported before. To model the observed characteristics, a compact π-model similar to [2] is used. Resistance temperature coefficient is modeled by using two resistors and a transformer. One resistor uses the temperature coefficient of sheet resistance of metal at DC bias condition. A less temperature dependent resistor is connected to the other side of a transformer to model the smaller temperature coefficient at high frequency. In terms of topology, this is slightly different from equivalent circuit shown in [10]. The model is found more suitable for Cu metal in deep submicron technology. A good fitting is found for all parameters, such as series resistance (R_s), R_s temperature coefficient ($TC1$), inductance (L_s), quality factor and s-parameters across a wide operating frequency and from room to high temperature.

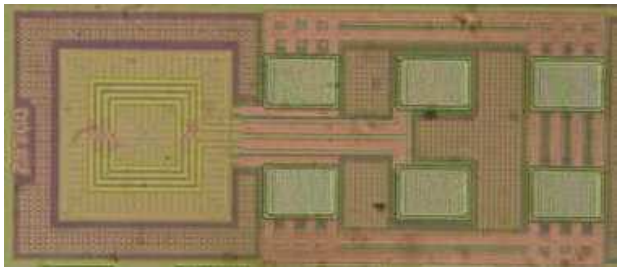

Fig. 1. A picture of spiral inductor fabricated using 90nm technology. G-S-G probe pads are placed side by side to the inductor to allow the module to fit in scribe-line.

II. Experimental Setup

Spiral inductors were fabricated with a 9-metal 90nm CMOS process. A patterned ground shield is placed at metal one layer to reduce coupling from inductor to Si substrate. High frequency test structures are implemented using a two port s-parameter structure with G-S-G pads. Standard open, short and through de-embedding structures are placed next to the spiral inductors. A picture of the

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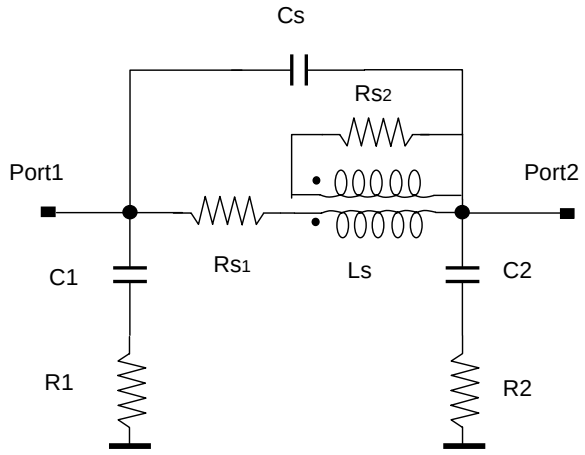

Fig. 2. Equivalant circuit of spiral inductor model. A single π-model is used as the core. A transformer is used to model the measured temperature coefficient. R_{s1} is with temperature coefficient measured at DC condition. R_{s2} has a lower temperature coefficient.

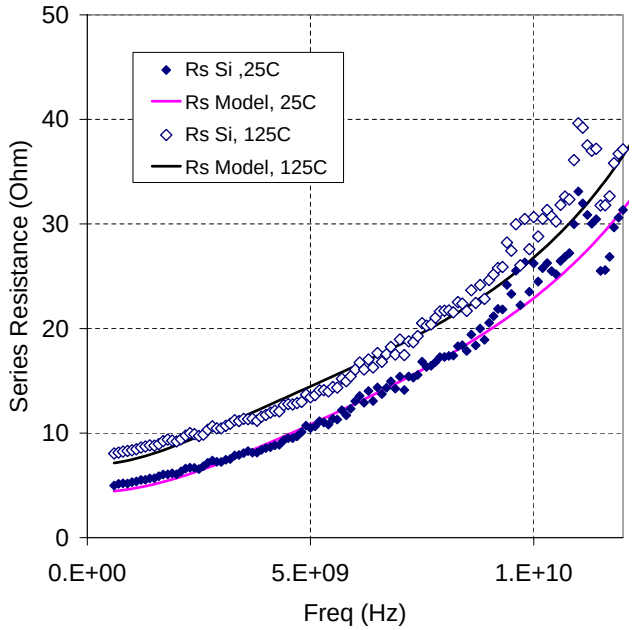

Fig. 3. Extracted series resistance at room temperature and 125°C. Series resistance increases with frequency.

spiral inductor is shown in Fig.1.

S-parameters were measured by using an Agilent E8364A PNA and Z5623A test set. Suss PA-300 probe station and SussCal5.0 were used for probing and calibration. ICCAP 2004 was used for model fitting. Power level was set at 0dBm for s-parameters measurement. Chuck temperature was controlled by Trio-Tech TC 1000.

III. Results and Discussion

The measured s-parameters are de-embedded using open-short scheme. Different schemes, such as short-open are compared to open-short schemes. There is very small difference at high frequency. Below 10GHz, there is no difference. A through de-embedding structure is also placed close to the spiral inductor. It is found that the through de-embedding is not necessary for the frequency range of interest.

A simple π-model is used to fit the measured parameters. The equivalent circuit is shown in Fig. 2, where L_s is inductance, R_{s1} is series resistance, R_{s2} is series resistance modeling skin effect and the substrate loss, C_s is coupling capacitor between two ports, C_1 and C_2 are coupling capacitors between the inductor to substrate, $R1$ and $R2$ are resistance depicting the substrate coupling current.

Assuming the spiral inductor can be modeled by a lumped π circuit, the parasitics of the spiral inductor can be extracted [9]. Series resistance is extracted from $\mathrm{Re}(|y_{12}^{-1}|)$, while inductance is extracted from $\mathrm{Im}(|y_{12}^{-1}|)$. A different extraction scheme of excluding C_s has been evaluated. The extracted parameters show the same frequency dependency for R_s and L_s regardless of whether or not C_s is excluded. A possible reason for the frequency dependence is the distributed nature of coupling capacitor, resistance and inductance. Therefore, for simplicity, the y-parameter scheme is used. Q-factor is extracted using $\frac{Im(|y_{11}|)}{Re(|y_{11}|)}$.

Fig.3 shows the extracted total series resistance. The resistance value increases with frequency and temperature. The feature of increase with frequency is similar to the results in [8], in which the steep increase of series resistance is considered beyond the frequency dependence of the skin effect. For Cu metal, a few factors, such as skin effect, the current crowding at high resistive liner layer and surface scattering of Cu, may lead to such a steep increase in resistance. As expected, the extracted resistance is higher at 125^oC. To examine the temperature dependence, a linear temperature coefficient is calculated using:

$$\frac{R_s(125^oC) - R_s(25^oC)}{100 \cdot R_s(25^oC)} \qquad (1)$$

The extracted temperature coefficient ($TC1$) is shown in Fig.4. It is clear that the temperature coefficient decreases with frequency. This is different from a simple resistor measured at DC bias, which is a dark solid line. To evaluate the equivalent high frequency temperature coefficient when metal resistors are assigned with the DC temperature coefficients, a conventional, single π-model without the second resistor and transformer has been tried to best fit the measured data, such as s-parameters, L_s and R_s. The single π model can roughly fit those parameters. However, the extracted high frequency R_s temperature coefficient clearly differs from the high frequency temperature coefficient extracted from S-parameters. It is unsuccessful to fit both room and high temperature. Using the new π-model including the second resistor and transformer, the frequency

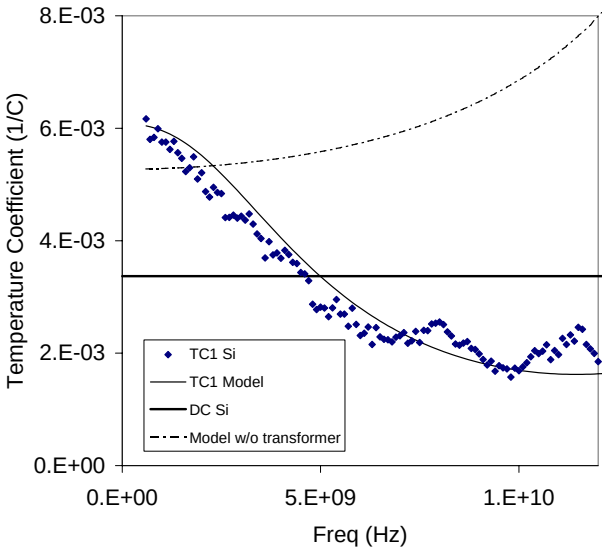

Fig. 4. Extracted temperature coefficient vs frequency.

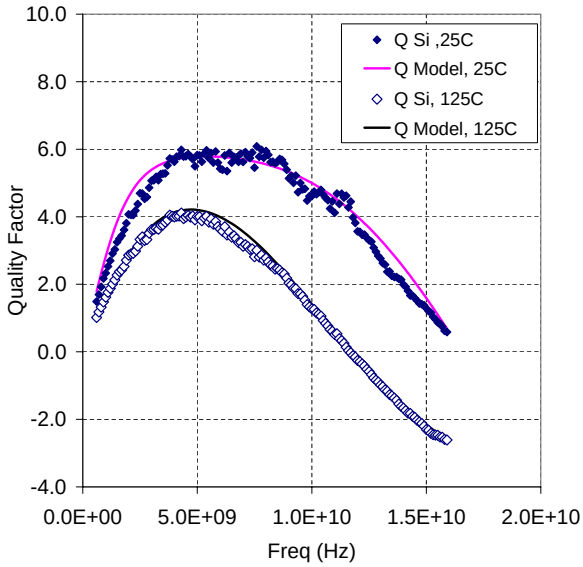

Fig. 5. Extracted spiral inductor quality factor vs frequency.

dependence and temperature coefficient of the series resistance are well depicted. For reference, the temperature coefficient measured at DC condition is also plotted in the figure as a thick solid line. The results show π-model with transformer closely follow Si results, while single π model without second resistor can not accurately model the measured silicon data.

Quality factor is one of the important parameters determining LC oscillator phase noise performance [12]. The total Quality factor can be written as:

$$\frac{1}{Q} = \frac{1}{Q_{Rp}} + \frac{1}{Q_L} + \frac{1}{Q_c} \qquad (2)$$

Here Q is the total Q factor, Q_L is quality factor for inductor, Q_L is quality factor for varactor and capacitor. The single sideband phase noise is inversely proportional to the total Q factor. In a conventional LC oscillator, the Q factor of the inductor is the smallest and apparently limits the circuit performance.

Fig.5 shows the extracted Q factor. At high temperature, Q factor reduces due to higher series resistance and more loss from substrate. The Q factor increases with frequency and peaks around 8-9GHz and gradually decreases with further increase of frequency. The peak of Q factor, however, is smaller than the conventional π-model predicts. The new π-model successfully repeats the peaks with the increase of series resistance at high frequency. It is noteworthy that at high temperature Q factor becomes negative. This feature has been discussed in reference [11] and is due to the definition of Q factor from Y-parameters. When frequency is close to resonance frequency and the substrate loss increases significantly, the Q factor can be zero and negative.

Further examination of Q temperature dependence reveals that series resistance increase can be evaluated from the Q slope reduction from low frequency to peak frequency. In this frequency domain, the impact of series resistance reduces with frequency as more voltage drops on inductor. From Fig.5, it is clear that series resistance increases with temperature. At high frequency, the loss due to coupling to Si substrate gradually increases. As can been seen from the figure, at high temperature Q factor reduces more significantly than those at lower frequency. The reduction of peak Q is about 2, while reduction of Q at 15GHz is close to 4. Compared to the absolute value, this change is significant. There is a patterned ground shield at lower metal level to reduce inductor coupling with Si substrate. Si results show that the coupling is getting stronger at high temperature. This may arise from the fact that Si substrate resistivity is more sensitive to temperature. The difference of temperature coefficient between metal layers (inductor layer and the patterned ground shield layer) is overridden by the substrate loss at high temperature and high frequency.

In addition, the model is also examined from other aspects. In Fig.6, the extracted inductance vs frequency is shown. Fig.7 shows s-parameter fitting curve. Good fit can be found for both cases.

In terms of model corners, a realistic corner methodology should be enough to cover all the process change, such as substrate resistivity, metal thickness, dielectric thickness etc. To determine the corner models, we have evaluated all process variation window and selected the corners based on statistical probability for the desired die yield.

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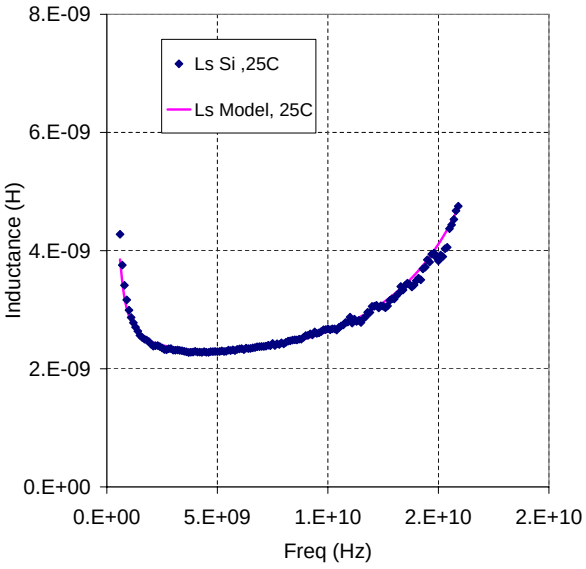

Fig. 6. Extracted inductance vs frequency.

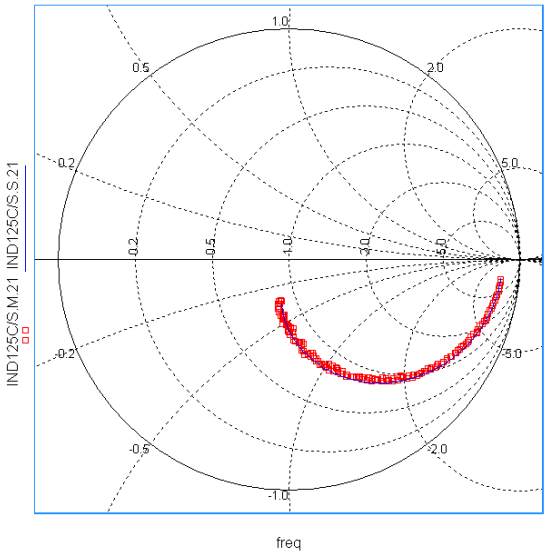

Fig. 7. Smith chart of measured S21 and model simulation results. A good fitting can be found.

IV. Conclusion

A spiral inductor fabricated using 90nm CMOS process has been characterized and analyzed. The extracted model parameters show a rapid increase of series resistance with frequency. The resistor temperature coefficient decreases with frequency. A π-model with an additional resistor and a transformer is used to model the measured data. A good fitting of Q factor, inductance and s-parameters are also shown by the model. The impact of the Q factor to *LC* oscillator is also been discussed. Finally, the model corner methodology is briefly described.

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