A Carrier-Based Analytic Model for Undoped Ultra-Thin-Body Silicon-on-Insulator (UTB-SOI) MOSFETs

Jin He, Wei Bian, Yadong Tao, Bo Li, Yu Chen

School of Computer& Information Engineering, Shenzhen Graduate School, Peking University, Shenzhen, 518055, P.R.China
Tel: 86-10-62765916 Fax: 86-10-62751789 e-mail: frankjinhe@yahoo.com

ABSTRACT

This paper presents a carrier-based continuous analytic I-V model for long channel undoped (lightly doped) Ultra-Thin-Body Silicon-on-Insulator (UTB-SOI) MOSFETs. It is based on the solution of Poisson-Boltzmann equation, and the current continuity equation of Pao-Sah current formulation in terms of the mobile carrier concentration under an appropriate boundary approximation. The model is continuous and valid for all the operation regions (linear, saturation, sub-threshold) and traces the transition between them. This preliminary model has been verified by comparing with long channel results generated by two-dimensional simulator. The predicted I-V characteristics also show in a good agreement with two-dimensional numerical simulations for all ranges of gate and drain voltages, proving the validity of the analytical model. All these indicate that this model will be an ideal core model for UTB MOSFET modelling if the appropriate second-order effects such as quantum mechanical effect, doping profile effect, short-channel effects, and poly-depletion effect are integrated into it.

Keywords: Non-classic CMOS, Ultra-thin-body, Silicon-on-insulator, Device physics, and Compact modeling.

1 INTRODUCTION

Among the non-classic CMOS device concepts ultra-thin-body silicon-on-insulator (UTB-SOI) is one of the most promising approaches for future CMOS scaling to feature sizes below 50 nm [1-5]. In contrast to other emerging device concepts UTB-SOI technology combines a planar transistor configuration with a superior sub-threshold slope resulting from a thin Si-body thickness of 5–40 nm. Together with reduced junction capacitances, high-k dielectrics, poly-SiGe gates or metal gates, these are attractive features for energy efficient CMOS logic operated at low supply voltages.

In recent years, the fabrication experiments and process improvements have been performed to explore the UTB-SOI MOSFET device characteristics and evaluate the UTB-SOI based circuit performance [1-3]. The numerical simulations have also been widely used to analyze the UTB-SOI device transport mechanism and design guideline although they are very time-consuming [4-7]. On the other hand, the compact modeling development on the UTB-SOI MOSFET has also been initialized in terms of the University Florid Double-Gate model (UFDG) by J.G.Fossum group [8] and further used to evaluate the circuit and device design.

In this paper, we first use an appropriate boundary approximation to derive the analytical solution of Poisson's equation in terms of the mobile carrier concentration and then add the effect of the back interface boundary into the field and charge equations following such a carrier -based approach. As a result, a preliminary carrier-based analytic I-V model is derived for the long channel UTB-SOI MOSFETs directly from Pao-Sah current formulation. It is shown that this analytic model covers all three regions of MOSFET operations: linear, saturation, and sub-threshold, thus maintaining full continuity between different regions, and yet is completely physics based without the need for ad hoc fitting parameters. The model has been validated by two-dimensional (2-D) numerical simulations, implying it is an ideal background for UTB-SOI MOSFET modeling if the appropriate short-channel effects, quantum effects, low and high field transport, noise, and the doping profile effect are considered.

2 ANALYTICAL MODEL

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In present study, second order considerations, such as the poly-silicon depletion, doping impurity concentration profile of the source and drain end, and the quantum-mechanical effects, are neglected for the sake of simplicity. Their exclusion, however, should not affect the general validity of the conclusions, and it is possible to incorporate them for applications where they are significant. These problems will be discussed elsewhere. Consider an undoped (or lightly doped), UTB-SOI shown schematically in Fig.1. Under the gradual-channel-approximation (GCA), the Poisson equation along a vertical cut perpendicular to the Si film takes the form:

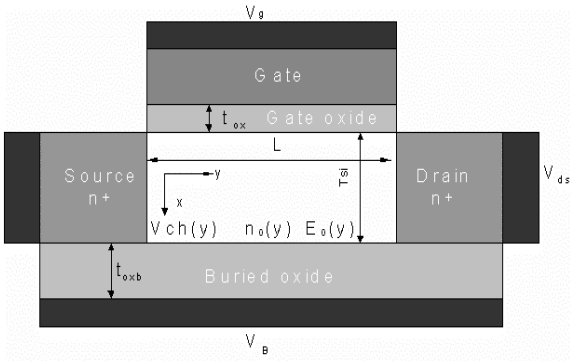

Figure 1: Coordinate diagram of an UTB-SOI MOSFET.

$$\frac{d^2\phi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} e^{q(\phi - V_{ch})/kT} \tag{1}$$

With Boltzmann statistics

$$n = n_i \exp\left(\frac{q(\phi - V_{ch})}{kT}\right) \quad n_0 = n_i \exp\left(\frac{q(\phi_0 - V_{ch})}{kT}\right) \tag{2}$$

Where all symbols have the common physics meanings.

(1) is easily converted into the following equation in the term of the mobile following Boltzmann statistics [9]

$$\frac{d^2 n}{dx^2} = \frac{1}{n}\left(\frac{dn}{dx}\right)^2 + \frac{q^2 n^2}{\varepsilon_{si} kT} \tag{3}$$

Since the potential ϕ_0 and the electrical field E_0 at the back surface of silicon body are always low compared with that of the front surface as in the general SOI case, we can first assume the back interface E_0 being zero for simplicity and we choose the reference coordinate point to being at the back surface, thus $x = 0$, $n(0) = n_o$. In this case, we can obtain the approximate potential, electron concentration and vertical field distribution. Finally, we will modify the electric field equation to compensate this assumption so to include non-zero back surface field effect.

Under the zero reference point field assumption, (3) is a general second-order differentiation equation with the exact solution

$$n(x) = \frac{n_0}{\cos^2\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} x\right]} \tag{4}$$

Substituting (4) into (2) gives the potential distribution in the silicon film as follows

$$\phi(x) = \phi_0 + \frac{kT}{q} \ln\cos^{-2}\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} x\right] \tag{5a}$$

As a result, the surface potential can be given as

$$\phi_s = \phi_0 + \frac{kT}{q} \ln\cos^{-2}\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] \tag{5b}$$

Differentiating (5a) gives the field distribution in the silicon film

$$E(x) = \left[\frac{2n_0 kT}{\varepsilon_{si}}\right]^{1/2} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} x\right] \tag{6a}$$

The analytical expressions mentioned above are based on the assumption that the back interface field is zero. However, although the back interface field is always smaller compared with that of the front surface, it is not zero due to the limited thickness of the buried oxide layer. In this case, we modify the electric field equation (6a) to add a non-zero back surface field so to include the back interface effect. Using this correction, we have

$$E(x) - E_0 = \left[\frac{2n_0 kT}{\varepsilon_{si}}\right]^{1/2} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} x\right] \tag{6b}$$

Where the back surface field E_0 will be determined by the back interface boundary continuity condition. In this case, the surface field E_s is written as

$$E_s = E_0 + \left[\frac{2n_0 kT}{\varepsilon_{si}}\right]^{1/2} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] \tag{6c}$$

If we define *that* Q_i is the inversion charge per unit area, thus $Q_i = q\int_0^{T_{si}} n(x)dx$. Then, one obtains

$$Q_i = [2n_0 \varepsilon_{si} kT]^{1/2} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] \tag{7}$$

In practice, the surface potential, field and carrier concentration are controlled by applying a gate voltage. The Gauss's law for the front interface is written as

$$V_G - \Delta\phi = \phi_S + E_s \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} = \phi_s + \frac{Q_i}{\varepsilon_{ox}} t_{ox} + E_0 \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \tag{8}$$

Since the back gate is almost ground and the electric field must be terminated by zero at the electrode, we have the boundary condition at the back surface $E_0 \frac{\varepsilon_{si} t_{oxb}}{\varepsilon_{ox}} - \Delta\phi = \phi_0 - V_B$, thus,

$$E_0 \frac{\varepsilon_{si}}{\varepsilon_{ox}} = \left[\frac{kT}{q}\ln\left(\frac{n_0}{n_i}\right) + V_{ch} + \Delta\phi - V_B\right] / t_{oxb} \tag{9}$$

Finally, substituting (7) and (9) into (8) gives the solution of Poisson-Boltzmann equation in the terms of n_o

$$V_g + \frac{t_{ox} + T_{si}}{t_{oxb}} V_B - \left[1 + \frac{t_{ox}}{t_{oxb}}\right][\Delta\phi + V_{ch}] = \frac{kT}{q}\left[1 + \frac{t_{ox}}{t_{oxb}}\right]\ln\left[\frac{n_0}{n_i}\right] - \frac{2kT}{q}\ln\cos\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] + \frac{t_{ox}}{\varepsilon_{ox}}[2n_0 \varepsilon_{si} kT]^{1/2} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] \tag{10}$$

For a given V_g, n_o can be solved from Eq. (10) as a function of V_{ch}. Along the channel direction (*y*), V_{ch} varies from the source to the drain. So does n_o. The functional dependence of n_o (*y*) and V_{ch} (*y*) is determined by the current continuity condition which requires the current constant, independent of *V* or *y*. Following Pao-Sah current formulation [10], integrating $I_{ds}dy$ from the source to the drain and expressing V_{ch}/dy as $(dV_{ch}/dn_0)(dn_0/dy)$, the drain current is written as

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$$I_{DS} = \mu \frac{W}{L} \int_0^{V_{DS}} Q_i(V_{ch}) dV_{ch} = \mu \frac{W}{L} \int_{n_{0S}}^{n_{0D}} Q_i(n_0) \frac{dV_{ch}}{dn_0} dn_0 \quad (11)$$

Where n_{0S} and n_{0D} are solutions of (10) corresponding to $V_{ch} = 0$ and $V_{ch} = V_{ds}$, respectively. Note that the dV_{ch}/dy can also be expressed as a function of n_0 by differentiating (10). Substituting these factors into (11), integrating can be performed analytical to yield:

$$I_{DS} = \mu \frac{W \varepsilon_{si}}{L} \left(\frac{2kT}{q}\right)^2 \left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] - \frac{q^2 n_0 T_{si}}{4\varepsilon_{si} kT(1 + t_{ox}/t_{oxb})} + \frac{t_{ox} q^2 n_0}{4\varepsilon_{ox} kT(1 + t_{ox}/t_{oxb})} \tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} T_{si}\right] \right]_{n_{0S}}^{n_{0D}} \quad (12)$$

3 RESULTS AND DISCUSSION

UTB SOI-MOSFET characteristics for all regions: linear, saturation, and sub-threshold, can be generated from this continuous, analytic solution. In order to test the analytic model we have simulated one long channel well-tempered UTB-SOI MOSFETs with the abrupt junction approximation of the source and drain end with 2-D numerical simulations from DESSIS-ISE® turning-off the quantum mechanism, poly-silicon depletion effect and the tunneling current effect for comparison with the analytical model. A constant effective mobility of 300 cm^2/V-s has been used for all calculations either for the numerical simulation or the analytic prediction. The simulated UTB-SOI MOSFET has a channel length of 2 μm, width of 10um, silicon gate oxide thickness (t_{ox}) of 2 nm, and the mid-gap gate, e.g. $\Delta\phi_i = 0$.

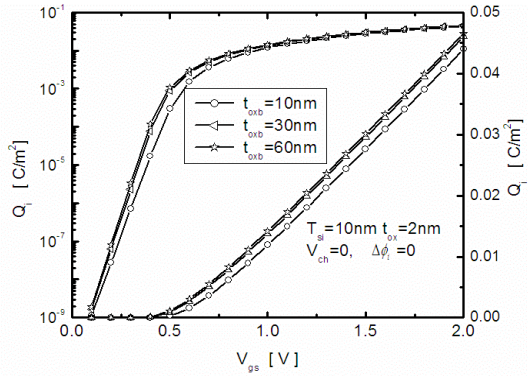

Fig.2 Inversion charge density versus gate voltage for different buried oxide layer thickness in undoped UTB-SOI MOSFETs with the midgap gates for $V_{ch} = 0$.

Fig.2 demonstrates the total inversion charge versus gate voltage for three buried oxide thickness, 10-, 30- and 60-nm. It is evident that the buried oxide thickness not only changes the threshold voltage point of the UTB SOI-MOSFETs, but also has a slight affect on the sub-threshold slope of devices. The thicker the buried oxide layer, the better the sub-threshold slope and the driving current of the UTB-SOI MOSFETs. We can expect this effect will become more significant when the channel length of the UTB-SOI MOSFETs is scaled down into nanoscale size.

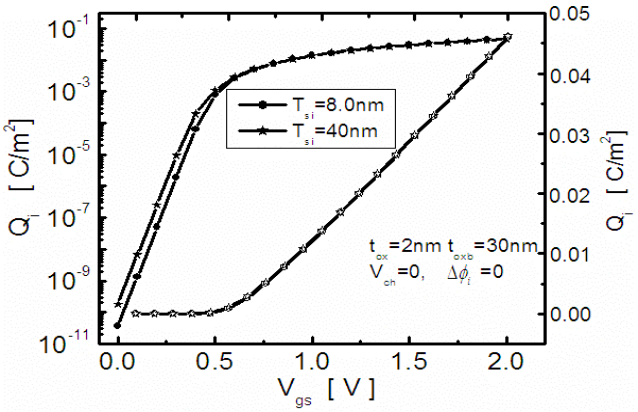

Fig.3 Inversion charge density versus gate voltage for different silicon film thickness in undoped UTB-SOI MOSFETs with the midgap gates for $V_{ch} = 0$.

Fig.3 demonstrates the dependence of the channel inversion charge on the silicon body thickness, e.g., the ‘ Volume inversion”, a non-charge-sheet phenomena [11]. It is found that the silicon film thickness only changes the amount of sub-threshold inversion charge but has no effect on the strong inversion charge density. This verified the existence of the volume inversion and illustrates the “ Volume inversion” effect can be used to control the sub-leakage current in the used of UTB SOI-MOSFETs for nano-CMOS application, as the design of the non-classical MOSFET requires the use of the ultra-thin body.

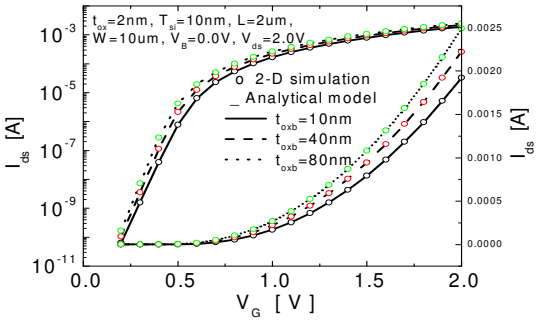

Fig.4 Plot of I_{ds} vs. V_g with t_{oxb} as a hidden parameter, compared with the 2-D numerical simulation results (open circles) for an UTB-SOI MOSFE with the mid-gap gate, $\Delta\phi_i = 0$. The same curve is plotted on both logarithmic (left) and linear (right) scales.

Fig.4 demonstrates drain current versus gate voltage for buried oxide thickness of 10-, 40- and 80-nm. It is found that the drain current increases with the increase of the buried oxide thickness in both the sub-threshold and strong inversion regions. However, the drain current gradually tends to a constant when $t_{ox}/t_{oxb} \le 10^{-2}$. An interesting result is that the sub-threshold slope of the UTB-SOI has a slight variation with the increase of the buried oxide layer thickness in this figure, which is consistent with the inversion charge change as shown in Fig.2.

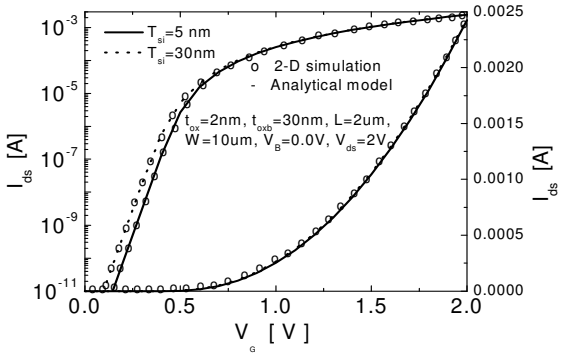

Fig.5 I_{ds}-V_g characteristics obtained from the analytic model for two different values of t_{si} (solid and dashed curves), compared with the 2-D numerical simulation results (symbols) for one UTB-SOI MOSFET.

Fig.5 shows the good comparison of the transfer curve between the analytical model prediction and the numerical simulation result for 5- and 30-nm-thick body silicon film. There are two distinct regions of operation in this figure, both sub-threshold and strong inversion in UTB-SOI MOSFETs, just like in a conventional MOSFET. " Volume inversion," in which the sub-threshold current is proportional to T_{si}, is self evident in this figure. Again, the good agreement is observed. In the meantime, Eqs. (10), (12) are dominated by the first terms for both the source end and the drain end. In this case, one obtains

$$I_{ds} = \mu \frac{W}{L} kTn_i t_{si} e^{q(V_g - V_t + \frac{t_{ox}}{t_{oxb}} V_B)/kT} \left(1 - e^{-qV_{ds}(1+t_{ox}/t_{oxb})/kT}\right) \quad (13)$$

here $V_t = \left(1 + \frac{t_{ox}}{t_{oxb}}\right)(\Delta\phi - \delta) \qquad \delta = \frac{kT}{q} \ln\left[\frac{q^2 n_i T_{si}^2}{2\varepsilon_{si} kT}\right]$.

Fig.6 is I_{ds}-V_{ds} curves calculated from the analytic model (solid curves), compared with the 2-D numerical simulation results (open circles). Both match well in both the linear and the saturation region. One key physical effect ignored in the above analysis is the inversion layer quantum effect, which make the threshold voltage increase, sub-threshold slope degradation with the reduction of the silicon film thickness. It is difficult to include all these effects in a single study. A more feasible model development process is to separately develop the second-order effect as modules and then integrate them into the core model. This approach has been applied by many model developers and the most famous is BSIM3/BSIM4. Therefore, the same approach will be used to develop the complete DG MOSFET model.

4 CONCLUSIONS

A continuous analytic model for the long channel undoped UTB-SOI MOSFETs has been derived from a carrier-based approach in this paper by solving the Poisson-Boltzmann equation with the appropriate boundary approximation. All the regions of operation and the transitions of the UTB-SOI MOSFETs are correctly described by the single set of the carrier equations. In particular, the volume inversion that cannot be captured by using the charge-sheet approximation is well accounted and the effect of the buried oxide layer on the inversion charge and channel current is demonstrated in the detail by this model. It is also shown that the predicted I-V curves coincide with 2-D numerical simulation results without any need for fitting parameter.

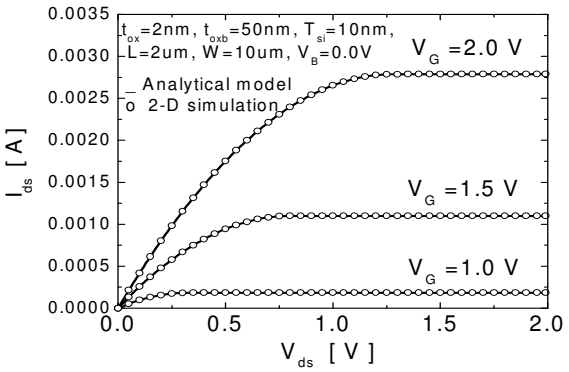

Fig.6 I_{ds}-$V_{s.}$ curves from analytic model (solid curves), compared with the 2-D numerical simulation results (open circles) for one UTB-SOI MOSFET with $\Delta\phi_i = 0$.

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REFERENCES

[1] Y.K.Choi, et al., IEEE Electron Device Letters, vol.21, pp.254-255, 2000.
[2] K.Uchida et al, IEDM Tech.Dig., 2002, pp.47-50.
[3] T.Tezuka, et al. IEEE Trans on Electron Devices, ED-50, pp.1328-1330, 2003.
[4] J.H.Choi, et al. IEEE Electron Device Letter, vol.16, pp.527-529, 1995.
[5] David Esseni, et al. IEEE Trans. Electron Devices, TED-50, pp.2445-2454. 2003.
[6] R.J.Luyken, et al., Solid-State Electronics vol.47, pp. 1199–1203,2003.
[7] T. Schulz, et al. Solid-State Electronics vol.48, pp. 521–527,2004.
[8] J.G. Fossum, et al. Solid-State Electronics vol.48 pp.919–926,2004.
[9] Jin He, et al., IEEE of EDSSC, pp.247-252, Hong Kong. Dec. 2005.
[10] H. C. Pao et al. *Solid-State Electronics*, vol. 9, pp. 927-937, 1966.
[11] J. R. Brews, Solid-*State Electronics*, vol.21, pp.345-352, 1978.