A Unified View of Drain Current Models for Undoped Double-Gate SOI MOSFETs

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ABSTRACT

This paper discusses a compact modeling framework for undoped double-gate (DG) SOI MOSFETs. Drain current classical physics non-regional core models are unified for undoped-body MOSFETs, from bulk to asymmetric and symmetric double-gate device structures. Unification is attained through the use of a mixed formulation of the drain current based on a combination of charge and surface potential. The resulting unified expression describes the behavior inside the silicon body, and does not explicitly contain the front and back flatband voltages, oxide thicknesses, or gate biases. This type of unification, which is valid when the electric field vanishes inside or outside the semiconductor body, may provide useful insight about surface potential-based and charge-based formulations for developing MOSFET core compact models.

***Keywords**:* Asymmetric and Symmetric Dual-gate MOSFET, Undoped body, intrinsic channel, Surface potential, MOS compact modeling, Drain current model.

1 INTRODUCTION

Double-gate MOSFETs are rapidly becoming the most promising candidates for next generation nonclassical CMOS nanodevices. At the same time, there is increasing interest on the independently driven-gate variety of the DG MOSFET [1]. From a phenomenological point of view it would be worthwhile to be able to model both symmetric and asymmetric DG MOSFETs in a unified manner [2]. The model must be formulated in such a generalized manner that it remains valid for different front- and back-oxide thicknesses and for arbitrary front- and back-gate biases. This generalization may be achieved by noting that a given one-dimensional solution of surface potential in the body of the device, for a given voltage along the channel, is valid for a linear combination of front- and back-gate biases and front- and back-oxide thicknesses. The convenience of using either surface potential-based or charge-based formulations for developing MOSFET compact models has received a great deal of attention [3-6]. We will present here a unified classical physics core model for the drain current of symmetric DG, asymmetric DG, and bulk undoped-body MOSFETs, which is based on a mixed formulation consisting of a combination of charge and surface potential. The resulting expression does not explicitly contain the front and back flatband voltages, oxide thicknesses, or gate biases, and therefore it is a description of the behaviour in the silicon body by itself.

2 MIXED DRAIN CURRENT FORMULATION

The drain current of the undoped-body asymmetric DG MOSFET was recently described [7], based on a fully consistent classical physics description in terms of surface potential, assuming that the electric field does not vanish inside the semiconductor body, as

$$\begin{aligned} I_D = \mu \frac{W}{L} \Bigg\{ & \frac{\varepsilon_s t_{Si}}{2}\left(\alpha_0 - \alpha_L\right) \\ & + C_{of}\left[\left(V_{Gf} + 2v_t\right)\left(\psi_{sfL} - \psi_{sf0}\right) - \frac{1}{2}\left(\psi_{sfL}^2 - \psi_{sf0}^2\right)\right] \\ & + C_{ob}\left[\left(V_{Gb} + 2v_t\right)\left(\psi_{sbL} - \psi_{sb0}\right) - \frac{1}{2}\left(\psi_{sbL}^2 - \psi_{sb0}^2\right)\right] \Bigg\} \end{aligned} \quad (1)$$

where μ is the effective electron mobility, W is the channel width, L is the effective channel length, t_{Si} is the semiconductor body thickness, V_{Gf} and V_{Gb} are the front and back gate-to-source voltages with their respective flat-band voltages subtracted, ψ_{sf} and ψ_{sb} are the front and back surface potentials, C_{of} and C_{ob} are the front and back oxide capacitances per unit area, t_{Si} is the silicon thickness, ε_s is the silicon permittivity, $v_t = kT/q = 1/\beta$ is the thermal voltage, and the subscripts “0” and “L” indicate that the variable is evaluated at the “source” and “drain” respectively. α is an interaction factor representing the amount of charge coupling between the front and the back [8,9]. The potentials and α are calculated following the procedure described in [10,11].

We will prove in Section 4 that although (1) was developed assuming that the electric field does not vanish inside the semiconductor body, this equation is also valid even when the electric field vanishes inside the semiconductor body.

In the present section we will transform (1), without introducing additional approximations, into a new equation

which describes the behavior inside the silicon body, and does not explicitly contain the front and back flatband voltages, oxide thicknesses, or gate biases. The mixed boundary conditions at the front and back surfaces are, respectively:

$$+C_{of}\left(V_{Gf}-\psi_{sf}\right) = +\varepsilon_s F_{sf} \equiv Q_{sf} \quad , \tag{2}$$

$$-C_{ob}\left(V_{Gb}-\psi_{sb}\right) = +\varepsilon_s F_{sb} \equiv Q_{sb} \quad , \tag{3}$$

where F_{sf} and F_{sb} are the electric fields at the front and back interfaces, and Q_{sf} and Q_{sb} [12] are defined as the front and back equivalent charges in the silicon that are contained from the respective surface up to the point at which the electric field vanishes. Such point may occur outside the silicon film depending on the charge coupling factor α, which is defined as [7,11]:

$$\alpha \equiv F_{sf}^2 - \frac{2q\, n_i}{\beta\varepsilon_s} e^{\beta(\psi_{sf}-V)} = F_{sb}^2 - \frac{2q\, n_i}{\beta\varepsilon_s} e^{\beta(\psi_{sb}-V)} = -\frac{2q\, n_i}{\beta\varepsilon_s} e^{\beta(\psi_o-V)} \tag{4}$$

where ψ_o is the value of the potential where the electric field vanishes. We observe from (4) that ψ_o is real for negatives values of α, and that ψ_o is imaginary for positive values of α.

The term $C_{of}\left(\psi_{sfL} - \psi_{sf0}\right)$ in (1) may be rewritten using (2) evaluated at source and drain:

$$C_{of}\left(\psi_{sfL} - \psi_{sf0}\right) = C_{of}\left(\psi_{sfL} - \psi_{sf0} + V_{Gf} - V_{Gf}\right) = Q_{sf0} - Q_{sfL} \quad . \tag{5}$$

Analogously, using (3) evaluated at source and drain,

$$C_{ob}\left(\psi_{sbL} - \psi_{sb0}\right) = C_{ob}\left(\psi_{sbL} - \psi_{sb0} + V_{Gb} - V_{Gb}\right) = -Q_{sb0} + Q_{sbL} \quad . \tag{6}$$

The term $C_{of}\left(\psi_{sfL}^2 - \psi_{sf0}^2\right)$ in (1) may be rewritten by using (2) and (5) as

$$C_{of}\left(\psi_{sfL}^2 - \psi_{sf0}^2\right) = C_{of}\left[\left(V_{Gf}-\psi_{sfL}\right)^2 + 2V_{Gf}\psi_{sfL} - \left(V_{Gf}-\psi_{sf0}\right)^2 - 2V_{Gf}\psi_{sf0}\right] = \frac{Q_{sfL}^2}{C_{of}} - \frac{Q_{sf0}^2}{C_{of}} + 2V_{Gf}\left(Q_{sf0}-Q_{sfL}\right) \tag{7}$$

Analogously, at the back,

$$C_{ob}\left(\psi_{sbL}^2 - \psi_{sb0}^2\right) = C_{ob}\left[\left(V_{Gb}-\psi_{sbL}\right)^2 + 2V_{Gb}\psi_{sbL} - \left(V_{Gb}-\psi_{sb0}\right)^2 - 2V_{Gb}\psi_{sb0}\right] = \frac{Q_{sbL}^2}{C_{ob}} - \frac{Q_{sb0}^2}{C_{ob}} + 2V_{Gb}\left(-Q_{sb0}+Q_{sbL}\right) \tag{8}$$

Replacing (5)-(8) into (1) we may express (1) in terms of charge only as:

$$I_D = \mu\frac{W}{L}\left\{ \frac{\varepsilon_s t_{Si}}{2}\left(\alpha_0-\alpha_L\right) + \left[2v_t\left(Q_{sf0}-Q_{sfL}\right) - \frac{1}{2}\left(\frac{Q_{sfL}^2}{C_{of}} - \frac{Q_{sf0}^2}{C_{of}}\right)\right] + \left[2v_t\left(-Q_{sb0}+Q_{sbL}\right) - \frac{1}{2}\left(\frac{Q_{sbL}^2}{C_{ob}} - \frac{Q_{sb0}^2}{C_{ob}}\right)\right]\right\} \quad . \tag{9}$$

We now wish to obtain an expression dependent only on the silicon body. To that end, we further reduce (9) to eliminate C_{of} and C_{ob}.

Using (5), we rewrite at the front:

$$\left(\frac{Q_{sfL}^2}{C_{of}} - \frac{Q_{sf0}^2}{C_{of}}\right) = \frac{1}{C_{of}}\left(Q_{sfL} - Q_{sf0}\right)\left(Q_{sfL} + Q_{sf0}\right) = -\left(\psi_{sfL} - \psi_{sf0}\right)\left(Q_{sfL} + Q_{sf0}\right) \quad . \tag{10}$$

Analogously, at the back:

$$\left(\frac{Q_{sbL}^2}{C_{ob}} - \frac{Q_{sb0}^2}{C_{ob}}\right) = \frac{1}{C_{ob}}\left(Q_{sbL} - Q_{sb0}\right)\left(Q_{sbL} + Q_{sb0}\right) = +\left(\psi_{sbL} - \psi_{sb0}\right)\left(Q_{sbL} + Q_{sb0}\right) \quad . \tag{11}$$

Finally, substituting (10) and (11) into (9) we get a mixed charge and surface potential formulation:

$$I_D = \mu\frac{W}{L}\left\{ \frac{\varepsilon_s t_{Si}}{2}\left(\alpha_0-\alpha_L\right) + \left[2v_t\left(Q_{sf0}-Q_{sfL}\right) + \frac{1}{2}\left(\psi_{sfL} - \psi_{sf0}\right)\left(Q_{sfL}+Q_{sf0}\right)\right] - \left[2v_t\left(Q_{sb0}-Q_{sbL}\right) + \frac{1}{2}\left(\psi_{sbL} - \psi_{sb0}\right)\left(Q_{sbL}+Q_{sb0}\right)\right]\right\} \tag{12}$$

It is evident that the resulting expression for the drain current (12) represents a description which is based on the silicon body alone. Such a characteristic turns out to be very convenient for studying different geometries and different operating conditions. It is important to emphasize that (12) is completely equivalent to potential based (1) and charged based (9).

3 SYMMETRIC DG MOSFET

In a symmetric device, where the front and back flat-band voltages, oxide thicknesses, and gate biases are the same, the electric field vanishes at the midpoint between the front and back surfaces. If we assume a back surface at this midpoint, we may use (12) with the condition $Q_{sb0} = Q_{sbL} = 0$, and taking the new value of t_{Si} as being half of the value that would be used in (12) for an asymmetric device. Doing so we obtain a mixed charge and surface potential current expression for half of the symmetric DG MOSFET:

$$I_D = \mu \frac{W}{L} \left\{ + \frac{\varepsilon_s t_{Si}}{4}(\alpha_0 - \alpha_L) + 2v_t(Q_{sf0} - Q_{sfL}) + \frac{1}{2}(\psi_{sfL} - \psi_{sf0})(Q_{sfL} + Q_{sf0}) \right\} \quad , \quad (13)$$

The above mixed charge and surface potential based drain current equation corresponds to half of the surface potential-based expression for undoped-body symmetric DG MOSFETs, previously published in [13]. A comparable drain current expression has also been published by Taur [14] for these devices.

4 GENERAL ASYMMETRIC DG MOSFET

The current can be expressed as

$$I_D = \mu \frac{W}{L} \int_0^{V_{DS}} Q_I \, dV \quad , \quad (14)$$

where Q_I is the total (integrated in the transverse direction) conduction charge density inside the silicon film at a given location, y, along the channel. Q_I is obtained by Gauss' Law as:

$$Q_I = \varepsilon_S (F_{sf} - F_{sb}) = (Q_{sf} - Q_{sb}) \quad , \quad (15)$$

where Q_{sf} and Q_{sb} are the front and back equivalent charges in the silicon, defined in (2) and (3), that are contained from the surface up to the point x_o at which the electric field would vanish.

Figure 1 illustrates the potential distributions within the body of an undoped asymmetric DG MOSFET with t_{Si} =10nm, at V_{Gf} =2V, for two back-gate voltage values, such that $x_o > t_{Si}$ and $x_o < t_{Si}$.

Substituting (15) into (14), we obtain:

$$I_D = \mu \frac{W}{L} \left(\int_0^{V_{DS}} Q_{sf} \, dV - \int_0^{V_{DS}} Q_{sb} \, dV \right) \quad , \quad (16)$$

Now we recognize that the first term of the above equation represents half of the current of a symmetrical DG MOSFET with a silicon thickness of $2x_o$, that is:

$$\int_0^{V_{DS}} Q_{sf} \, dV = + \frac{\varepsilon_s}{4}(\alpha_0 - \alpha_L)(2x_o) + 2v_t(Q_{sf0} - Q_{sfL}) + \frac{1}{2}(\psi_{sfL} - \psi_{sf0})(Q_{sfL} + Q_{sf0}) \quad , \quad (17)$$

For the particular case of an asymmetrical device in which the electric field does not vanish in the semiconductor, the point x_o is larger than t_{SI} (see Fig. 1). On the other hand, the second term of (16) represents half of the current of a symmetrical DG MOSFET extending from the back surface to x_o. Therefore, it has a silicon thickness of $2(x_o - t_{SI})$ and the integral becomes:

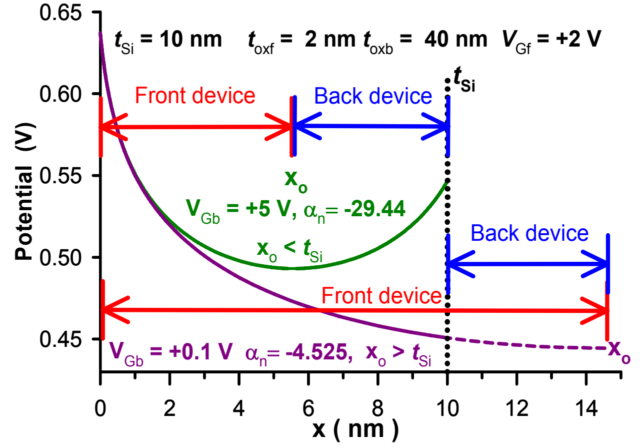

Fig. 1. Potential distributions within the body of a 10nm thick undoped asymmetric DG MOSFET, at given front-gate voltage and two back-gate voltages, showing the occurrence of the field vanishing point inside and outside the semiconductor body.

$$\int_0^{V_{DS}} Q_{sb} \, dV = + \frac{\varepsilon_s}{4}(\alpha_0 - \alpha_L)\left[2(x_o - t_{SI})\right] + 2v_t(Q_{sb0} - Q_{sbL}) + \frac{1}{2}(\psi_{sbL} - \psi_{sb0})(Q_{sbL} + Q_{sb0}) \quad (18)$$

Substituting (17) and (18) into (16) we obtain Eq. (12).

Therefore we have obtained an expression for the current of the asymmetric device from the solution for the symmetric device. Equations (1), (9) and (12) are valid even when the electric field does vanish inside the semiconductor body, in fact, they are valid for all gate bias conditions.

Figure 2 presents the normalized output characteristics of an asymmetric DG MOSFET as a function of drain voltage for a fixed front-gate voltage and various back-gate voltages, as calculated from numerical integration of the charge and from the present analytical expression.

Figure 3 compares calculated and Atlas simulated normalized front-gate transfer characteristics of the same asymmetric DG MOSFET, for low drain voltage and four back gate voltages.

5 DISCUSSION

In a conventional bulk MOSFET, the surface potential, ψ_s, is obtained from the simultaneous solution of the two following equations:

$$V_G = \psi_s + \frac{\varepsilon_s F_s}{C_o} \quad , \quad (19)$$

$$F_s^2 - G^2(\psi_s) = 0 \quad , \quad (20)$$

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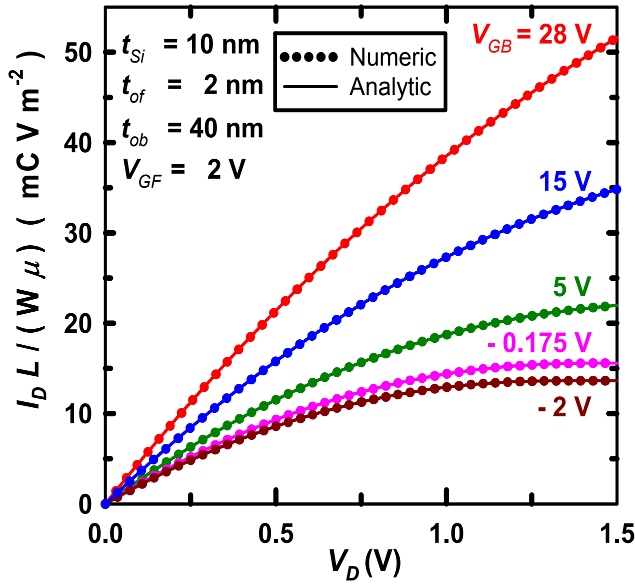

Fig. 2. Comparison of analytic and numerically calculated normalized drain current of undoped asymmetric DG MOSFET as a function of drain voltage for several back gate biases.

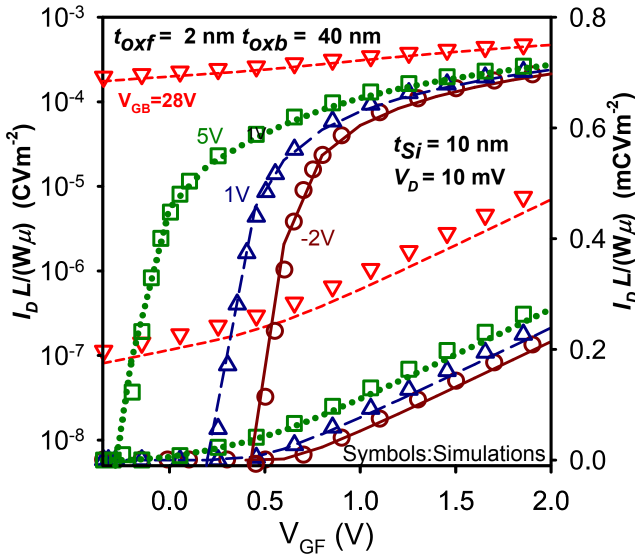

Fig. 3. Normalized drain current of asymmetric DG MOSFET as a function of front gate voltage for four back gate voltages. Lines: calculated; Symbols: simulated with Atlas.

where V_G is the gate-to-source voltage with its flat-band voltage subtracted, C_o is the oxide capacitance per unit area, F_s is the surface electric field, and $G^2(\psi_s)$ is the Kingston function [8].

After a value of ψ_s is obtained, the complete potential versus distance can be calculated by:

$$x = \int_{\psi}^{\psi_s} \frac{d\psi}{F} \quad . \tag{21}$$

where $F = \sqrt{G^2(\psi)}$ is the electric field and ψ is the potential at any arbitrary distance x.

For a known value of ψ_s, a value of F_s is defined by (20), and we observe from (19) that this particular solution is valid for several pairs of values of V_G and C_o.

Replacing $C_o = \frac{\varepsilon_{ox}}{t_{ox}}$ in (19), we obtain:

$$V_G = \psi_s + \frac{\varepsilon_s F_s}{\varepsilon_{ox}} t_{ox} \quad , \tag{22}$$

which implies that this particular solution is valid for a linear combination of gate biases and oxide thicknesses.

The generalization of this idea for the asymmetric DG MOSFET is analogous to the bulk device. The general solution for the asymmetric DG MOSFET has been recently described [11] for all possible bias conditions. After values of the front surface potential, ψ_{sf}, and the charge coupling variable, α, are obtained from the general solution, a value of front surface electric field, F_{sf}, is defined by

$$F_{sf}^2 - G^2(\psi_{sf}) = \alpha \quad . \tag{23}$$

Using the boundary condition in the front surface we find that this particular solution is valid for a linear combination of front gate biases, V_{Gf}, and front oxide thicknesses, t_{oxf}:

$$V_{Gf} = \psi_{sf} + \frac{\varepsilon_s F_{sf}}{\varepsilon_{ox}} t_{oxf} \quad . \tag{24}$$

Knowing ψ_{sf} and α, the complete potential versus distance can be calculated by:

$$x = \int_{\psi}^{\psi_{sf}} \frac{d\psi}{F} \quad . \tag{25}$$

where $F = \sqrt{\alpha + G^2(\psi)}$ is the electric field and ψ is the potential at any arbitrary distance x.

The value of ψ_{sb} can be obtained from the evaluation of (25) at x= t_{Si}. The back surface electric field, F_{sb}, is defined by

$$F_{sb}^2 - G^2(\psi_{sb}) = \alpha \quad . \tag{26}$$

Using the boundary condition in the back surface we find that this particular solution is valid for a linear combination of back gate biases, V_{Gb}, and front oxide thicknesses, t_{oxb}:

$$V_{Gb} = \psi_{sb} - \frac{\varepsilon_s F_{sb}}{\varepsilon_{ox}} t_{oxb} \quad . \tag{27}$$

Now we will study the importance of each term of the drain current equation in (12). We rewrite (12) as:

$$\boxed{I_D = \mu \frac{W}{L} \left\{ C_\alpha + C_f + C_b \right\}} \quad , \tag{28}$$

where $$C_\alpha = \frac{\varepsilon_s t_{Si}}{2}(\alpha_0 - \alpha_L) \quad , \quad (29)$$

$$C_f = \left[2v_t\left(Q_{sf0} - Q_{sfL}\right) + \frac{1}{2}\left(\psi_{sfL} - \psi_{sf0}\right)\left(Q_{sfL} + Q_{sf0}\right)\right] \quad , \quad (30)$$

$$C_b = -\left[2v_t\left(Q_{sb0} - Q_{sbL}\right) + \frac{1}{2}\left(\psi_{sbL} - \psi_{sb0}\right)\left(Q_{sbL} + Q_{sb0}\right)\right] . \quad (31)$$

Figure 4 shows the normalized drain current and its components of the asymmetric DG MOSFET, as a function of back gate voltage, for a drain voltage of 10mV and 1.5V. We observe that C_b is negative for values of V_{Gb} corresponding to the condition $x_o > t_{Si}$ and that C_b is positive for $x_o < t_{Si}$. These two conditions were illustrated in Fig. 1. C_f is insensitive to V_{Gb} because V_{Gf} is above threshold.

We find that $C_b = C_f$ for a value of V_{Gb} which depends on V_D. At this point, the device behaves as a symmetric device. This figure and additional calculations reveal that C_α is negligible.

Figure 5 presents the behavior of the normalized drain current back side component, C_b, for the asymmetric DG MOSFET, as a function of back gate voltage, for six values of drain voltage.

Figure 6 illustrates the analytical solutions of the potential within the semiconductor body, for negative and positive α_n, for an asymmetric DG MOSFET with a front-gate voltage of 2 V and various back gate voltages. The case of V_{Gb}= 28V and α_n =-36.08 is illustrated because it corresponds to the case in which the front and back gates cause the same level of band-bending at both surfaces of the semiconductor.

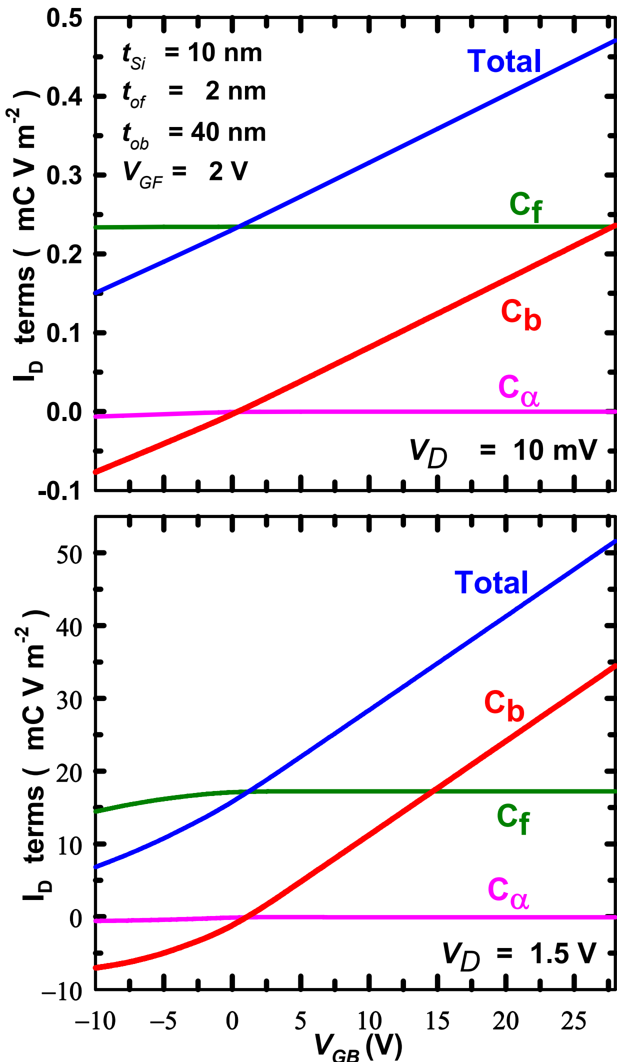

Fig. 4. Asymmetric DG MOSFET normalized drain current and its components, as a function of back gate voltage, for two values of drain voltage.

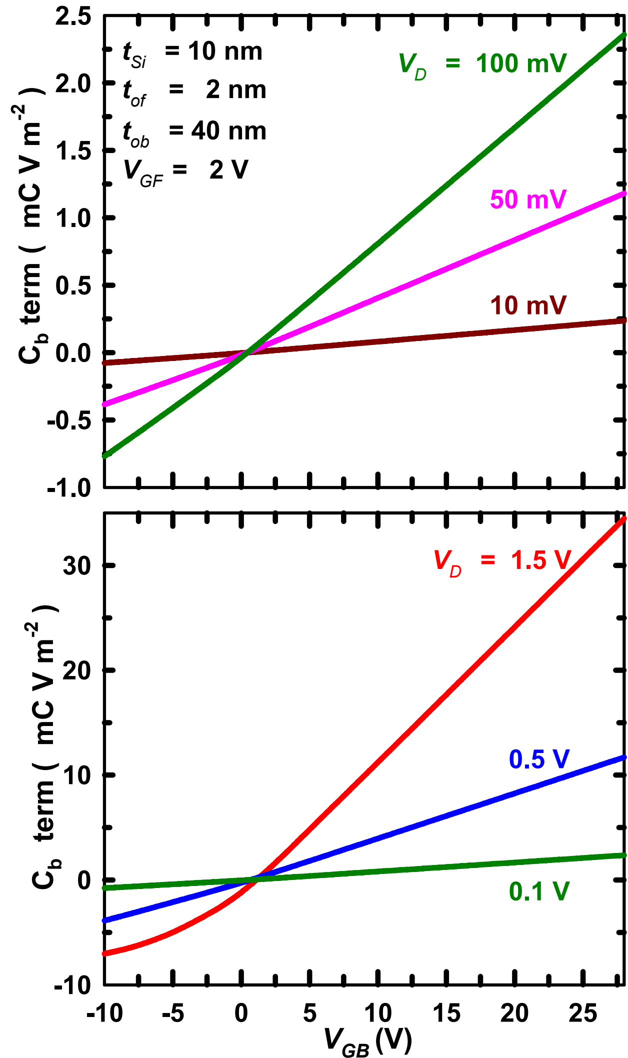

Fig.5. Back side component of the normalized drain current, as a function of back gate voltage, for six values of drain voltage.

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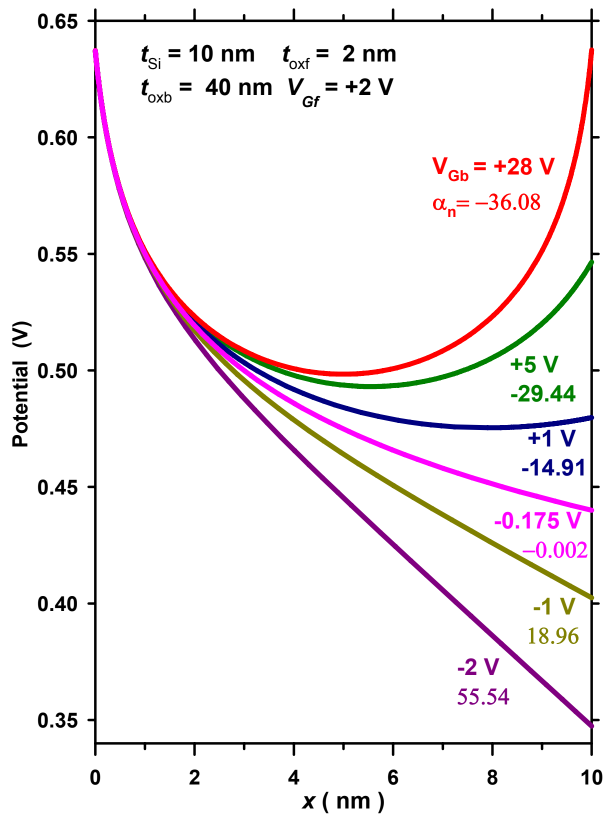

Fig. 6 Potential distribution in the semiconductor body of undoped asymmetric DG MOSFET for a given front-gate voltage and various back-gate voltages. The resulting negative and positive values of α_n are also indicated in each case.

5 CONCLUSIONS

We have presented a unified classical physics drain current core model for undoped-body symmetric and asymmetric DG MOSFETs. The model was built by using a mixed formulation of the drain current consisting on a combination of charge and surface potential descriptions. The front and back flatband voltages, oxide thicknesses, and gate biases are absent from the resulting expression, which means that it describes the behaviour of the silicon body by itself. This unification may contribute useful insight to the discussion about the convenience of using either surface potential-based or charge-based formulations for developing MOSFET core compact models.

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