A Versatile Multi-gate MOSFET Compact Model: BSIM-MG

(Invited Paper)

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ABSTRACT

BSIM-MG is a surface-potential based compact model for multi-gate MOSFETs such as FinFETs fabricated on either SOI or bulk substrates. It can model transistors with the gate controlling two, three, or four sides of the fin. The effects of body doping are modeled. It can also model a double-gate transistor with independently biased top and bottom gates and asymmetric top and bottom gate work-functions and dielectric thicknesses. It supports high performance metal-gate technologies as well low-cost polysilicon-gate memory technologies.

Keywords: compact model, BSIM, FinFET, double gate, trigate.

1 INTRODUCTION

Reducing device size is largely responsible for the rapid reduction of IC cost. With each new node of size shrinking, the gate must have greater electrostatic control over the channel than the previous node. As the scaling of gate dielectric thickness eventually slows down, multiple-gate CMOS structures such as FinFET [1] are expected to take up the slack. It is thus necessary to develop a compact model of multi-gate MOSFETs for technology/circuit development in the short term and for product design in the longer term. One challenge for multi-gate compact model development is to support several flavors of multi-gate transistors. Another is to model the effects of finite body doping since multiple-Vt technology will likely require doping the body to a significant concentration.

2 THE MODULAR APPROACH

The versatility of the model is achieved without sacrificing its computational efficiency. One technique used is to introduce two modules—a common-gate module and an asymmetric/independent-gate module. "Common-gate" means that there is only one electrically interconnected gate (one gate voltage) whether the device structure is a double, triple, or quadruple gate structure. The common-gate module assumes that the gate work-functions and the dielectric thickness on the two, three, or four active sides of the fin are the same. The carrier mobility on the vertical and horizontal channels may be different because of the different crystal orientations and/or strain.

The asymmetric/independent-gate module allows the top and bottom gate work-functions and dielectrics to be different. It assumes that the two gates have different voltages in general. The bottom gate can be used, for example, to adjust the threshold voltage of the top channel.

3 THE CORE MODEL

The core model is a double-gate (DG) model. Current analytical DG-MOSFET model only address transistors with undoped body [2,3,4]. We have developed a surface-potential-based core model for a DG-MOSFET with doped body. The Poisson's equation with inversion carrier is perturbed by the body doping and a modification to the surface potential is derived.

The analytical surface potential agrees well with TCAD double-gate device simulation for different doping concentration of the fin without any fitting parameters (**Fig. 1**).

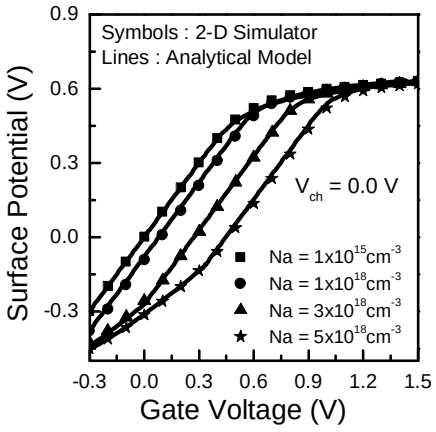

Fig. 1 Surface potential model agrees with TCAD simulation results well without any fitting parameters in both partially depleted and fully depleted regimes and for both lightly doped and heavily doped DG-MOSFETs.

Drift-diffusion equation [5] is then employed to obtain the drain current in terms of the surface potentials at the source and the drain:

$$I_d = \frac{2\mu WC_{ox}}{L}\left(V_g - V_{fb} - \frac{\psi_{ss}+\psi_{sd}}{2} - \frac{qN_A t_{Si}}{2C_{ox}} + \frac{kT}{q}\right)(\psi_{sd} - \psi_{ss})$$

The I-V core model predicts drain current accurately in all regimes of operation over a wide range of body doping without any fitting parameters (**Fig. 2**). Volume inversion is correctly modeled in the solution of the Poisson's equation and the I-V formulation (**Fig. 3**).

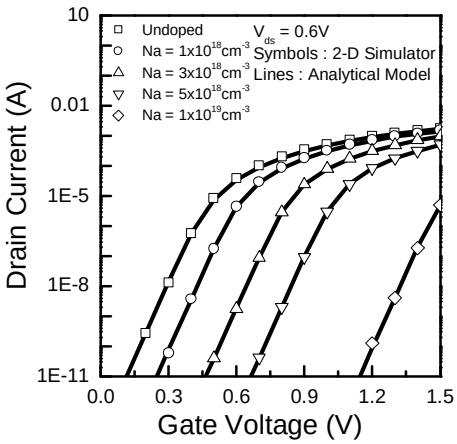

Fig. 2 I-V model predicts drain current for varying body doping, N_A. Model agrees with 2-D device simulation results without fitting parameters.

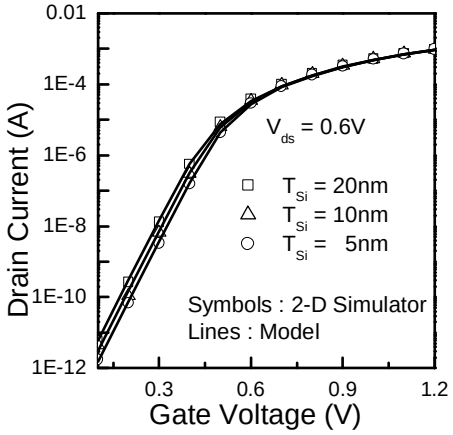

Fig. 3 I-V model accurately predicts drain current for different body thickness, *Tsi*. Volume inversion is captured---the subthreshold current is proportional to the body thickness.

The capacitance model has also been developed. The transcapacitances from the C-V model matches 2-D simulation results well (**Fig. 4**). The equality of C_{gs} and C_{gd} at V_{ds}=0 demonstrates the symmetry of the model. Furthermore, a separate core model has been developed for asymmetric/independent-gate MOSFETs. It also has excellent accuracy (**Fig. 5**). The threshold voltage tuning by the back gate bias is accurately predicted by the model.

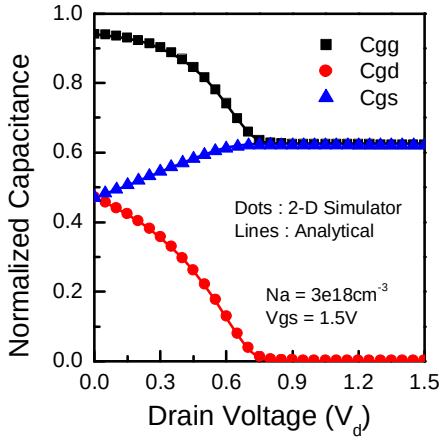

Fig. 4 All the transcapcitance match 2-D simulation results very well without fitting parameters. C_{gs} = C_{gd} at V_d=0 indicates that the model os symmetric.

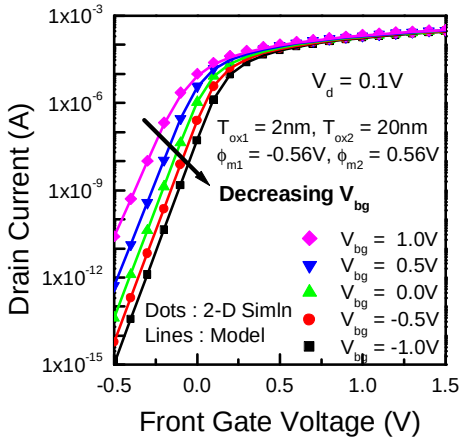

Fig. 5 I_d-V_g characteristics of independent-gate DG-MOSFET biased at different back gate voltages. The threshold voltage tuning with the back gate bias is accurately predicted by the model.

4 THE COMPLETE MODEL

The core model is only the beginning of any compact model. BSIM-MG, in the tradition of BSIM3 and BSIM4, models numerous physical phenomena that are expected to be important to the accurate representation of advanced multi-gate MOSFET technologies. In addition to velocity saturation, it also models velocity overshoot as well as source injection velocity effects on the saturation current. Short channel effects (SCE), such as drain-induced barrier lowering, V_{th} roll-off and subthreshold-slope degradation are modeled. So are the effects of drain coupling and channel length modulation on the output conductance in the saturation region. Gate leakage is of course also modeled as are the quantum mechanical effects on current and capacitance.

BSIM-MG even models the polysilicon-gate depletion effect. Although high-performance multi-gate MOSFETs will surely employ metal gate technologies, low-cost memories may use polysilicon gated FinFETs to enable continued cell size reduction. BSIM-MG also supports FinFETs fabricated on SOI and those fabricated on bulk substrates.

As an example of these physical-effects models, the short-channel effect model is briefly described here. In our model, the minimum barrier potential for the leakage path along the channel is derived as the basis for modeling drain-induced barrier lowering, V_{th} roll-off and subthreshold slope degradation. 2-D Poisson's equation of potential is solved across the thickness of the body [6,7]. A lower gate voltage is needed to obtain the same threshold barrier potential for a short channel device than the core model thus necessitating a V_g modification term. Subthreshold-slope degradation is automatically captured since the V_g modification is a function of the gate voltage. The SCE model matches the TCAD simulation results well (**Fig. 6**). Note that no fitting parameter is used.

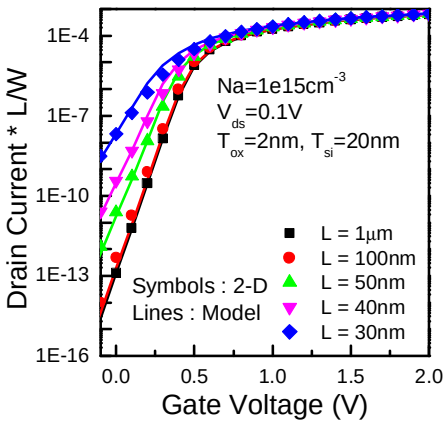

Fig. 6 I_d-V_g characteristics of common-gate DG-MOSFET for different channel length. V_{th} roll-off and subthreshold slope degradation are simultaneously captured by the model.

Furthermore the stronger electrostatic control provided by the "third" and the "fourth" gates is modeled and implemented in BSIM-MG.

5 CONCLUSION

BSIM-MG is a versatile multi-gate MOSFET compact model. It is surface-potential based with smooth and symmetric behaviors. Its accuracy has been proven with experimental data of triple-gate FinFETs fabricated on SOI and bulk substrates [8].

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