A History of Electronic Traps on Silicon Surfaces and Interfaces

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Abstract
A review of the electronic or electron and hole traps at Si/SiO2 interfaces of MOS capacitances and transistors is given. They are increasingly affecting the electrical signal properties of silicon capacitances and transistors as the technologies for digital, analog and memory applications advance. This review covers the 60-year history from the first quantitative study of barrier heights on 'bare' silicon surface in the form of Bethe (viz. Schottky) metal/Si surface barrier diodes in 1946 by Meyerhoff to the latest applications of a most sensitive monitoring method of interface traps (base terminal interface recombination current) for the endurance of memory transistors and operation life of logic and analog transistors. Historical experiments are described, all seemed to point to a broad energy-level distribution of the interface traps at the SiO2/Si interface with a U-shaped density of bound quantum states or energy levels, rather than single or few energy levels. Such a energy distribution of the energy levels of interface traps is not inconsistent with the expectation from an extension of Slater’s 1950 theory of bound electron state from the perturbation of a bulk impurity ion to a crystalline periodic potential, which extension was described by Sah for the perturbations from the random distribution of bond length and angle of the Si:Si and Si:O bonds at the SiO2/Si interfaces in recent MOS capacitances and transistors.

Keywords: interface traps, surface states, MOSFET, MOST, compact model, device physics, semiconductor history

1. Introduction
Interface properties in the basewell-channel region of the Metal-Oxide-Semiconductor Transistor (MOST) have limited its electrical performance via the random collisions (scattering and trapping) experienced by the electrons and holes. {See chapter 3 on p231-p310 of [1].} Electron and hole drift mobilities are lowered from the phonon (lattice-vibration) scattering-limited values due to random collisions at the transistor terminals. These additional currents have limited several transistor performance characteristics, which have recently become increasingly important, such as low stand-by dissipation-power, long operating-lifetime, low-noise amplification, and long-endurance memory [2]. The technological importance of oxidized crystalline silicon has prompted extensive research to characterize the interfacial electronic traps at the SiO2/Si interface and to delineate their microscopic origin [2-8]. Nevertheless, the microscopic origins of the interface traps at the SiO2/Si interface, even their electronic properties, have not been firmly established.

2. Motivations
The leakage current component in the basewell-channel terminal of the MOS transistor from carrier generation-recombination-trapping at interface traps, \( I_{GR} \), affects several operations of the MOS circuits. To quantify these, let us consider a single-energy-level electron trap located at the SiO2/Si interface of a MOS transistor. It is characterized by six fundamental parameters: the energy level position in the silicon energy gap \( E_T \) and the capture and emission rate coefficients of electrons and holes at the interface, \( c_m \) and \( c_p \) in the unit of cm\(^{-3}\cdot sec^{-1} \), and \( e_m \) and \( e_p \) in the unit of sec\(^{-1} \). Let the instantaneous trapped electron density be

\[
n_{iT}(r,t) = N_{iT}(r) + n_{iT}(r,t) \, \text{cm}^{-2}.
\]  

\{(See Appendix A, Notation Convention, on pp. 992-996 of [1] for detailed definitions and explanations.) \( N_{iT}(r) \) is the DC steady-state areal density of trapped electrons. \( n_{iT}(r,t) \) is the time-dependent part of the trapped electron density, usually much smaller than the DC steady-state value, \( n_{iT}(r,t) \leq N_{iT}(r,t) \). \( r \) is the vector defining the SiO2/Si interfacial plane. As shown in Fig.1, it reduces to the 2-dimensional vector on the interface boundary \( r=r(x=0,y,z)=s(y,z) \) of a planar SiO2/Si interface located at the \( x=0 \) plane.

MOS circuit operation properties, as affected by the presence of electron-hole traps at the SiO2/Si interface of the MOS transistors can be estimated as follows: (i) Average or DC standby power dissipation is specified by the base terminal leakage current; the portion related to the interface traps is given by \( I_B=I_{GR} \cdot (e_m e_p)^{1/2} N_{iT} \); (ii) Operation lifetime of the MOS transistor in logic and analog MOS circuits is specified by the MOS transistor gate threshold voltage shift of about 1mV which is given by \( \Delta V_{TH}=q n_{iT}(r,t)/C_{ox} \sim 1\,\text{mV} \) where \( C_{ox} \) is the specific capacity (F/cm\(^2\)) of the gate dielectric \( C_{ox} = \varepsilon_{ox}/X_{ox} \), and \( \varepsilon_{ox} \) is the permittivity and \( X_{ox} \) is the electrical thickness of the gate dielectrics; (iii) Endurance of the nonvolatile MOS memory circuits (program and data flash memory chips) using memory MOS transistor (floating polycrystalline silicon gate and nitrided, SONOS, and other charge-
storage-dielectric gate [9, 10, 11]) is also specified by the MOS transistor gate threshold voltage shift, at much higher magnitudes, about 1V, given by \( \Delta V_{GBth} \propto q n_t(r,t)/C_{ox} \sim 1\text{V} \), under much higher electrical stress during the write-program and erase operations than the logic switching and analog amplification; and (iv) RF and HF noise [12-23] from trapping and tunneling to interface and oxide traps with the multi-component or multi-time-constant GRT (Generation-Recombination-Trapping) \( 1/(1+\omega^2 \tau^2) \) [13] and \( 1/f \) [12, 22] noise spectra, is specified by a noise equivalent input voltage per unit bandwidth of about \( 1\mu\text{V} \cdot \text{Hz}^{1/2} \) from random emission and capture or trapping of electrons and holes at the interface traps and band-trap and trap-trap tunneling transitions given by a gate equivalent input noise voltage of \( V_{in} \propto q n_t(r,t)/C_{ox} \sim 1\mu\text{V} \) and a characteristics noise frequency of \( \omega_{in} = \tau^{-1} = (c_m N_S + e_m + c_p P_S + e_p)P_{TT} < 1\text{Hz} \) to \( > 10^{12}\text{Hz} \), where \( P_{TT} \) is the transition probability rate, an exponential attenuation factor, from electron and hole trap-band tunneling transitions between the near-interface oxide traps and the conduction and valence band states, or the less likely trap-trap tunneling transitions between a near-interface trap and an at-the-interface trap. {See sections 363n on pp. 286 to 289 and Fig. 36n0 and 35n4 on pp. 288-289 of [1] for the many possible tunneling transitions between band and trap, and trap and trap states.}

2. History of Electronic Traps on SiO\(_2\)/Si Interface

Historical evidences of interface traps on Si/material interfaces are briefly reviewed in this section. In 1946, Meyerhof [24] observed metal-independent Schottky barrier heights in many metal-semiconductor contacts. In 1947, Bardeen [25] presented two models of distribution in energy of interface trap energy-levels, a symmetrical 2-level pair and a U-shaped, to account for Meyerhof’s results. Bardeen’s theory qualitatively [25] showed that the pinning or locking of the Fermi level to the neutral Fermi level position is due to the high density of neutral electron and hole traps at the metal/Si interface.

The two Bardeen surface state models of interface traps were quantitatively proven and demonstrated by Sah in 1964 [26] with many computed MOSCV curves (metal/oxide/silicon capacitance-voltage curves). Two are shown, in Figs. 1(a) and 1(b), for the two Bardeen models: Fig. 1(a) for two interface traps located on each side of the midgap, and Fig. 1(b) for a U-shaped interface traps. Figure 1(b) shows the stretch-out of gate voltage around the neutral Fermi level, \( E_{FN} \).

A distinct experimental evidence of Fermi-level pinning was given by Sah in 1976 using a thermal-grown integrated circuit SiO\(_2\)/Si interface, which was further heated in pure Argon at 1100C to generate a high density of interface trap near the band edges. The CV curves of the nMOSC (C=capacitor, \( n\)= on n-type Si) are shown in Fig. 2. They came from Fig. 2 of [4].

Figure 1 LFCV of (a) two-level interface trap and (b) U-shape interface trap. From p.59 and p.61 of [26].

Figure 2. The 77K and 300K CV curves of two MOS capacitors, 2H2 and 2L2, with 1100C 2000A dry oxide heated in pure Argon at 1100C; 2H2 was then heated at 450C in wet Argon for 30 seconds. The 1974-vintage trivalent Si· reaction equation with OH· for 2H2 is to be added Si· + H· \( \rightarrow \) Si·H. From Fig. 2 of [4].
The cross sectional view, the atomic fraction of oxygen, $\text{SiO}_x$, in the oxygen deficient 1100°C-Ar heated 2000 Å oxide, and the one-electron energy band diagram and density of bound electronic states at the $\text{SiO}_2$/Si interface. In addition to the perturbation of electronic states by trivalent silicon’s or silicon dangling bonds $\text{Si}^+$, there are substantial perturbations from the random variations of $\text{Si}:\text{Si}$ and $\text{Si}:\text{O}$ bond lengths and angles at the interface. From Fig. 5 of [4].

These 1-MHz CV curves were taken on two MOS capacitors, 2H2 and 2L2, with 1100°C 2000 Å dry oxide and post-oxidation exposure to pure Argon at 1100°C. 2H2 is further heated in wet Argon at 450°C for 30 second. The 2H2 CV curve is very sharp at 300K and has invisible CV distortion (in this contracted gate-voltage scale) between its 77K and 300K CV curves, indicative of very low interface trap density. The 2L2 shows visible sloping of the 300K CV (compared with the sharp CV of 2H2), indicative of a high concentration of U-shaped interface traps, with the neutral Fermi-level position below the midgap indicated by intersection of the CV of the low-interface-trap 2H2 with that of 2L2 at about $C_V=70\text{pF}$. The 2L2 CV is broadened to a huge-huge (~200V) gate-voltage ledge at 77K, due to the very high concentration of interface traps near the silicon conduction band edge. The microscopic model was that the 1100C-heating in the pure and dry Argon from liquid-Argon source created a high density of oxygen-deficient or silicon-rich interfacial layer, $\text{SiO}_x$ ($x<2$) at the $\text{SiO}_2$/Si interface with very high density of trivalent silicon dangling bonds $\text{Si}^+$ dangling bonds and associated random variations of $\text{Si}:\text{Si}$ and $\text{Si}:\text{O}$ bond angles and lengths. These are tremendous perturbations to the possibly otherwise ideal $\text{SiO}_2$/Si interface with perfect-lattice-match between the crystalline $\text{SiO}_2$ and crystalline Si. A picture was given in 1976 [4], which is shown as Fig. 3.

There were also indirect experimental evidences, again from diode and transistor electrical measurements, on the nature and properties of the $\text{SiO}_2$/Si interface traps. The earliest was perhaps the 1948 Shockley-Pearson experiment seeking conductivity modulation on a thin semiconductor film, in search of a solid-state amplifier to replace the vacuum tube [27], as shown in Figure 4. They attributed their null results to high density of surface states that pin the Fermi level in accordance with Bardeen’s theory [25].

Two later transistor studies showed uncertainties of the extracted parameters of the recombination centers or interface traps from the dc current-voltage characteristics of mesa-etched [28] and thermal-oxide protected planar [29, 30] high-temperature diffused Si p/n junctions. The 1957-Sah-Noyce-Shockley study [28] extracted the energy level and the electron and hole capture rate ratio ($E_T$, $c_n/c_p$) of recombination centers (or traps), assumed to be in the bulk space-charge layer of the p/n junction, by fitting the theory to the experimental forward and reverse current-voltage (I-V or IV) data at three voltage-current points ($±0.1\text{V}$ and $10^{-4}\text{A}$). A typical I-V curve is shown in Fig. 5 which shows the three fit points.

On many diodes fabricated on the same silicon wafer and on different wafers at different fabrication conditions (diffusion temperature and time, and different chemical etches conditions to give the p/n junction mesa diodes), they found nearly equal extracted electron-hole capture rate ratio $c_n/c_p$, close to unity. The individual $c_n$ and $c_p$ values...
were not determined due to imprecise p/n junction area measured and electron-hole diffusivities, and unknown concentration of the recombination centers. They also found that the trap energy levels were always over a small energy range about the silicon midgap. The extracted \( c_0/c_p \) and \( E_T \) values were also not unique, depending on the three I-V matching points selected. Furthermore, they recognized that the trap energies extracted by matching the experiment with the theory were effective values that included valley-orbit and spin-orbit degeneracies, as well as excited states; hence, they were not true discrete-single quantum energy levels or binding energies of the trapped electron or hole.

In the second studies, performed in 1961, using silicon p/n junction diodes with MOS-gate over the oxide-protected surface of the p/n junction fabricated by newer technologies and materials [29, 30], bell-shaped peaks in the base terminal current, \( I_B \), versus the gate voltage, \( V_{GE} \) and \( V_{GB} \), were observed. These bell shaped \( I_B-V_{GE} \) and \( I_B-V_{GB} \), were the historical first’s which led to extensive application recently as the Recombination-Direct-Current-Voltage (R-DCIV) diagnosis methodology [31, 32].

The single peak in Fig. 6 and the double peak in Fig. 7, immediately led to the suggestion in 1961-1962 [29, 30] of the presence of discrete energy-level interface traps. Our recent theoretical understanding, 45 years later, suggested that these could be from a U-shaped distribution of interface traps, and the two peaks could come from the same interface trap species at two interface locations in the transistor with two different dopant impurity concentrations.
Another evidence showing the working of the Bardeen surface states on SiO$_2$/Si interface was the Fermi level pinning after the MOS capacitor is exposed to a high dose of radiation which generates a high concentration of interface traps. Figure 8 shows the MOSCV curves taken at each increasing fluence of 1MeV electrons, on a pMOS Capacitor with an n+ source to supply the minority carriers (electrons) when the p-Si surface is inverted at positive and high gate voltage. The flat capacitance minimum at the final and highest exposure, $\Phi = 4.5 \times 10^{15}$ e/cm$^2$, is the evidence of a high concentration of interface traps generated by the 1MeV electrons. Bulk traps are also generated by the 1MeV electrons in the p-Si underneath the aluminum-gated oxide, but it could not distort the CV curves that much.

On the nature of the SiO$_2$/Si interface traps, a fundamental study was made by Nishi in 1971 [35] using the EPR (Electron Paramagnetic or Spin Resonance) technique on very large area MOS capacitors (~1 cm$^2$). The EPR signals were interpreted by discrete SiO$_2$/Si interface trap energy levels. Areas of modern MOS transistors are much smaller (~1 mm$^2$ or $10^{-8}$ smaller than Nishi’s samples of ~1 cm$^2$). Thus, the interface quality and the interface traps should be very different. Statistically random spatial trap locations or fluctuation of the local concentration of the traps could also play a role. For example, in a MOS transistor with 250nm channel length and width, there are only 60 interface traps at 10$^{14}$ cm$^{-2}$, and only 6000 traps at 10$^{15}$ cm$^{-2}$, the latter is already about 10% of the Si:Si and Si:O bond densities of ~5 $\times$ 10$^{14}$ cm$^{-2}$ [6, 8], so not much higher to maintain some cohesion, otherwise the oxide film would peel off. Thus, it is impossible to observe the EPR signal on transistors since EPR needs 10$^{13}$-10$^{14}$ spins from unpaired trapped electrons which needs about one-square-centimeter of SiO$_2$/Si area.

3. Slater’s Theory Applied to SiO$_2$/Si Interface

Slater in his 1951 Massachusetts Institute of Technology (MIT) Radiation Laboratory Report and MIT Lecture handout [36] described the finite difference solutions of a periodic potential problem with a localized perturbation due to the presence of point-charge impurity atom. A positively charged n-type impurity atom (such as the net-singly positive-charged group-5 shallow-level phosphorus donor, D$^-$=P$^5$-Si$^{4+}$, or the net-doubly positive-charged group-6 deep-level sulfur double donor, D$^{2+}$=S$^{6-}$Si$^{4+}$) would give a negative-electron-energy perturbation and one-electron (or two-electron) bound electron state which is localized at the donor impurity site, by shifting downwards (negative) in energy a conduction band state into the semiconductor energy gap. Similarly, a negatively charged p-type impurity atom (such as the net-singly negative-charged group-3 shallow-level boron-acceptor, A$^+$=B$^{3-}$Si$^{4+}$, or the net-doubly negative-charged group-2 deep-level zinc-acceptor, A$^{2+}$=Zn$^{2-}$Si$^{4+}$) would give a positive-electron-energy (or negative-hole energy) perturbation, and one-hole (or two-hole) bound hole state which is localized at the acceptor impurity site, by shifting a valence band state upwards (positive) in energy into the semiconductor energy gap. These were graphically illustrated by Slater, and are shown in Figs. 9(a)-9(b).

Slater’s historical-first perturbed periodic potential diagrams, copied to Fig. 9, were not in constant scale due to a number of draftsman errors or Slater’s trade-mark copyright-infringement-protection inserts. (i) The long range Coulombic perturbation potential curves should be identical in the conduction and valence band for the donor in Fig. 9(A2-2), and the acceptor in Fig. 9(A2-3). (ii) The lattice distortion due to the core-charges difference between the impurity (+5 donor such as Phosphorus and +3 acceptor such as Boron) and the host (+4 Silicon) are reversed. It should have a local lattice expansion for the +5 donor (more repulsive force between P$^5$ and Si$^{4+}$ than Si$^{4+}$ and Si$^{4+}$) and local lattice contraction for the +3 acceptor (less repulsive force between B$^3$ and Si$^{4+}$ than Si$^{4+}$ and Si$^{4+}$). (iii) The Coulombic perturbation potentials were drawn for a solid with much lower dielectric constant and much heavier semiconductor effective mass of the electrons or holes than those of silicon, with a ratio of the Bohr or ground electronic bound state radius to lattice constant of $a_{\text{cm}}/a_{\text{lat}}$ of 6 = 0.5929(m$^2$/m$^3$)($\varepsilon_{\text{Si}}/\varepsilon_{\text{lat}}$)/$a_{\text{lat}}$ = 0.5929(0.443)(11.7)/2.35 = 14/2.35 = 5.95±6 using spherical energy band model [See Figs. 222.1 and 222.2 on p.164 and calculation on p.166, and problem P223.4 on p.223 of [1].}

With the above scaling nonlinearity considered, we simplified Slater’s microscopic diagram to macroscopic dimension in order to squeeze into the 3-inch wide column of this text an illustration of the perturbation of the periodic potential by the imperfections at the SiO$_2$/Si interface. This is shown in Figs. 10(a), 10(b) and 10(c) at the MOS flat-band condition.

Figure 8. The 1MHz MOSCV on p-Si with n+Source taken in-situ during 1MeV electron irradiation. The wide (~50V) flattened bottom indicate the generation of high concentrations of interface states on SiO$_2$/Si interface was the Fermi level pinning after the MOS capacitor is exposed to a high dose of radiation which generates a high concentration of interface traps. Area=5346cm$^2$, Oxide thickness=6000Å, p-Si=5 $\times$ 10$^{13}$Boron/cm$^3$. From Fig.2 of 1973-Walker-Sah [34].
Figures 9 Electronic energy diagrams of band and bound states. The periodic potential of the host ions is shown in these two microscopic diagrams. (a) Single positively charged donor impurity ion giving rise to an electron bound state. (b) Single negatively charged acceptor impurity ion giving rise to a hole bound state. From Slater’s Figs. A2-2 and A2-3 on page 293 of [36].

Figure 10. SiO₂/Si interfacial one-electron energy band diagrams containing localized perturbation: (a) positive perturbation potential Δ>0; (b) negative perturbation potential Δ<0; and (c) energy distributed perturbations of Δ>0 and Δ<0, giving U-shaped density of states (DOS).

First, the periodic potential is not shown. (See the not-omitted periodic potential of the Vacuum/Si interface shown Fig. 172.1 (c) on p.98 and Fig. 180.1 on p. 109, and its omission in Fig.172.2 on p.100, all of [1].) Second, the perturbation that give the interface electronic (i.e. electron and hole) trap, is modeled by a short-range (localized), electrical neutral, 3-dimensional, square-well, perturbation potential, with an amplitude of Δ and a full-width of W. This is shown in Fig. 10(a) for Δ>0 or electron-repulsive or hole-attractive to give a hole bound state, and in Fig. 10(b) for Δ<0 or electron-attractive or hole-repulsive to give an electron bound state. The microscopic origins of the Δ’s are electric dipole-multipoles perturbation potentials from the displacement of the core charges, Si⁺⁺ and O⁺⁺, or the variation of the Si:Si and Si:O bond length and angle, at the SiO₂/Si interface. The n-th bound solutions (bound-electron and bound-hole one-electron wave functions) would be 2.5-dimensional ψₙ(x,y,z) or quasi two-dimensional with slight penetration into the SiO₂ side (x<0, y, z) which is behind such a high potential wall, >3.13eV for the bound electron and >4.25eV for the bound hole, shown in Fig. 10(a), that it can be viewed as an impenetrable potential wall. This spatially symmetrical (y,z) localized perturbation does not shift any energy levels in the Silicon conduction and valence bands that have spatially anti-symmetric wave functions Φₙ, shown by the solid horizontal lines in Figs. 10(a) and 10(b), only those with symmetric wave functions Φₙ (long dash lines), by virtual of integration over the 2-dimensions (y, z) of the 2.5-dimensional physical space. The dipole and multipoles perturbations do not have the symmetry assumed here, but are still very short-ranged in comparison with spherically symmetric long-range 1/r Coulomb potential of a point charge.

As shown in Fig. 10(a), when the energy perturbation Δ is positive, all the symmetric-wave-function states are shifted upwards, and one of which in the silicon valence band at the SiO₂/Si interface is shifted upwards into the Si energy gap and forms a bound hole state or hole trap state which is localized at the perturbation site with the shallow-donor-impurity-like charge-states (0 and +1) and an energy level or hole binding energy of Eₙ-Eᵥ. The ideal model for an isolated and single perturbation in Figs. 10(a) and 10(b), can now be applied to the SiO₂/Si interface of an MOS capacitor or transistor. The conventional thermal oxidation process is not epitaxial. It is limited by the diffusion of neutral oxygen atom from the ambient through the already-grown SiO₂ to the SiO₂/Si interface where the oxygen reacts with a silicon to form new interfacial mono-layer of SiO₂. The diffusion process is random, giving rise to random variations of bond-angle and bond-length of the strain-distorted Si:Si and Si:O bonds [6,7,8]. These random perturbations are short-ranged and nearly electrically neutral compared with the long-ranged Columb potential of a point charge, and are highly localized at the distortion sites. To illustrate this graphically, Fig. 10(c) shows that two energy or potential perturbations (Δ>0 and Δ<0) at two interface locations could produce two discrete interface trap levels Eₙ and E₆ in the silicon energy gap which are physically localized at the SiO₂/Si interface plane but widely separated in the interfacial plane, (y, z). Extending these two perturbations to many perturbations from the random variations of the length and angle of the many Si:Si and Si:O bonds at the SiO₂/Si interface plane or boundary, and using the conservation of the number of quantum states, then N random perturbations at N interface locations would give N bound states, each localized physically or spatially at one of the N perturbation sites. From perturbation mathematics, small changes of the angle and length of the bonds from those of the perfectly periodic lattice at the SiO₂/Si interface give small perturbation
amplitudes, hence small binding energies or shallow trap energy levels near the two band edges. Similarly, large changes of the angle and length of the interfacial bonds give large perturbations, hence, large binding energies or deep trap levels as measured from one of the two energy band edges. For a good SiO₂/Si interface, usually attained in today’s manufacturing of silicon MOS and non-MOS integrated circuits, there are few large changes of angle and length of the interfacial bonds, hence few deep trap levels, and there are many small changes of angle and length of the interfacial bonds, hence many shallow trap levels. These changes are the result of the fundamental statistically-distributed thermodynamic fluctuations during oxidation and cooling, which could be reduced to negligible density by epitaxial growth, a wish yet fulfilled. The randomness then give rise to the U-shaped density of interface traps, which is sketched in Fig. 10(c) and labeled DOS. A particular feature of the interface traps from the electrically neutral perturbation represented by the short-range square-well potential of strength ∆ is that the gap levels from the conduction band levels have the acceptor-like charge state, (0, -1) respectively before and after the capture of an electron from the conduction band, while those from the valence band states, the donor-like charge states, (0, +1) respectively before and after the capture of a hole from the valence band. The donor-acceptor charge-state designations are exactly the opposite to those shown in Figs. 10(a) and 10(b), for the group-2 and group-3 ionized acceptor impurities and group-5 and group-6 ionized donor impurities with the Coulomb-like trap potentials, a constant confusion in the literature of interface traps from day-1 since the Bardeen surface states models.

From the energy band diagram description alone, one might expect additional electronic transitions between adjacent interface traps. These inter-trap transitions are extremely unlikely because of the highly localized trapped-electron and trap-hole wavefunctions at the highly localized short-range perturbation potentials (~ interatomic spacing ~ 1Å) and the large inter-trap distance at the usually observed low trap concentration in fresh or unstressed, unused transistors, 10¹⁰ cm⁻², or 10¹⁴ A⁻¹, and even at the limiting interface trap densities (from used-up MOS flash memory transistors after about 20000 write-erase cycles), 10¹⁵ cm⁻², ~30Å, which is still much larger than the interatomic spacing of ~1Å and the similar radii of the trapped electron and hole wavefunction, especially at deep midgap interface traps, but inter-trap transition could be responsible for the 10-year retention time.

Thus, the U-shaped electronic density of state of the interface traps at the thermally grown SiO₂/Si interface is a foregone conclusion based on the simple microscopic picture just described rather than discrete levels [37, 38] I (Sah) thought we finally observed experimentally! The U-shaped DOS is consistent with all the experiments, some of which are described in the preceding section-2, in particular, the theoretical account based on U-shaped electronic energy density of interface traps [3] of the experimental line-shape of the bell-shape Recombination DC Current-Voltage (R-DCIV) curves measured on a variety of MOS transistors, first in 1961 [29, 30] and recently in 2002 [31, 32].

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References


[12] Chih-Tang Sah, “A new semiconductor tetrode – the surface-potential controlled transistor,” Proc. IRE, 49(11), 1623-1634, November 1961. This article reported the historical first measurement of low frequency noise in a MOS transistor. See Fig. 8 on p.1625 for the frequency dependence of base equivalent input noise voltage for several grid (gate) voltages in a bandwidth of 6 cps and source resistance of 500 ohms, with a shot (thermal) noise of 0.015 µV and the 1/f corner frequency of 700c to 30kc.


