BONDING PAD WITH REDUCED CAPACITY

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ABSTRACT

Technical solutions for the Integrated Circuits (ICs) packaging remains more conservative than other facets of microelectronic development. The ICs with active components, having size of micrometers or nanometers, continue to have bonding pads areas within thousands square micrometers. The leads from the contact pads on a silicon substrate to the terminals in its package are bonded creating a parasitic capacitor. This process is one of the most critical steps influencing the reliability of the High Frequency (HF) Junction Field Effect Transistors (JFETs).

We developed a bonding pad design, with parasitic capacity determined by a contacting spot between only the wire and the bonding pad metallizing. The proposed solution allows for decreasing the gate-draining capacity (Cgd) in the pair of JFETs from 1.15 – 1.2 pF to 1.0 – 1.05 pF. We have supplied JFETs having bonding pads, with this technique, for wideband (0-500) MHz oscilloscopes

Keywords: bonding, design, pad, punchthrough, reliability

1 INTRODUCTION

Technical solutions for the Integrated Circuits (ICs) packaging remains more conservative than other facets of microelectronic development. The ICs with active components having size of micrometers or nanometers continue to have Bonding Pad (BP) areas within thousands square micrometers. The bonding task parameters include: the connecting wire size, applied welding or soldering equipment. The leads from the contact pads on a silicon substrate to the terminals in its package are bonded creating a parasitic capacitor. This process is one of the most critical steps influencing the reliability of the High Frequency (HF) Junction Field effect Transistors (JFETs).

2 BONDING PAD AND IC RELIABILITY

An ultrasonic transducer is a common method of a wire attachment. In this method, the wire is brought into contact with the bond pad and then vibrated under pressure. This breaks through any surface oxide or contamination and affects a cold weld between the freshly exposed metallic surfaces. This aspect of bonding is very much dependant upon the method of bonding that is foreseen. Aluminum wedge bonds need a more rectangular bond pad form whereas gold ball bonds favor a more square form pad. As device sizes continue to decrease and the number of connections (i.e., the pin count) increases, it is necessary to reduce both the bond pads size and spacing. Bonding pads are connected to the silicon substrate through a parasitic capacitor. As the substrate is conductive, electrical signals, applied to the pad structure, may couple to other nearby structures, including other pads [1]. Introducing new intermetal materials, with improved electrical properties but lowered mechanical resistance requires, in terms of reliability, designing new structures for pads [2].

To solve the problem of a reliable connection between the die and the wire there are several main directions: a) design, b) technological features, c) new connection methods, and d) testing process improvement.

Design and technological features are used for an active device under bond pads to save Input/Output (I/O) layout for high-pin-count socket [3]. This solution allows bonding pads to be placed directly upon device's active zone. This designing method is combined with a series of complicated technological operations and tests.

Several new technological processes include sandwiching several metal-dielectric metal structures [4] and additional trench [5]. New intermetal materials with improved electrical properties have been introduced [2], but they lowered mechanical resistance, required in terms of reliability.

As integrated circuits have become increasingly smaller, electrically conductive structures are placed closer within the ICs. This situation tends to enhance the inherent problem of parasitic capacitance between adjacent electrically conductive structures. Shifting to the higher frequencies requires new semiconductor materials, especially based on $A^{III}B^{V}$ or $A^{II}B^{VI}$ hetero-structures as well as sophisticated measurement methods that take into consideration contact effects [6].

At the same time, new electrically insulating materials have been developed, for the usage between conductive structures, reducing parasitic capacitance. The new electrically insulating materials typically have lower dielectric constants (k), relative permittivity (ε_r), and thus, are generally referred to as low-k materials. While low-k materials help to resolve the capacitance problems described above, at the same time, they tend to introduce new challenges. Low-k materials are typically filled with small voids that help reduce the material's effective dielectric constant. As there is less of the material itself

within a given volume, it tends to reduce the overall structural strength. The resulting porous and brittle nature of such low -k materials present new challenges in both the fabrication and packaging processes. Unless special precautions are taken, the robustness and mechanical reliability of an integrated circuit that is fabricated with low-k materials may be lower that of an integrated circuit that is fabricated with conventional materials. Low-k materials differ from traditional materials in properties such as thermal coefficient of expansion, moisture absorption, and adhesion to adjacent layers, mechanical strength, and thermal conductivity. The low-k dielectric layers [7] decreasing parasitic capacitance have been introduced. After that, developers had to solve the tasks facing new challenges. New design implies an introduction of new, complicated technological operations. The low-k layers reduce mechanical resistance, thus upsetting the established technological yield balance.

Other solutions include a serial connection of a parasitic Metal Oxide Semiconductor (MOS) capacity with a p-n capacity (n- type isolated zone under bonding pad) that decreases bonding pads stray capacitance by (10-20)%. Oxide SiO_2 is the perfect solution for dielectrics in Si technology with ε_r = 3.7. Polysilicon, widely used as an insulating material in semiconductor's industry has, unfortunately higher relative permittivity value: ε_r = 7.5. More possibilities for bonding pad's capacitance reduction in case of MOS with serial p-n capacity, can be provided by using a reverse-bias voltage (Urb), applied to isolated zone, under the bonding pad. Ordinary, similar solution is used in bipolar technology devices for the purpose of electrical isolation by p-n junctions.

A better effect is obtained if an independent source of power is used. An independent power source allows decoupling of parasitic capacitances from supplying voltages. The technological process includes a contact formation to n- or p - isolated zone. The reverse - bias voltage, less than breakdown for MOS structure, is applied to the bonding pad – oxide – n (p) zone and p-n junction as well. We mention the important topology feature for this bonding pad: any interconnection between bonding pad and contact to isolated zone is impossible. The design requires a part of the isolated zone shape change and/or the bonding pad's shape change. As the p-n junction capacitance is proportional to a square root of the reverse-bias voltage; a useful effect can easily reach 2-5 times.

More complex technologies [8-10] allow creating a thick insulating layer under the bonding pad. A bond pad structure using semi-insulating porous silicon (PS) has recently been proposed for the purpose of reducing the parasitic pad capacitance and increasing the crosstalk isolation characteristics on low impedance p^-/p^+ epitaxy substrates for high-performance CMOS [8]. The technological process is quite complicated and critical to the p – regions' concentration.

We could not solve problems with leakage on the p-n - junctions' border of active zone (JFETs channels) after receiving porous regions in p-silicon[9]. The problems with oxidation and metallizing of "dirty" technological process significantly increases 1/f – noise, leakage, and reduce breakdown parameters. The application of porous silicon only for decreasing stray capacitance bonding pad – substrate, especially for digital ICs gets great improvement [8]. A smooth Polysilicon bond pad with a solid-oxide island underneath [10] has an implementation on a 15 mkm thick Silicon on Insulator (SOI) substrate.

3 BONDING PAD DESIGN

We developed a bonding pad design [11], with parasitic capacity determined contacting spot between only the wire and bonding pad metallizing. This new bonding pad

The technique has been used for a HF JFETs and does not require significant technological changes. Respective design is explained below. The p- type substrate is the bottom gate of two gate's (top and bottom) JFETs. The channel is an n-type epilayer. The source and the drain bonding pads are formed on the surface of the substrate and make complementing components in spurious capacities of gate-drain (Cgd) and source-gate (Csg). The gate length (Lg) is limited to 2.0 micrometers. The attempt to further decrease Lg generates the problem as it transforms output Volt Ampere Characteristic (VAC) from pentode into triode one.

Our design avoids the decrease of load characteristic (i.e. saving pentode VAC) and reduces interconnection capacity. We have decreased the gate-drain capacitance in the pair of JFETs from (1.15 –1.2) pF to (1.0 –1.05) pF. The technique is used to supply JFETs for wideband (0 – 500) MHz oscilloscopes.

The advantages are:

1. A working convenience for the soldering operator due to saved space outside of the bonding pad
2. A stray capacitance is diminished up to three times
3. The same level of reliability as for standard bonding pad
4. Open the way to reduce the wire diameter and develop new types of equipment and tools
5. The design can be applied in a number of semiconductor's technological processes including hybrid circuits

The described bonding pad design fits well with automatic bonding process. The solution allows an alignment wire to be in a pad center for any "target" shape. A displacement's sensor can visualize current alignment and compare it with memorized image.

Several variations of these topologies are represented on Figure 1 (for square-, round-, and rectangle-shaped tools for different soldering methods).

We can see bonding pad's outstanding parts (1) on Figure 1, not covered by soldering tool heads (2). Those outstanding parts, not shadowed by soldering tool, enhance operating visibility/alignment during wire bonding.

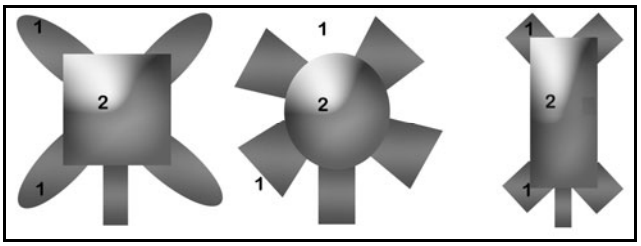

Figure 1: Pad topologies (1) and soldering tools (2)

As the wire is bonded to the pad a bonding spot is created, having the size almost twice as wire diameter. Our design has the aim to limit resulting capacitance to the spot capacitance thus, excluding bonding pad area influence. The design main feature is dividing BP in several parts: a) central monolithic area (core), which repeats the bonding spot shape and b) a rest of the BP consisting of separated micropads. The visible parts (1) on Figure 1 are entirely done by micropads with minimum gaps between them. The bonding pad spot, formed during the soldering process, may have misplacement, if it is shifted outside central, monolithic area. In this case the part of discrete micropads, underneath bonding spot, is used. This feature allows the contact areas automatic adjustment resulting in a reliable connection with minimum parasitic capacity. The described misplacement varies from zero to 10-20 mkm and depends on specific tools and operation environment.

BP Size/Spot (mkm)	**(100x100)/ (50x75)**	**(90x90)/ (40x65)**	**(80x80)/ (30x55)**
Capacitance for a 20mkm misplace, pF	0.18	0.125	0.095
Capacitance for a 10mkm misplace, pF	0.167	0.11	0.073
Capacitance for a 0 mkm misplace, pF	0.12	0.07	0.05
Capacitance for a 0 mkm misplace, pF standard BP	0.3	0.24	0.19

Table 1: Bonding pad resulting capacitance, pF

As we can see from data Table 1, even in the worst case scenario, with the maximum misplacement, our design gives us technical effect in lowering resulting capacitance up to 1.8 times. The best outcome is in the case of minimum misplacement. A reduction in the parasitic capacitance over 3.7 times by comparison with conventional bonding pads is obtained. Our research shows that in eighty percent of every type of bonding pads exists a misplacement of up to 10 mkm from center (ideal position).

A soldering methods change, reduction in wire sizes, introducing new wire materials, and new tools would require, if using proposed design, only new bonding pads' drawings and would keep technological yield rate.

The new bonding pad design allowed us to benefit from the higher level of flexibility during packaging process developing with reduction of wire diameters (from 27 to 22 mkm and less). We were able to use several various wire diameters to obtain minimum parasitic capacitance and keep the reliability simultaneously.

It is especially important to overview bonding pad design influence in the case of JFETs structures. An attempt to decrease the bonding pad size for the lowering of parasitic capacitance is a standard approach. But the result is a dramatically decreased yield and reliability, particularly, after thermal cycles. There are several reasons for this, but the main two are:

1. A wire is transformed into flat oval shape after soldering. A small misplacement between the wire and pad contacting spot resulting in a partly covered pad's metallizing, and partly the wafer surface, covered with SiO_2. The more misplacement - the more SiO_2 is covered instead of pad's metallizing.
2. As the pads become smaller, the same situation occurs; even the wire is in the pad's center. The wire itself starts overlapping SiO_2 and many failures appear after thermal cycle and test.

The bonding pads' size continue decreasing from 100 x 100 mkm to 60 x 90 mkm [12], 40 x 40 mkm [13] and less [14]. Probe heads (also called manipulators or positioners) often have to carry measurement modules (e.g. tuners for noise and load pull measurements as well as for test at 110 GHz) without restricting their positioning accuracy. Bonding pad contact must be made in the middle of a high frequency pad, which is sometimes as small as 40 x 40 mkm [13]. Our solution allows for having comfortable conditions for fast, reliable contact with the target in the center of the bonding pad, ensuring smallest spurious capacity.

Modern electronic equipment uses MOS and JFETs, which receive inputs from various sources, and have outputs that control equipments' operation. The integrated circuits' inputs and outputs may be subject to undesirable high voltage electrostatic discharge (ESD) in addition to the desired signal level. Various voltages Protection Elements (PE) have been used to limit the peak voltage in the integrated circuits. Attempts have been made to incorporate ESD protection within the integrated circuit. The idea is not very effective as requires a significant amount of area within the integrated circuit die, and may add unacceptable additional capacitance to the circuit node being protected. Design – technological improvements [16] allow partial solutions of these new challenges. ESD is located directly under the bonding pad [16], integrated with the BP [15, 16] or directly built-into the protecting input JFETs [16, 17]. The design [16] is based on punchthrough effect. The solution [16] uses a combination of a punchthrough (reach-

through) effect to transmit a voltage on the buried p^+n^+ junction and avalanche (Zener) process. Flexibility provided by both solutions [15, 16] and their integration with the bonding pad, increases functionality, improves reliability, and resistance to overvoltages.

The BP design, with parasitic capacity determined by the contacting spot between the wire and the bonding pad metallizing, is utilized in HF input devices for precision measuring equipment. The proposed solution allows decreasing the gate-drain capacity in the pair of JFETs [18] from (1.15 – 1.2) pF to (1.0 – 1.05) pF. The new types of high frequency JFETs have a redistribution of squares that are occupying source and drain regions (asymmetric structures). The additional advantage [19] is a reduction of 1/f - noise. We are discussing outcomes that lead to decreasing the JFETs capacitance values by (0.1-0.15) pF - small numbers, but it is significant in terms of technical profit. The high speed $A^{III}B^{V}$ semiconductors (GaAs, InP) [21], as well as hetero-structures are able to provide active components with Ft up to 100 GHz. Such BP capacitance values for HF components provides an additional passband extension up to hundreds MHz and GHz for microwave devices, with highest linearity, decoupling, accuracy, and minimum HF-noise.

4 CONCLUSION

The proposed design save JFETs load characteristics and reduce interconnection capacity. We have successfully supplied JFETs for wideband (0-500) MHz oscilloscopes using bonding pad techniques described above. As IC active components' number increase, oxides' thickness decrease and bonding pads become an important functional part, that influence core IC duties via parasitic capacitance.

REFERENCES

[1] D. Koester, A. Cowen, R. Mahadevan, M. Stonefield, and B. Hardy, PolyMUMPS Design Handbook, 9th Ed. MEMSCAP, Bernin, France, 2003.

[2] G. Bouche, R. Gonella and E. Sabouret, Bonding Pad Resistance, A Combined Approach, Proceedings of the Int. Conf. Nanotech 2001, Vol.1, pp. 442 - 445.

[3] Ming-Dou Ker, Jeng-Jie Peng, Hsin-Chin Jiang, Active device under bond pad to save I/O layout for high-pin-count SOC, Fourth international symposium on quality electronic design, p. 241.

[4] Ming-Dou Ker, Hsin-Chin Jiang, "A low-capacitance bonding pad for a semiconductor device", U.S. Patent 6717238, April 6, 2004.

[5] Seung Jong Yoo,"A method of forming a bonding pad of a semiconductor device", U.S. Patent 7037826, May 2, 2006.

[6] A. Ivascenco, A. Barciuc, V. Tarcenco, Some problems on DLTS method caused by nonexponential relaxation of barrier capacitance, Proceedings of International Conference on Application and theory electro-technique, ICATET91. Craiova, Romania, 1991, p.A6.

[7] Derryl D. J. Allman, Charles E. May, "Bond pad design", U.S. Patent 7023067, April 4, 2006.

[8] Chong Kyushu, Xie Ya-Hong, Low capacitance and high isolation BP for HF RFICs, IEEE Electron Device Letters, 2005, vol. 26, No10, pp. 746-748.

[9] L. Jurchenok, I. Mats, V. Bondarenko, V. Labunov, "Method of semiconductors devices manufacturing with operating p-n-junction", U.S.S.R. Patent 1267993, July 1, 1986

[10] R. Abdolvand, G. K. Ho, F. Ayazi, Poly-wire-coupled single crystal silicon HARSS filters using oxide islands, Solid-State Sensor, Actuator and Microsystems Workshop, South Carolina, June 6-10, 2004, pp. 242-245.

[11] I. Mats, "Bonding pad", Russia. Patent application 5066915, priority as of June 30, 1992.

[12] M. B. Ketchen, M. Bhushan, Product-representative "at speed" test structures for CMOS characterization, IBM Journal of Research and Development, 2006, vol.50, no 4/5, pp.451-468.

[13] High Frequency Probing, www.suss.com. SUSS MicroTec, Süss Str.1, Sacka, D-01561,GERMANY

[14] Automated Ribbon Bonding for Microwave and MCM Applications. Palomar Technology Inc., 2728 Loker Avenue, West Carlsbad, CA 92010

[15] Jun Cai, Keng Foo Lo, "ESD protection network with field oxide device and bonding pad", U.S. Patent 6417541, July 9, 2002.

[16] I.Mats, "Stabilizer diode", Russia. Patent application 5066877, priority as of June 30, 1992.

[17] I. Mats, E. Matson, I.Nichiporovich, "JFET with protection," U.S.S.R. Patent 1463081, March 23, 1989.

[18] I. Mats "The topology optimization of high frequency transistors for matched JFET pairs. Development of wideband components for oscilloscopes and digital voltmeters with high input resistance", Report at development project, State registration Y17809, Minsk scientific and research institute of engineering, 1987, Minsk, Belarus.

[19] I. Mats, "JFET", Russia. Patent 2024996, December 15, 1994.

[20] Wang J, Bing XO, Cai PF, Tian JB, Sun CZ, Luo Y, Novel planar electrode structure for high-speed (> 40 GHz) electroabsorption modulators, Jap. J. of Appl. Physics, 2006, part.2, vol. 45, No. 42-45, pp. L1209-1211.

[21] V. Blaje, G. Korotchenkov, V. Tarcenco, The thermal treatment of the Indium Phosphide surface and the Au-n-InP contact's properties, "Elektronnaya Technika" ser. 1, Ultra High Frequency Electronics, pp. 57-60, 1988 (in Russian).