A Simulation-Based Hybrid Optimization Technique for Analog and Digital Integrated Circuits Design Automation

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ABSTRACT

In this paper, a simulation-based optimization technique for integrated circuit (IC) design automation is presented. Based on biological inspired techniques, numerical deterministic methods and circuit simulator, the hybrid optimization methodology is developed for IC design. Two different circuits, low noise amplifier (LNA) and static random access memory (SRAM) are analyzed with our technique. Considering LNA IC, we simultaneously evaluate specifications including S parameters, K factor, noise figure, and input third-order intercept point in the optimization process. If the simulated results meet the aforementioned constraints, we output the optimized parameters. Otherwise, one of evolutionary algorithms will enable us to search solution globally; simultaneously, numerical optimization methods solve the solutions according to the results of global search. A circuit simulator calculates the circuit's characteristics with the updated configurations, and the developed prototype will evaluate newer results until all specifications are matched. Similarly, by considering the static noise margin (SNM), optimal device's channel length and supply voltage for SRAM cells with different circuit types could be tuned. Our preliminary results confirm the robustness and efficiency of the proposed simulation-based optimization technique.

Keywords: simulation-based, hybrid optimization, low noise amplifier, static random access memory, integrated circuit, circuit design, digital circuit, analog circuit, design automation, circuit tuning, methodology

1 Introduction

Computer-aided circuit simulation and analysis plays a crucial role in analog and digital integrated-circuit (IC) design and chip implementation [1–5]. Designers are requested to tune parameters of circuits to achieve a specified system. The parameters includes active and passive device parameters, device size, circuit layout, width of wires, and biasing condition. Circuit simulation tools are used in IC design in the past decades, but it requires a very experienced electronic engineer to accomplish complicated works. Optimization techniques continuously benefit the communities of electronic design automation [6–8].

In this paper, based on biological inspired techniques (e.g., evolutionary algorithms) [6–8, 14–18], numerical optimization methods (e.g., gradient-based methods) [11, 12, 14], and circuit simulation tool [6–13], a simulation-based hybrid optimization technique for circuit design automation is advanced and applied to optimal design of two important circuits, LNA and SRAM. For a given analog circuit, such as LNA the hybrid optimization method simultaneously considers the electrical specifications such as S parameters, K factor, the noise figure, and the input third-order intercept point in the optimization process. First of all, preliminary parameters as well as the netlist for circuit simulation [6,13] are loaded. A circuit simulation tool will be performed for the circuit simulation and then the results are used in the evaluation of specification. Once the specification meets the aforementioned constraints, the optimized parameters will be outputted. Otherwise, we activate an evolutionary method, such as genetic algorithm (GA) [6–8] for the global optimization; in the meanwhile, a gradient-based method, such as the Levenberg-Marquardt (LM) method [11, 12] searches the local optima according to the global searched results. The numerical optimization method does significantly accelerate the evolution process. We repeatedly call circuit simulator to compute and evaluate newer results until the specification is matched. To verify the validity of the proposed methodology, several testing experiments are organized, where we simultaneously consider the characteristic optimization of passive and active devices, and power dissipation. For the LNA with the 0.18 μm CMOS technology, more than fifteen parameters including device sizes, capacitance, inductance, resistance, and biasing conditions are optimized with respect to the aforementioned constraints. Considering the static noise margin (SNM) [3–5] of six- and four-transistors (6T and 4T) SRAM cells with 65 nm CMOS devices, we also successfully tune device's channel length and supply voltage to meet the specified target of SNM. Benchmark results confirm the robustness and efficiency of the proposed simulation-based hybrid optimization technique.

This paper is organized as follows. In Sec. 2, we introduce the framework of the proposed optimization

technique. In Sec. 3, the achieved results are discussed. Finally, we draw conclusions.

2 The Optimization Technique

Modern IC design is a real-world challenge to solve multidimensional optimization problems by using either conventional numerical method [6,9–12] or soft computing techniques [6–8]. Our idea of the simulation-based hybrid optimization technique takes a evolutionary algorithm to perform global search, and while the evolution seems to be saturated, the gradient-based method is then enhancing the searching behavior to perform the local search.

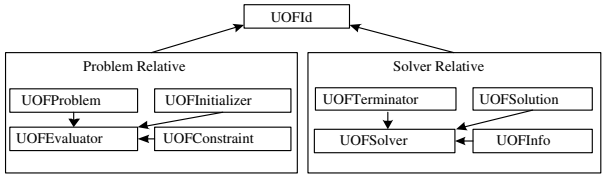

Figure 1: An illustration of the architecture of the developed unified optimization framework.

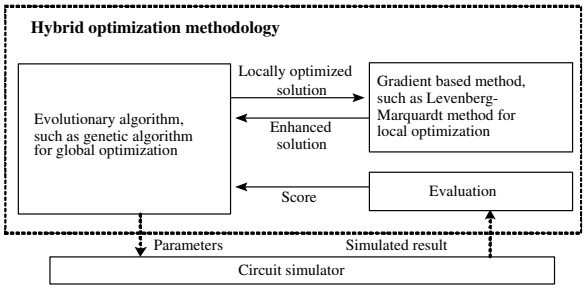

Figure 2: The flow of the proposed simulation-based hybrid optimization technique.

Figure 1 is an architecture of the developed unified optimization framework (UOF) and Fig. 2 shows the optimization flow for the proposed hybrid optimization technique. Based on global evolutionary algorithms, numerical deterministic methods, and C++ objective design, the developed framework can bridge the optimization methods and IC designs. The developed UOF [14] consists of two parts, one is problem related and the other is solver related. For problem related part, it contains the main body of the problem, initialization, evaluation, and constraint. A solver includes the solution procedure, termination, and information. Separation of each part into several classes increases the efficiency of reutilization. The UOFProblem class is the main class to define the problem; as for UOFInitializer class, it is responsible for the initialization of the solution for each problem; The UOFEvaluator class provides the method

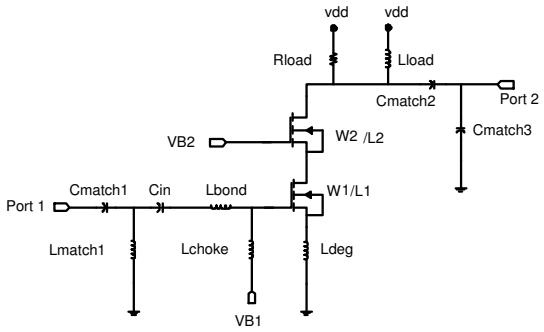

Figure 3: The explored LNA circuit in our experiment. The Lload and Rload are the compact models of on-chip spiral inductors. The choke inductor Lchoke working at high frequency is fixed at 1uH and Cin is an external signal couple capacitor which is fixed at 20pF. The compact model BSIM 3v3 is adopted for the 0.18 μm metal-oxide-semiconductor field effect transistors (MOSFETs).

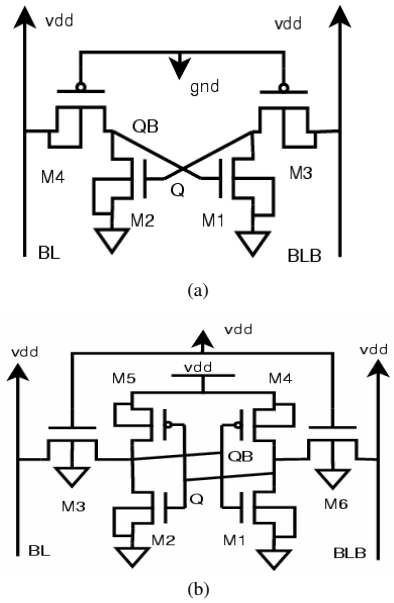

Figure 4: The explored (a) 4T and (b) 6T SRAM cells. The circuit of 6T SRAM is a flip-flop comprising two cross-coupled inverters and two access transistors, M3 and M6. The flip-flop consists of two load elements (M5, M4) called pull-up (load) transistors and two storage elements (M2, M1) called pull-down (driver) transistors. Data are stored as voltage levels with the two sides of the flip-flop in opposite voltage configurations, that is, node Q is high and node QB is low in one state and node Q is low and node QB is high in the other resulting in two stable states.

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of evaluating the result obtained by UOFProblem derived classes; The UOFConstraint class defines the type and candidate or range of each parameter. On the other hand, the UOFSolver class takes the major character in solver relative category, and the UOFSolution class stores possible solutions and several operators of the specified solver; class UOFTerminator judges when and how to stop the optimization process of the solver; and UOFInfo class logs the behavior of the solver during the solving process.

Based on the developed architecture, the UOF can easily integrate well-known circuit simulation tools, such as HSPICE [13], ELDO, SPECTRE, SmartSPICE in the optimization flow. For a circuit to be optimized, we automatically parse and generate the corresponding netlist of the circuit for the circuit simulation and result evaluation. If the result meets the target, we output the final optimized data. If the error between the target and result does not meet the stopping criterion, the established optimization kernel will enable the circuit parameter extraction in a global sense, where the number of parameters to be extracted depends upon the specification that we want to be achieved. According to the optimized results, the netlist is updated and the next optimization is repeated. As shown in Fig. 2, the prototype searches the entire problem space. During this period, the global-searched candidates will be inputted into a circuit simulator to retrieve the simulation results, where a set of differential equations is solved numerically. According to the specified targets of S_{11}, S_{12}, S_{21}, S_{22}, K factor, the noise figure, and the input third-order intercept point for a LNA circuit, the results are evaluated to measure the fitness score, which guides the evolutionary process. Once a solution is obtained, the gradient-based numerical method solves the problem locally. The local optima are right the initial values of evolutionary algorithm for further optimization.

3 Results and Discussion

Figure 3 shows the explored LNA circuit, Figs. 4(a) and 3(b) are 4T and 6T SRAM cells. The tested LNA IC focuses on the working frequency ranging from 2.11GHz to 2.17GHz. There are more than fifteen parameters to be extracted in the designed LNA with 0.18 μm technology. Table 1 shows the optimized parameters of the investigated experiment. The specified targets and extracted results of S parameters, K factor, the noise figure, and the input third-order intercept point are listed in the Tab. 2. It shows that the extracted parameters can satisfy all the specified targets.

Considering the static noise margin, we set targets of 190 mV and 173 mV for the 4T and 6T SRAM cells, as shown in Figs 4(a) and 4(b). The SNM is the minimum DC-voltage disturbance necessary to upset the state of SRAM cell. It is quantified by the length of the side

Table 1: A list of the range of designing parameters and the optimized parameters for the LNA circuit. Its operation frequency varies from 2.11GHz to 2.17GHz. for the LNA circuit.

Element	Unit	Range	Result
Cmatch1	F	$300 \sim 800$	657.738 f
Cmatch2	F	$1 \sim 10$	4.505 p
Cmatch3	F	$1 \sim 10$	4.951 p
Lbond	H	$1 \sim 10$	1.058 n
Ldeg	H	$0.1 \sim 5$	1.155 n
Lmatch1	H	$1 \sim 10$	5.257 n
Rload	Ω	$1P5 \sim 5P5$	3P5.l
Lload	H	$1P5 \sim 5P5$	3P5.l
VB1	V	$0.5 \sim 1.5$	0.69 V
VB2	V	$0.5 \sim 5$	1.96 V
L	H	$0.13 \sim 0.3$	0.25 u

Table 2: A list of the specified targets and the extracted results for the LNA circuit.

Specification	Target	Test
S_{11}	$<$ -10dB	-35.1dB
S_{22}	$<$ -10dB	-19.1dB
S_{12}	$<$ -25dB	-38.3dB
S_{21}	as large as possible	11.3dB
K	> 1	11.1
NF	< 2	1.17
IIP3	$>$ -10	0.3

Table 3: A list of the range of designing parameters and the optimized parameters for the 4T and 6T SRAM cells. The optimization is subject to specified target of SNM in the SRAM cells.

Factors (Parameters)	Range	Result (6T)	Result (4T)
L1: channel length of transistor M1 (nm)	$60 \sim 70$	68.3	67.8
L2: channel length of transistor M2 (nm)	$60 \sim 70$	62.2	65.9
L3 : channel length for other transistors (nm)	$60 \sim 70$	69.1	63.2
Vdd: supply voltage (V)	$1.08 \sim 1.38$	1.35	1.22

of the maximum square that can fit inside the butterfly curves formed by the cross-coupled inverters. The cell stability is based on the ability of the cell to resist accidental overwrites during different operating conditions in the presence of electrical noise and process variations. The factors that influence the cell stability include the device size (channel widths and lengths), the supply voltage, and temperature. In this work, we adjust the device's channel length and supply voltage to fit our targets. The range of the circuit parameters and extracted results are summarized in Tab. 3. The results confirm the validity of the method.

4 Conclusions

In this paper, a simulation-based hybrid optimization technique for optimal design of analog and digital ICs has been advanced. Based upon global evolutionary algorithms, numerical deterministic methods, and one of the well-known circuit simulators, HSPICE, the hybrid optimization technique has been implemented. Different testing cases for the designed LNA circuit with the 0.18 μm MOSFETs and 6T/4T SRAM cells with 65 nm CMOS devices have been examined to show the validity, efficiency, and robustness of the method. We notice that the hybrid optimization methodology was proposed for model parameter extraction of sub-100 nm complementary metal-oxide-semiconductor (CMOS) devices and optimal characterization of heterojunction bipolar transistor in our early works [6, 8]. We have successfully generalized it to analog and digital IC design optimization. We believe that this hybrid optimization methodology can benefit advanced IC design and chip fabrication.

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