High Density Through Wafer Via Technology

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ABSTRACT

The Through Silicon Via (TSV) process developed by Silex offers sub 50 µm pitch for through wafer connections in up to 600 µm thick substrates. Silex via process enables MEMS designs with significantly reduced die size and true "Wafer Level Packaging" - features that are particularly important in consumer market applications. The TSV technology also enables integration of advanced interconnect functions in optical MEMS, sensors and microfluidic devices. With several foundry customers using the process today and an extraordinary line-up of potential users, Silex aims at making the process a standard in the MEMS industry. The swift propagation of the technology will be facilitated by reasonable licensing agreements and technology transfer programs with customers and partners who may favor implementation in their existing manufacturing lines. This paper gives a brief introduction to the via formation process and focuses in more detail on the novel solutions made available by this enabling technology.

Keywords: through silicon via, 3d interconnect, wafer level packaging, CMOS integration, interposer

1 INTRODUCTION AND BACKGROUND

Silex Microsystems offers MEMS foundry manufacturing services in its fully equipped 750 m² clean room state-of-the-art 6" wafer fab. With a team of skilled MEMS experts, Silex helps its customers to quickly take their design concepts to working prototypes and the following volume manufacturing. Since the company was founded in year 2000, Silex has successfully completed well over 100 MEMS products with more than 60 customers around the globe. Following the trend of the IC foundries, Silex is also continuously working on developing proprietary MEMS foundry processes, leveraging on intellectual property and know-how to complement the foundry manufacturing offer. One example of such MEMS process is this presented high density through wafer via technology that enables true wafer level packaging and MEMS designs with significantly reduced form factor. Silex diversified market exposure, large customer base and clear strategy to not offer any own products to the market ensures Silex customers a solid and reliable long term MEMS supply.

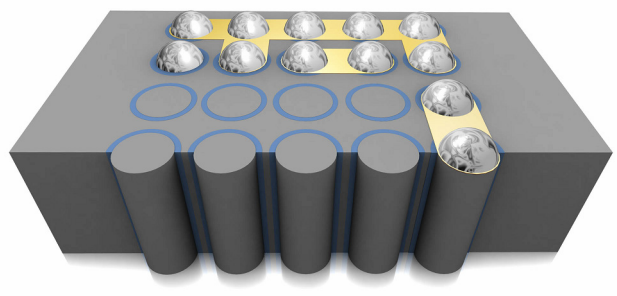

Figure 1: Schematic cross section of through wafer interconnect.

2 TECHNOLOGY

In response to foundry customer demand for through silicon interconnect functionality; Silex engineers invented the novel idea to isolate a section of a low resistivity silicon wafer laterally by incorporating a trench filled with an isolating material [1]. This isolating trench will most often have the shape of a square or a circle but could also take other shapes if necessary as long as it constitutes a closed loop. The process begins with the formation of the trench using a DRIE process, achieving the necessary high aspect ratio features in up to 600 µm thick substrates. Typical trench width is in the order of 10 to 15 µm.

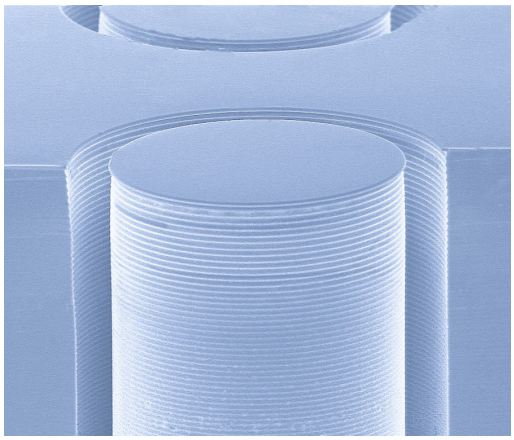

Figure 2: SEM picture of through wafer via "plug", formed using DRIE.

In order to keep the via plug in position, the trench etch stops short of reaching all the way through the wafer. Following the trench etch, the wafer is subject to a high temperature filling of the trenches by a dielectric material. Finally, a CMP process is applied to the backside of the wafer, removing the material that keeps the "via plugs" connected to the bulk, thereby isolating the via plugs from the bulk of the wafer.

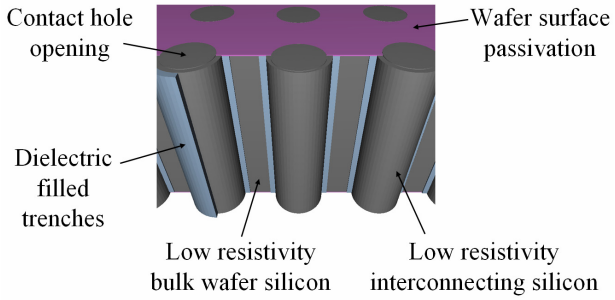

Figure 3: Schematic cross section of via substrate features.

In some sense Silex via technology could be associated with the Silicon on Insulator (SOI) technology, noting the 90° difference in the orientation of the buried insulator versus the plane of the wafer.

2.1 Typical Design Flow

Somewhat confidential in nature, design rules cannot be detailed in this paper, but some general remarks can be made with respect to deploying Silex via technology on wafer level. The typical procedure begins with the customer outlining the requested position of the through wafer connections on the wafer. For a pitch between vias in the order of 50 µm or less, it is necessary to have neighboring vias share the same isolating trench. There is no upper limit in terms of the size of the isolated area. In practice, a greater portion of the total wafer could be one isolated through wafer connection. As the designer can choose the trench layout freely, assuming a uniform trench width is used over the entire wafer, and the resistance is proportional to the cross section of the connecting silicon, shapes can be chosen that efficiently utilize the available space. In many cases there is a tight pitch requirement in one axis of the two-dimensional space but less of a limitation in the other axis. One practical example is the contact pads surrounding a CMOS chip. In such case, a larger total cross section area of the via connection, and thereby lower resistance, can be achieved by outlining the vias into the available chip area while maintaining a small pitch along the axis of the contact pads. Following customer input on the design layout, Silex engineers will cross check against design rules, taking into consideration wafer thickness and structural stability versus possible post processing requirements.

2.2 Process Implementation

From a technological standpoint, Silex via process is primarily a "via-first" process as it needs a high temperature filling step. From a MEMS processing perspective, the "via-first" approach is by all means preferred as in most cases completed delicate MEMS structures will not benefit from additional wafer level post processing and handling. Again, the completed via substrate wafer resembles the SOI wafer as it allows more or less unlimited processing of the substrate, even at temperatures exceeding 1000°C. This means the via substrate wafer will be used in the MEMS device manufacturing flow as part of the starting material.

Some applications may require a high resistivity device layer. As the inherent nature of the via process requires a low resistivity bulk part to create a low loss electrical connection, it is possible to integrate the via process into an SOI wafer with a low resistivity handle and high resistivity device layer. Depending on the post processing requirements, the contacting to the via sections in the handle part of the substrate can be made directly by one of the metal layers or alternatively by incorporating shallow trenches of doped polysilicon.

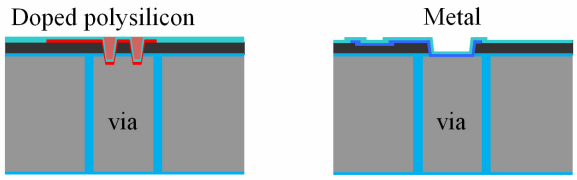

Figure 4: Integration of via process in SOI wafer with high resistivity device layer.

3 IMPLEMENTATION

When pros and cons of MEMS technology is debated in general, not rarely is the argument brought forth that the main hurdles relating to commercial implementation is packaging and interconnect. Silex via process virtually takes care of one of the inherent, most significant problems associated with MEMS by providing true wafer level packaging of MEMS.

3.1 Cost Factor

The via substrate manufacturing flow, containing a through wafer DRIE process and the following filling and CMP, does in volume production amount to an overall cost similar to that of an SOI substrate. The reduced form factor and wafer level packaging of the MEMS die, enabled by the technology, makes the implementation clear-cut for most applications with die size smaller than 5 mm x 5 mm.

3.2 Implementation Examples

To date, the via process has been offered to Silex foundry customers as an added value building block for integration in customers designs. One of the most unmistakable examples of via process implementation is the wafer level packaging of MEMS devices. A large portion of many MEMS die layouts are currently consumed by metal routing and contact pad area. Adding on top of that a standard ceramic package, the final component will in most cases be tenfold larger in area than the active die itself. Incorporating a via technology for the interconnect and wafer level packaging significantly reduces the form factor while getting rid of a large share of the traditional "back-end" process.

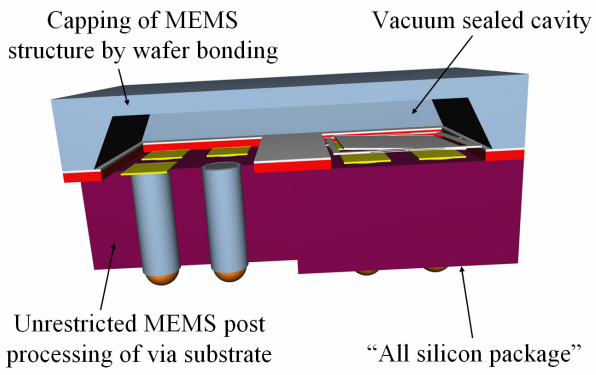

Figure 5: Example of wafer level packaging of MEMS device with 3D interconnect by Silex silicon vias.

Another area of interest for implementation is the integration of MEMS and CMOS. Very demanding micromirror structures in MEMS technology will have lower line yield than the accompanying CMOS wafer with drive circuitry. Through building the MEMS mirror array on a via wafer it is possible to integrate a probed MEMS mirror wafer with good yield to a good CMOS wafer, thereby saving very expensive material in the manufacturing process.

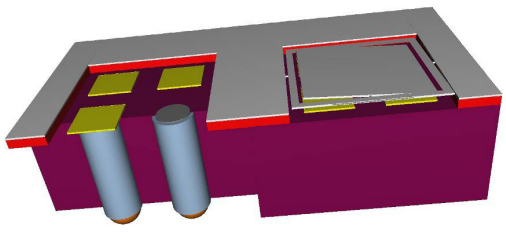

Figure 6: MEMS micromirror with Silex vias for cost efficient integration of MEMS and CMOS.

With the System in Package (SiP) approach, a number of integrated circuits are combined in a single module. The SiP can perform many of the functions of an electronic device, such as a mobile phone. The individual chips of a SiP are internally connected using flip-chip technology and may contain several silicon components (dies) and passive components all mounted on the same substrate, possibly also stacked on top of each other. This means that a complete functional unit can be built in a single package. This feature is particularly valuable in space constrained environments like mobile phones as it reduces the form factor and complexity of the PCB and overall design. Silex silicon via is well suited for this task as it allows post processing and integration of additional functionalities into the interposer die.

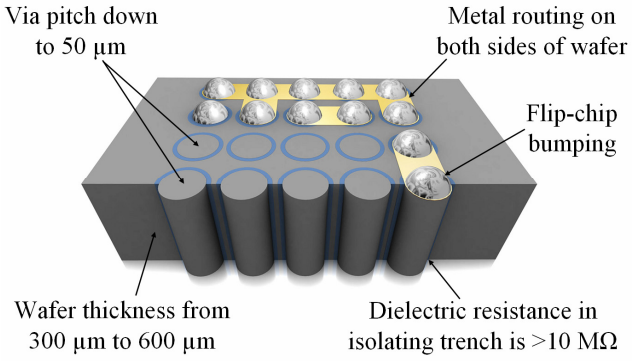

Figure 7: Interposer solution for system in package (SiP).

Many sensing devices such as flow- and pressure sensors require the chip to be located in close proximity to the media being measured. Under such conditions it can very often be useful to have the connection to the sensing chip made at the chip side that is facing away from the media.

Imaging is another sector helped greatly by a working high density via technology. Dies made up of large arrays of sensing "facets" require extensive metal routing in the same plane as the active area. Deploying a through wafer via technology, it is possible to save total die real estate while at the same time improving fill factor. Metal routing and flip chip mounting is easily accommodated on the back side of the die.

Also some microfluidic applications need integration of electrodes in the fluidic channels. Using Silex via technology to create electrodes in the channels is practical, and at the same time it allows the integration of more advanced MEMS features such as filters, high aspect ratio structured channels and silicon to glass bonding.

Traditional packaging of electronic components is based on low temperature or high temperature co-fired ceramics (LTCC or HTCC). With the trend of ever decreasing component form factors, advanced small scale packaging

may in the foreseeable future require other materials than ceramics to achieve the accuracy and reduction in footprint requested by the market. To some extent the limit may already have been reached for some ceramic based technologies as the existing manufacturing methods have difficulties achieving the small pitch for the electrical feedthroughs (<100 µm) and tight tolerances required when moving closer to "micro scale". In that respect, silicon stands out as a very good candidate with its long term reliability and high precision micromachining capabilities. In this respect, Silex via technology and MEMS processing technology can be implemented to realize customized silicon based wafer level packaging solutions.

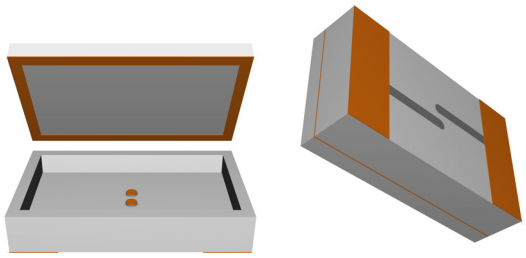

Figure 8: Wafer level micro scale packaging enabled by Silex via technology.

4 TECHNOLOGY LIMITATIONS

Limitations when it comes to implementing Silex silicon via technology is typically found in the domain of RF applications. When signal lines made of gold in many high frequency circuits are rendered too lossy and solutions are sought in copper, Silex silicon via will not do the job. Typical resistance in a standard via connection of 100 µm diameter in a 400 µm thick substrate is in the order of 1 Ohm and such resistance will in most RF designs constitute a higher than acceptable loss.

5 COMPETING TECHNOLOGIES

Via technologies is not a brand new concept in the MEMS community but have so far had modest success in terms of commercial viability. To be more precise, the various approaches have been struggling to a large extent with inherent technological difficulties tightly linked to the respective chosen technology. Typical issues with metal based vias have been the thermal incompatibility with silicon causing micro cracks and reliability issues. Furthermore, a metal via must always be incorporated towards the end of a MEMS process as the thermal budget of most metal candidates would not allow too much of high temperature post processing. Another quite common approach has been to use doped polysilicon for the through wafer connection. Some of the inherent problems of such approach is to get high enough level of dopants to accumulate during the filling of the via hole. Due to the low yield and very high via resistance of such process, it has not reached commercial viability.

6 TECHNOLOGY LICENSING

With several foundry customers using the process today and an extraordinary line-up of potential users, Silex will facilitate making this process a standard in the MEMS industry. In this context, Silex may also offer licensing agreements and technology transfer programs to selected customers and partners who would favor to incorporate the technology in their own existing manufacturing lines [1].

7 SUMMARY

This paper has detailed information on a through wafer via process that provides a reasonable and commercially viable solution to some of the inherent problems associated with MEMS (packaging and interconnect). It has also provided examples of some of the many features made possible through this new technology. The via process has now been in production at Silex since 2005 for applications ranging from advanced medical devices to mobile phones, and since mid 2006, Silex is offering this process as a standard MEMS foundry process.

To conclude this paper, key features characterizing Silex through silicon via process are listed below:

- High density via technology (pitch <50 µm)
- "No metal" starting material with unrestricted MEMS or CMOS post processing capability
- Enables true wafer level packaging of MEMS devices with vacuum sealing
- Low cost solution due to minimized component form factor and "all silicon package" for SMD assembly
- First through wafer via in volume production

REFERENCES

[1] Edvard Kälvesten, Thorbjörn Ebefors, Niklas Svedin, Pelle Rangsten, Tommy Schönberg, "Elektriska anslutningar i substrat / Electrical connections in substrates", Swedish Patent No. : 0300784. Several parallel International patent application publications (in English) e.g. WO2004084300 published 30.09.2004, as well as other patent applications within SILEX Via technology patent portfolio are available through different patent databases).