Process Aware Hybrid SPICE Models Based on TCAD and Silicon Data.

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ABSTRACT

This paper describes a methodology for extraction of process dependent SPICE compact model parameters. The extraction combines calibrated TCAD (Technology Computer-Aided Design) data and measured silicon data. Sensitivity of the transistor electrical performance is calculated using TCAD. The calculated sensitivity is put on top of the typical measured data. Such combined electrical performance data is used to extract SPICE model parameters as explicit functions of process parameters.

Keywords: process aware, SPICE models.

1 INTRODUCTION

Process variations play dominant role in determining the device behavior for deep sub-micron technologies. However, traditional SPICE model cards do not include explicit process variation related information. In order to capture process variations in SPICE models ([1] and [2]), the extraction requires electrical data for different process conditions. This is practically impossible to obtain from silicon data for the following two reasons.

First, it is impossible to fix all process conditions and vary just one of them. Instead, they all vary simultaneously, making the response very noisy. Second, random variations that are independent of the systematic process variations make their contribution to the data noise. Therefore, huge statistical sample has to be collected, making silicon data approach prohibitively expensive.

In this work we propose a methodology which allows extraction of process dependent SPICE model using typical silicon data for the nominal process conditions, combined with the TCAD data for process deviations from nominal.

2 METHODOLOGY

The strength of silicon data is that it exactly characterizes particular process when averaged on a large statistical sample. The weakness is that it is prohibitively expensive to measure transistor sensitivities to variations of the processing conditions like temperature, implant energy, etc.

The strength of TCAD simulations is that you can easily obtain transistor sensitivities to any processing conditions. The weakness is that it is difficult to exactly describe the nominal transistors from first principles due to the complexity of physical phenomena taking place during the manufacturing process. In other words, TCAD is good at describing trends and deviations from the nominal process flow, but often requires fine-tuning to accurately describe the nominal transistor behavior.

In this work, we combine the best of the two worlds, taking nominal transistor behavior from silicon measurements, and its process sensitivities from TCAD data, as is illustrated schematically on Fig. 1.

Let's refer to the data that is obtained this way as "pseudo silicon data". Pseudo silicon data is used to extract the process-dependent SPICE model cards using PARAMOS (process-dependent SPICE model extractor) [1].

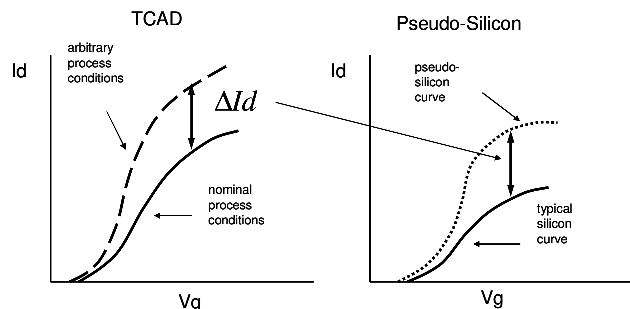

Figure 1: Generation of pseudo-silicon data

3 DATA GENERATION

Process and device simulations are performed for a generic 90 nm process using TSUPREM4 and Taurus Device. The nominal poly gate length is 65 nm. The simulations are done in 2-dimentional approximation, assuming logic applications with wide channels. A set of advanced physical models is used to accurately describe transistor sensitivities to the variations of processing conditions and geometry.

The process simulation accounts for all important effects, including pre-amorphizing implants, non-equilibrium impurity activation with carbon co-implants, transient-enhanced diffusion, and super-halo retrograde channel doping. The device simulation is based on a calibrated drift-diffusion carrier transport model and includes polysilicon gate depletion effect. The quantum

mechanical effects are considered both in the silicon channel and in the polysilicon gate.

Instead of the measured silicon data in this work we used data generated with SPICE BSIM4 model for a typical generic 90 nm transistor. The results obtained with this approach are very similar to the case where measured silicon data is used.

4 DATA SHIFTING

Data shifting has been used in a variety of different applications, including chemistry, spectroscopy, astronomy, and others, see for example [3]. In this section, we analyze application of such methods to SPICE models.

Data shifting procedure is a very important part of the proposed methodology. The basic idea is very simple: estimate the changes of drain current ΔId between nominal process condition and modified process condition using TCAD simulations. Then superpose this difference on top of silicon data to generate the pseudo-silicon data. Let's consider shifting procedure which is defined as:

$$Id_{pseudo} = Id_{silicon} + \Delta Id \tag{1}$$

Where $Id_{silicon}$ is measured drain current and Id_{pseudo} is pseudo-silicon drain current. However, a detailed consideration of generated pseudo-silicon curves shows limitations of approach (1). Whenever the ΔId is higher then the nominal drain current by a factor of two or more, which would often happen in the subthreshold region, the generated curves are smooth, but their first and second derivatives exhibit a multi-peak unphysical behavior, as shown for example in Fig 2.

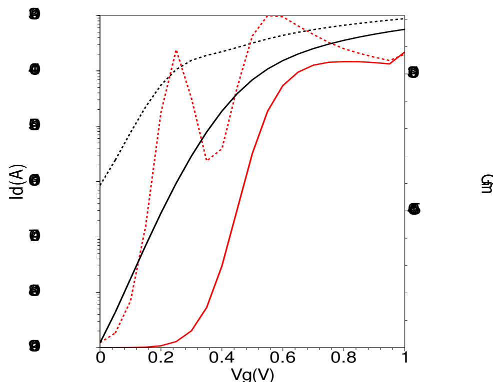

Figure 2: Unphysical Gm behavior, Black solid line – typical silicon IdVg curve, black dashed line – pseudo-silicon IdVg curve, red solid line – silicon Gm, red dashed line – pseudo-silicon Gm.

The second shifting procedure we have studied is defined as:

$$Id_{pseudo} = Id_{silicon} \times \left(1 + \frac{\Delta Id}{Id_{tcad}}\right) \tag{2}$$

As opposed to (1), which applies the absolute value of ΔId, the expression (2) utilizes the relative value of drain current change. Application of relative shifting (2) to transistor sensitivity analysis shows better local properties compared to the absolute shifting (1). Figure 3 illustrates acceptable behavior of both the shifter IdVg curve as well as the Gm curve that is derived from it.

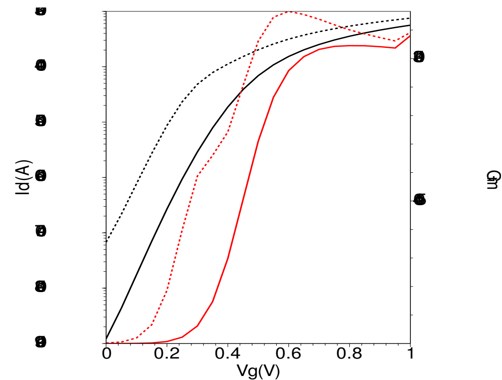

Figure 3: Accepteble Gm behavior, Black solid line – typical silicon IdVg curve, black dashed line – pseudo-silicon IdVg curve, red solid line – silicon Gm, red dashed line – pseudo-silicon Gm.

5 NUMERICAL EXPERIMENTS

In order to validate the proposed methodology, several numerical experiments have been performed. First, we obtain the pseudo-silicon data for the channel length variations in the range ±10 nm around nominal channel length, with IdVg curves shown in Fig. 4.

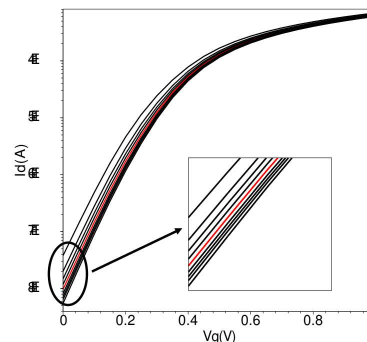

Figure 4: Pseudo-silicon IdVg curves for several channel lengths that are different by the same fixed increment. Red line – typical curve.

The depicted curves show good smooth behavior that provide the absence of unphysical trends of the first derivatives in contract to those shown in Fig. 2. Then the process-dependent BSIM4 model with only one process parameter, ΔL, was extracted using PARAMOS [2].

Similar exercise has been done with another process parameter, the halo implant dose. Figure 5 shows good behavior of pseudo-silicon curves in that case. We are paying most attention to the subthreshold region because of the difficulties to model this region. For example, Fig. 4 shows strongly non-linear Ioff dependence on L, whereas Fig. 5 demonstrated almost linear response of Ioff to the halo dose variation – this can be clearly seen on the inserts.

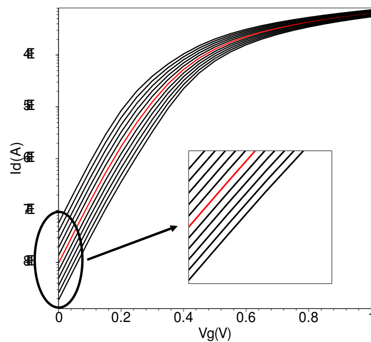

Figure 5: Pseudo-silicon IdVg curves for several halo implant doses that are different by the same fixed increment. Red line – typical curve.

The next step in our study is to construct a process-dependent SPICE model with two process parameters. Two previously obtained process-dependent model cards for the two different process conditions, ΔL and halo dose, have the following common properties: a) without process variations they represent silicon data; b) ΔL and halo dose as a process parameters are physically and statistically independent which leads to independency of process sensitivity coefficients in the two model cards. These properties allow us to combine independent process coefficients in one model card which is used later for predictive modeling.

Predictive modeling starting with TCAD simulations for classical DOE and two additional nodes, is schematically illustrated on Fig. 6. The black circles represent process conditions that are used to generate the model shown on Figs. 4 and 5. The data points shown as crosses did not participate in model generation, and are only used to verify the predictive power of the model.

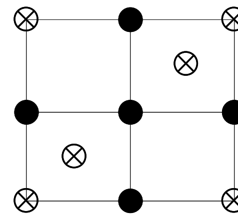

Figure 6: Prediction DOE.

The RMS error of the model that is built on the black reference points is about 2% in the entire range of terminal biases. When this model is used to predict the transistor behavior at the cross nodes that combine two variables changing simultaneously, the RMS is less than 8%. This accuracy is acceptable, taking into account more than 1000% range of the Ioff variation.

6 CONCLUSION

Extracted hybrid SPICE models contain model parameters that are functions of the relative process variations. These models are extracted from the pseudo-silicon data generated by estimating the process dependence of electrical transistor data using well calibrated TCAD data as well as silicon data. Whenever the relative process variations are forced to zero, the hybrid SPICE model reduces to the typical SPICE model card. Besides, for a given finite value of relative process variation, the SPICE model card accurately predicts the variation of silicon device behavior. This enables the circuit designer to estimate the impact of relative process variations on circuit performance.

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