SPICE Modeling of Hook Shaped Idsat Curve for I/O 2.5V MOS Transistors

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ABSTRACT

This paper demonstrates the modeling of hook shaped saturation drain current, Idsat versus transistor channel width curve by using the combination of two effects, a physical-based exponential factor in SPICE mobility parameter, u0 and the default SPICE delta width parameters. The physical-based exponential factor in u0 was derived based on the compressive STI y-stress (stress in the direction of channel width) for both NMOS and PMOS. The physical-based factor in u0 equation that we proposed is an exponential function of channel width with two new parameters (styu01 and styu02) for tweaking. The physical-based equation can be applied to all CMOS transistors that use the STI process for field isolation.

Keywords: STI stress, y-stress, hook shaped, MOS transistor, SPICE modeling.

1 INTRODUCTION

Mechanical STI stress has become a popular subject for sub-micron CMOS processes due to its effect of changing the effective mobility of electrons and holes. The STI stress effect is present in all STI isolation based CMOS processes.

The current standard SPICE models have included equations to model the effect of STI stress in the direction of channel length (x-stress). The STI x-stress model is a function of sa and sb (the distance between STI edge and gate edge) [1]. The STI x-stress model uses 21 parameters for tweaking. Since STI stress also compressing the channel width, the drain current of a transistor will also be affected.

From our studies in [2, 3], we found that when the saturation drain current (Idsat) of both NMOS and PMOS transistors are plotted versus channel width, W, the curve will first roll down at about W = 1um and then curves up at minimum width. This forms an Idsat curve that looks like a hook. We have shown that this hook shaped Idsat versus W curve is caused by the combination of the compressive STI y-stress (transverse stress in the direction of channel width) and delta width effect at narrow width [3]. The compressive STI y-stress causes mobility degradation for both NMOS and PMOS [4]. Delta width effect increases both NMOS and PMOS Idsat because of the extra delta width.

In the standard SPICE models, the delta width (DW) effect will raise the saturation drain current (Idsat) of narrow width transistors. We propose to add in the effect of compressive STI y-stress to u0 which will degrade the Idsat of narrow width transistors because of the reduction in mobility due to compressive y-stress. The combination of both the DW effect and the mobility degradation due to compressive STI stress will result in a hook shaped Idsat versus width curve as seen in the actual silicon measurement data, as shown in Figure 1.

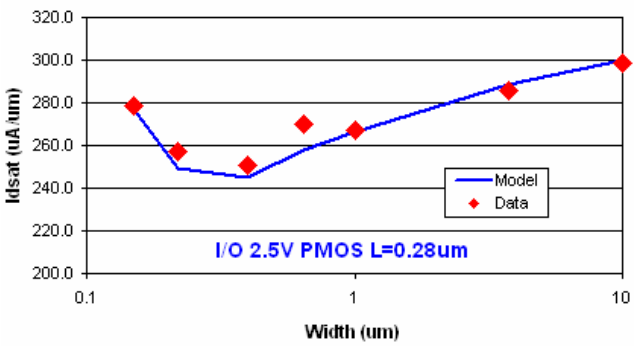

Figure 1: Actual silicon measured data showing a hook shaped Idsat vs Width curve.

We have demonstrated the hook shaped Idsat curve in our previous study in [2] and we have proposed an empirical SPICE model to capture the hook shaped Idsat curve in [5]. In paper [6], we have proposed a physical-based SPICE model to capture the hook shaped Idsat curve correctly and accurately. In this paper, we demonstrate that by applying the STI y-stress model that we proposed in [6], we can successfully model the hook shaped Idsat behavior of the I/O 2.5V transistors.

2 EXPERIMENT

The structures used in this experiment for I/O 2.5V thick oxide transistors are the standard modeling structures with different width, W and length, L. The thickness of the thick oxide is 4.6nm.

All the transistors are fabricated using Silterra's standard CL130G CMOS technology with 2.5V thick oxide transistors option. The minimum channel length is 0.28um. The linear threshold voltage (Vtlin) is extracted at Id = 0.1uA*(W/L) with Vd = 0.1V and Vs = Vb = 0V. Saturation drain current (Idsat) is extracted at Vg = Vd = 2.5V and Vs = Vb = 0V. The operating voltage (VDD) for the I/O transistor is 2.5V.

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3 SPICE MODELING

In the STI y-stress model, we added a physics-based exponential factor to the effective mobility of the SPICE model by using a macro model methodology. Our main purpose is to model the effect of mechanical STI stress in the direction of channel width. The exponential factor multiplies the SPICE mobility parameter, u0 and was derived based on the compressive STI stress effect in the direction of channel width (y-direction) on both NMOS and PMOS.

This physical-based exponential equation that we used is a function of channel width. It uses two parameters (styu01 and styu02) for tweaking. These two parameters are tweaked to model the hook shaped Idsat versus W curve accurately. The new exponential factor that we included in the effective mobility, u0_Effective is shown in Equation 1.

$$u0\_Effective = u0 * [1 - (styu01*\exp(-styu02*W))] \quad (1)$$

The hook shaped Idsat curve is formed due to the combination of compressive STI stress effect in the direction of channel width and delta width effect. Therefore, by tweaking both the STI y-stress parameters (styu01 and styu02) and the delta width parameter (wint), we can successfully model the hook shaped Idsat versus W curve.

4 RESULTS AND DISCUSSION

The I-V accuracy plots of the I/O 2.5V NMOS (Vtlin and Idsat versus W and L) are shown in Figure 2 to Figure 7 and Figure 8 to Figure 13 show the I/O 2.5V PMOS IV characteristics. There are basically three groups of devices; fixed W = 10um, fixed L = 10um and fixed L = 0.28um.

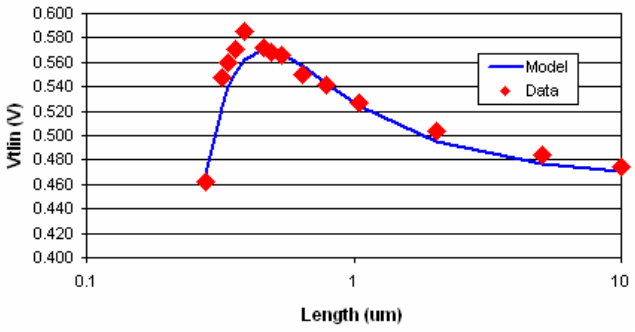

Figure 2: Accuracy plot of Vtlin versus L for I/O 2.5V NMOS at fixed W = 10um.

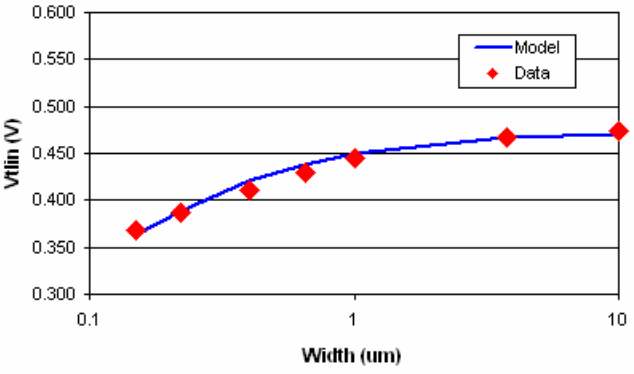

Figure 3: Accuracy plot of Vtlin versus W for I/O 2.5V NMOS at fixed L = 10um.

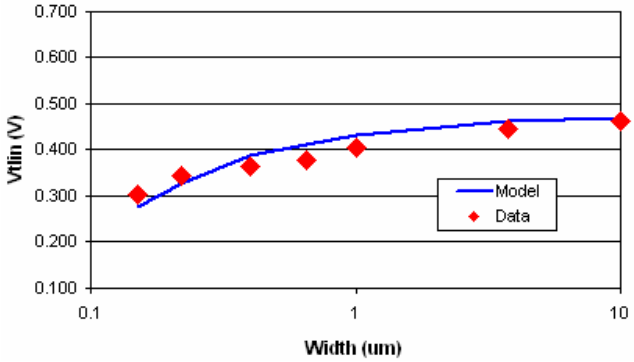

Figure 4: Accuracy plot of Vtlin versus W for I/O 2.5V NMOS at fixed Length = 0.28um.

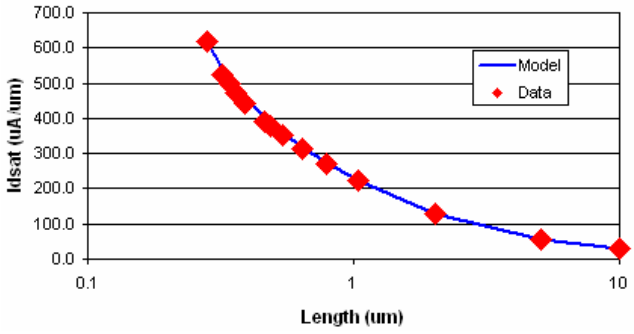

Figure 5: Accuracy plot of Idsat versus L for I/O 2.5V NMOS at fixed W = 10um.

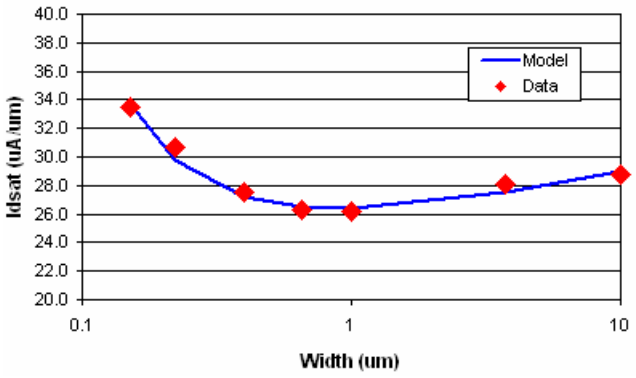

Figure 6: Accuracy plot of Idsat versus W for I/O 2.5V NMOS at fixed L = 10um.

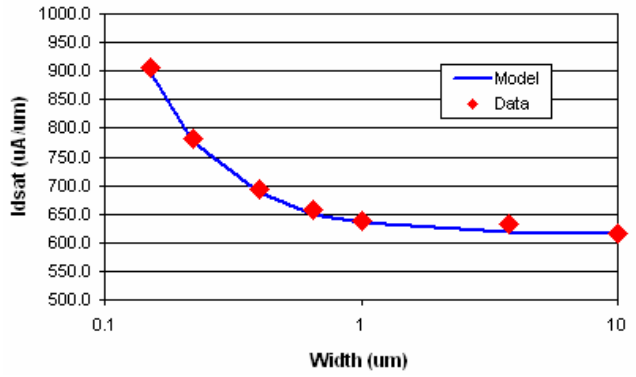

Figure 7: Accuracy plot of Idsat versus W for I/O 2.5V NMOS at fixed L = 0.28um.

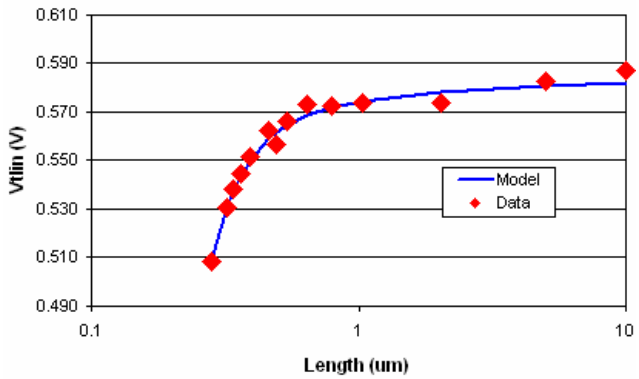

Figure 8: Accuracy plot of Vtlin versus L for I/O 2.5V PMOS at fixed W = 10um.

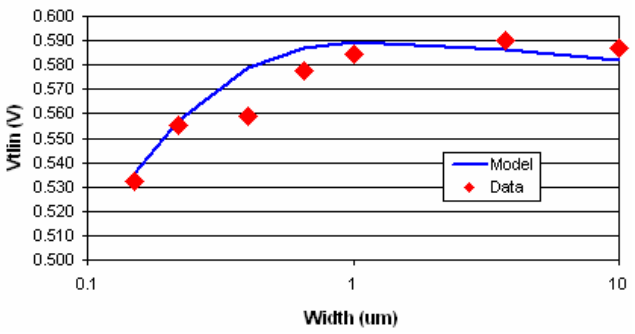

Figure 9: Accuracy plot of Vtlin versus W for I/O 2.5V PMOS at fixed L = 10um.

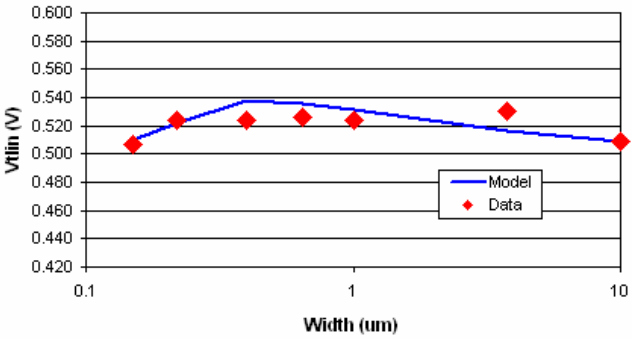

Figure 10: Accuracy plot of Vtlin versus W for I/O 2.5V PMOS at fixed Length = 0.28um.

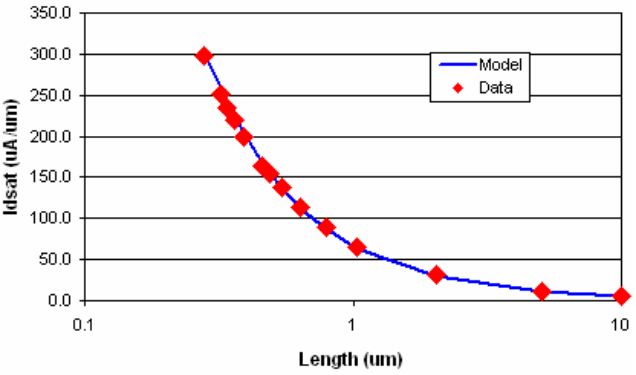

Figure 11: Accuracy plot of Idsat versus L for I/O 2.5V PMOS at fixed W = 10um.

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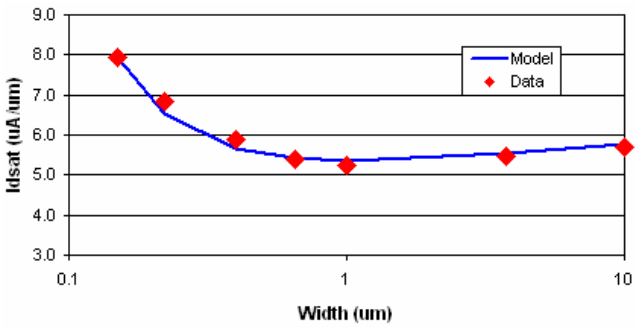

Figure 12: Accuracy plot of Idsat versus W for I/O 2.5V PMOS at fixed L = 10um.

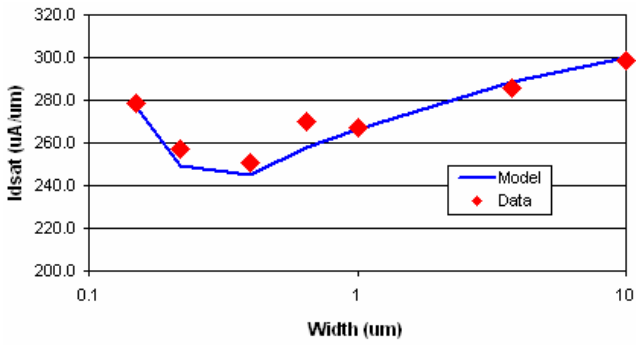

Figure 13: Accuracy plot of Idsat versus W for I/O 2.5V PMOS at fixed L = 0.28um.

Figure 6 and Figure 13 show the hook shaped Idsat curve of NMOS and PMOS transistors. For NMOS, the hook happens at long channel (L=10um) but for PMOS, the hook is more obvious at short channel (L=0.28um). Although, the hook occurs at different channel lengths for NMOS and PMOS, the physical-based mobility equation (Equation 1) still holds for both NMOS and PMOS without adding any L dependence into the equation.

5 CONCLUSION

In conclusion, we have demonstrated that by introducing a physics-based exponential factor to the effective mobility of the SPICE model, we can accurately model the I-V characteristics of the I/O 2.5V NMOS and PMOS transistors. The STI y-stress model that we proposed is a function of channel width with two parameters, styu01 and styu02 for tweaking. In comparison, the standard STI x-stress model is a function of sa and sb with 21 parameters for tweaking.

6 ACKNOWLEDGEMENTS

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