High Quality Nanogap Electrodes for Electronic Transport Measurements of Single Molecules

Danvers E. Johnston[*], Douglas R. Strachan[*], Beth S. Guiton[**], Peter K. Davies[**], Dawn A. Bonnell[**]
and
A.T. Charlie Johnson[*]

[*]University of Pennsylvania, Dept. of Physics and Astronomy
209 S 33rd St, Philadelphia, PA 19104, danvers@sas.upenn.edu
[**]University of Pennsylvania, Materials Science and Engineering
3231 Walnut St, Philadelphia, PA 19104

ABSTRACT

Electromigrated nanogaps have frequently been used in molecular scale electronics. We use a computer controlled electromigration (CCE) process for creating nanogaps at room temperature permitting characterization of bare gaps prior to application of molecules. This is very different from other approaches where nanogaps are formed by a simple voltage ramp performed at low temperature with molecules already attached to the nanowire. Using CCE, we formed nanogaps at room temperature on both thick substrates and thin SiN_x membranes compatible with transmission electron microscopy. We showed that the electromigration process evolves through an initial bulk behavior regime and crosses over to a ballistic conduction regime. It was found that nanogaps formed on SiN_x membranes are clean of parasitic conduction pathways and contamination. This work has implications to the design of clean metallic electrodes for use in nanoscale devices.

Keywords: nanogap, electromigration, molecular electronics

1 INTRODUCTION

Single molecule-based electronic devices hold the potential for higher density and higher performance applications over a broad range of fields including sensing, computing and photovoltaics. Experimentally, metal-molecule-metal (MMM) or metal-nanoparticle-metal junctions offer a direct route to measuring electronic properties of nanoscale objects in a three probe geometry.[1] Over the past several years, a body of literature has emerged on single molecule nanogap transistors formed at low temperature by electromigration of a nanoscale metal wire in the presence of a sub-monolayer of molecules on a thick insulating substrate.[2,3] Data from the resulting devices have been interpreted under the assumption that they consist of a single MMM junction capacitively coupled to a nearby gate electrode. At present, a major concern is that the electronic behavior of a device may be due to transport via nano-scale metal particles that form in the nanogap region during electromigration rather than the molecular species under study.[4]

A method of forming nanogaps in gold wires at room temperature is therefore desirable because the bare gap can be studied and characterized prior to the application of the molecular species.[5] This goal is achieved using CCE. Additionally, nanogaps formed at room temperature using CCE on transparent SiN_x membranes are compatible with transmission electron microscopy (TEM) for high resolution visual inspection.[6] Using TEM we verify that our process produces nanogaps that are clean of residual contamination and metal nano-cluster parasitic conduction pathways that can spoil the nanogap.

2 MATERIALS AND METHODS

2.1 Sample Fabrication

Samples were fabricated using electron beam lithography (JEOL USA, Inc. 6400 scanning electron microscope with Raith GmbH ELPHY Plus) followed by angle evaporation of Cr and Au and, finally, liftoff to create a narrow gold wire as described in ref. 1. The substrate is B doped Si with 100 nm of polished thermal oxide. The substrate thickness is ~ 500 μm which promotes substantial backscatter and secondary electron emission during electron beam irradiation for enhanced undercutting of dual electron beam resist layers. The top layer is polymer, polymethyl-methacrylate (PMMA), dissolved in chlorobenzene (MicroChem Corp. 950PMMA C2) approximately 100 nm thick and the bottom layer is copolymer, a mixture of PMMA and ~8.5% methacrylic acid dissolved in ethyl lactate (MicroChem Corp. EL9) several hundreds of nanometers thick. The underlying copolymer layer is initially applied by spinning at 1500 rpm for 65 sec followed by pre-baking on a hot plate at 180°C for 2 minutes. The PMMA layer is applied by spinning at 6000 rpm for 45 sec and pre-baking for 2 minutes at 180°C. The PMMA resist layer requires more electron beam irradiation to break cross-linked bonds than the underlying copolymer causing a narrow resist bridge to remain after patterning and developing. A weak developer made of a 3:1

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061828 Vol. 1, 2007

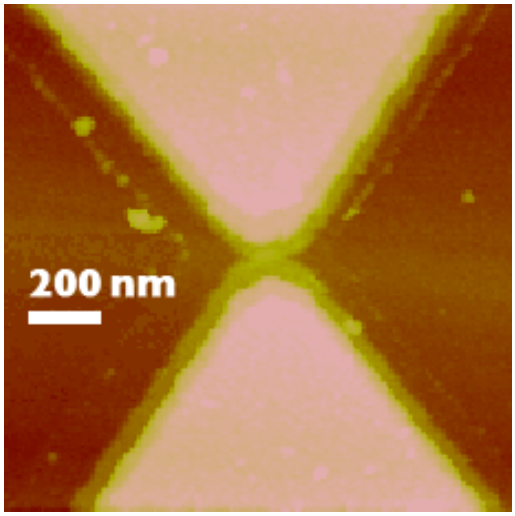

Figure 1. Atomic force microscope image of a narrow Au wire designed for electromigration. Brightly colored regions are 60 nm in height and the thinner central region is about 20 nm in height.

mixture of isopropanol and methyl isobutyl ketone is used to remove the exposed resist.

A metal film is deposited underneath the suspended resist bridge by angle evaporation of Cr and Au in a thermal evaporator with a base pressure between 10^{-7} to 10^{-6} Torr. The deposition process begins with 3 nm of Cr deposited normal to the substrate. The substrate is then tilted ±11° and 12 nm of Au is deposited under the resist bridge to form a continuous Au wire. Finally, 30 nm of Au is deposited perpendicular to the plane of the substrate to reduce the total resistance of the source and drain leads while the resist bridge prevents a thick layer of Au from accumulating at the junction of the two overlapping 12 nm Au layers. This is the location where we want a nanogap to form. Figure 1 shows an atomic force microscope image illustrating the device geometry and deposited metal thicknesses.

2.2 Experimental Setup

Controlling a steady rate of electromigration requires continuously measuring resistance in order to detect changes and then incrementally stepping the applied voltage appropriately depending on the magnitude and sign of the change in resistance. Figure 2 is a diagram of the connections between the components in the setup used for CCE. Feedback is controlled by a computer running the LabVIEW virtual instrument (VI) described in section 3. The VI controls the output voltage of a digital to analog conversion (DAC) peripheral component interconnect (PCI) card (National Instruments 16 bit PCI DAQ) connected to a current buffer (Op Amp). The current-proportional analog voltage output (±2 V) from the ammeter (Keithley Instruments, Inc. 6517A Electrometer) is read by an analog to digital conversion (ADC) PCI card (National Instruments

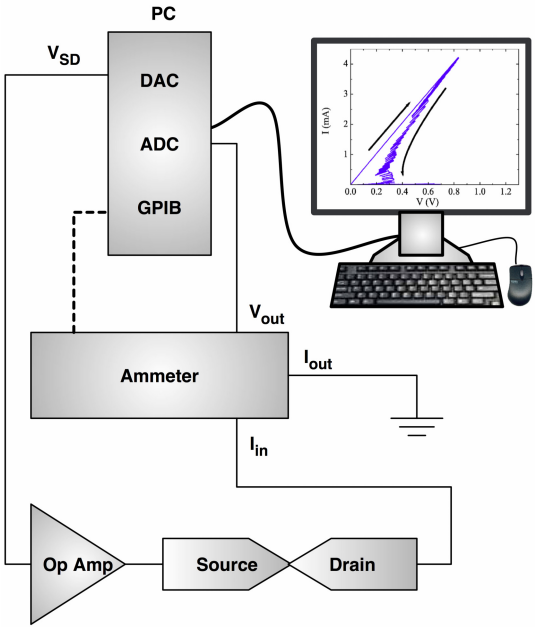

Figure 2. Diagram of the experimental setup for CCE of the junction between source and drain electrodes. Prior to electromigration, a 100 nm wide by 20 nm thick Au film connects the source and drain.

16 bit PCI DAQ) to monitor the current flowing through the sample in real time.

The measurement scheme used in this experiment does not use general purpose interface bus (GPIB) communication aside from a one-time instrument initialization step. GPIB is inherently slow in applications that require frequent short reads and writes to instruments due to a first-bit latency of 100 µs. In comparison, the DAQ cards we use have between 10 to 100 ns first-bit latencies over PCI interface.[7]

3 COMPUTER CONTROLLED ELECTROMIGRATION

Formation of nanogaps at room temperature requires CCE because an uncontrolled ramp in voltage at room temperature results in larger gap sizes of order 100 nm and promotes metal particle formation. We use a controlled feedback algorithm to simultaneously monitor the resistance of the narrow Au wire (the "neck") and to adjust the source voltage (V). The algorithm implemented in LabVIEW is designed to mimic as closely as possible how a person would intuitively adjust the voltage if it were possible to turn a voltage knob while simultaneously observing the sample resistance ($R \equiv V/I$). Increasing voltage increases current flow as $I = V/R$ with $R \approx$ const. until the wire fails and current drops to zero (at which point $R \to \infty$) due to opening of a gap in the wire. Classical physical quantities change continuously and, indeed, as the

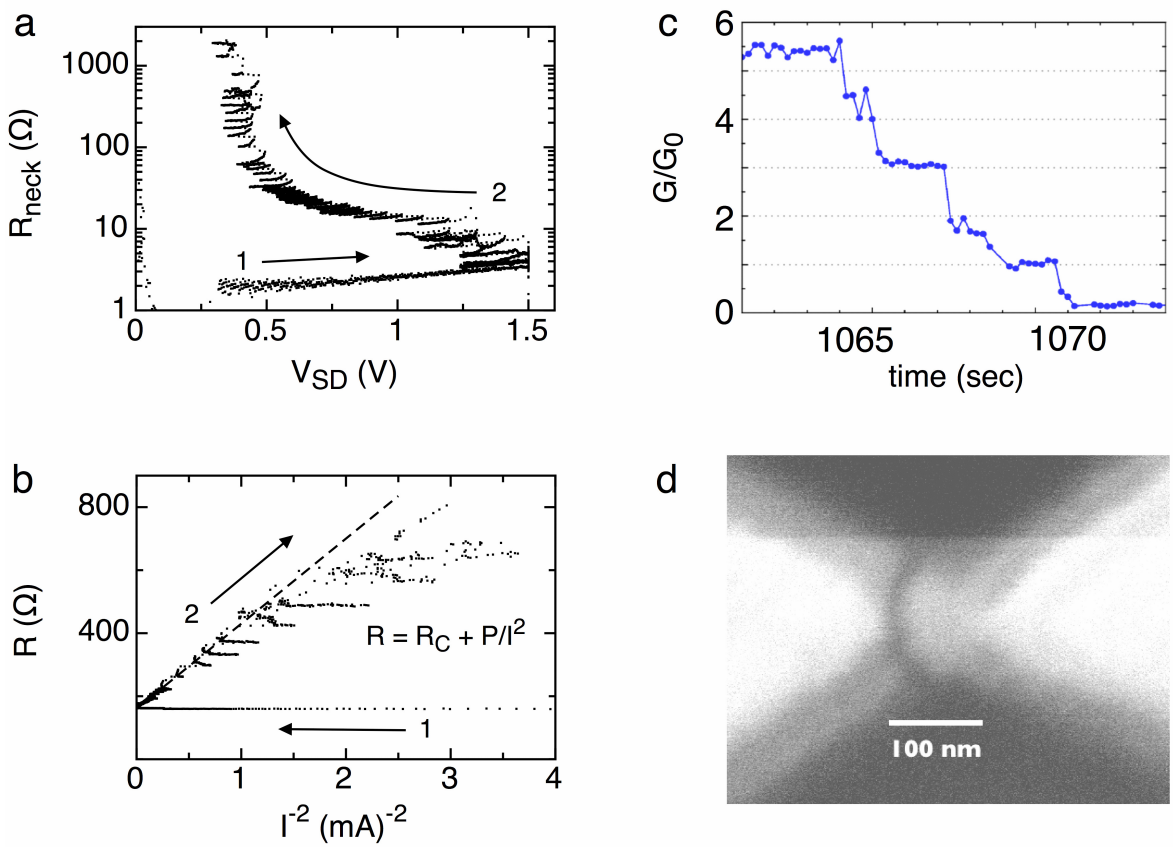

Figure 3. CCE electrical data and SEM image. (a) R_{neck}–V during CCE. (b) The same data plotted in a way which stresses the validity of a constant-power model at low resistances when the neck behaves as a bulk conductor. As R approaches 1 kΩ the behavior deviates from bulk behavior. (c) Quantum of conductance jumps are observed as the gap evolves under a constant V = 89 mV bias when only a few Au atoms are connecting the electrodes. (d) SEM image of the Au neck after CCE.

resistance goes from finite to infinite, R goes through intermediate values of resistance. At sufficiently high current, R increases due to electromigration of Au in the wire. Electromigration proceeds catastrophically unless we rapidly decrease V. By repeatedly increasing V and quickly reducing it when breaking occurs we obtain nearly continuous control over the increase in the resistance of the wire as long as we are in the bulk behavior regime.[5] This increase in resistance corresponds initially to narrowing of the wire due to Au electromigration away from the neck region. Figure 3 shows typical data of CCE in a gold wire during nanogap formation. A controlled increase in resistance from roughly 100 Ω to 1 kΩ requires approximately 5 minutes and is highly reproducible across many samples.

The shape of the I–V curve during CCE is identical for all samples tested and reliably fits a constant-power model with two parameters. Assuming that electromigration occurs at an appreciable rate only when the quantity $P = I^2R_{neck}$ reaches a constant value, Ohm's law, $V = IR$, predicts the relationship

$$R = R_l + P/I^2 \quad (1)$$

where R_l is the lead resistance ($R_l \equiv R - R_{neck}$). In Figure 3b equation 1 is used to fit the data with P = 270 μW and R_l = 160 Ω. The conduction immediately prior to nanogap formation is plotted as a function of time in Figure 3c. We notice ballistic conduction channels each contributing $G_0 \equiv 2e^2/h$, where e is the charge of an electron and h is Planck's constant. Figure 3d shows a scanning electron microscope (SEM) image of an Au neck after electromigration. The distance of closest approach between the left and the right electrodes cannot be resolved due to limited resolution of the SEM, however it is expected to be on the order of a few nanometers because a finite tunneling resistance remains after stopping the CCE.

4 HIGH RESOLUTION IMAGING

We have adapted the computer controlled electromigration process to create nanogaps on electron transparent SiN_x membranes less than 100 nm thick for

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061828 Vol. 1, 2007

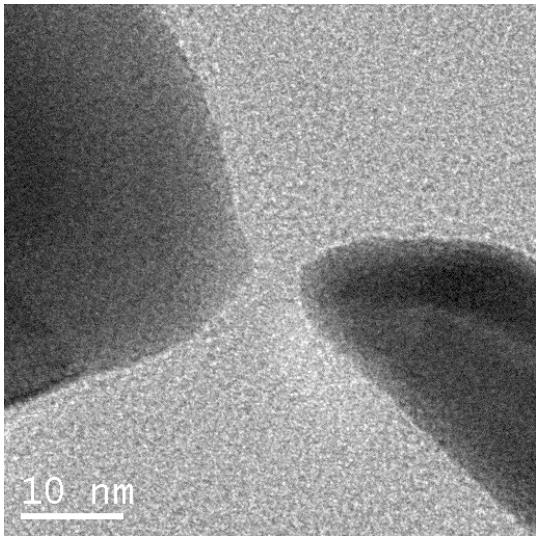

Figure 4. TEM image of a nanogap in an Au nanowire formed by computer controlled electromigration on an electron transparent SiN_x membrane. The nanogap size is approximately 4 nm.

transmission electron microscope imaging.[6] Samples were prepared in a similar way to those made on SiO_2 substrates but without angle evaporation because an undercut resist bridge does not form on thin membranes due to decreased backscattering. Use of an adhesion layer is omitted during device fabrication on SiN_x membranes.

TEM (JEOL Ltd. JEM-2010F) imaging reveals that electromigrated Au electrodes consistently snap to a smallest gap size of approximately 4 nm and provides detailed information on the geometry of the nanogap. Figure 4 clearly shows that nanogaps formed in Au wires on SiN_x by CCE are clean of all contaminating factors of diameter greater than roughly ~ 0.5 nm.

5 CONCLUSIONS

We developed a room temperature computer controlled electromigration process employing fast electronics. This process was used to form stable nanogaps in Au wires on both thick substrates and thin membranes compatible with TEM.

A constant-power model fits the electromigration data as it proceeds through an initial bulk behavior regime. The electromigration process then crosses over to a ballistic conduction regime where the constant-power model breaks down and quantum conductance channels are observed.

Nanogaps formed on transparent SiN_x membranes were successfully imaged using TEM. The ability to inspect nanogaps with high resolution microscopy is particularly important because we verified the absence of metal nano-clusters or other contamination in nanogaps formed using our CCE process. Therefore, bare nanogaps formed using CCE at room temperature provide a useful test bed for further molecular electronics experiments in which the bare gap contribution to the behavior of the metal-molecule-metal system is well understood.

6 ACKNOWLEDGMENT

This work was supported through NSF-NIRT Grant No. 0304531 and MRSEC-NSF Grant No. DMR-00-79909. D.E.J. acknowledges financial support from NSF IGERT program (Grant No. DGE-0221664d) and SENS.

REFERENCES

[1] H. Park, A. K. L. Lim, A. P. Alivisatos et al., Appl. Phys. Lett. 75 301-303 (1999)
[2] W. J. Liang, M. P. Shores, M. Bockrath et al., Nature 417, 725-729 (2002)
[3] J. Park, A. N. Pasupathy, J. I. Goldsmith et al., Nature 417, 722-725 (2002)
[4] A. A. Houck, J. Labaziewicz, E. K. Chan et al., Nano Lett. 5, 1685-1688 (2005)
[5] D. R. Strachan, D. E. Smith, D. E. Johnston et al., Appl. Phys. Lett. 86 043109 (2005)
[6] D. R. Strachan, D. E. Smith, M. D. Fischbein, D. E. Johnston et al., Nano Lett. 6 441-444 (2006)
[7] http://zone.ni.com Eight Ways to Increase GPIB System Performance – Tutorial – Development Library – National Instruments