Carbon Nanotube Transistors with 60mV/decade Switching and its Capacitance Measurement

Yuerui Lu*, Hongjie Dai** and Yoshio Nishi***

* Physics Department, Stanford University, Stanford, CA 94305, USA, yueruilu@stanford.edu
** Department of Chemistry and Laboratory for Advanced Materials, Stanford University, Stanford, CA 94305, USA, hdai@stanford.edu
*** Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA, nishiy@stanford.edu,

ABSTRACT

Recently, we have been able to approach the ultimate vertical scaling limit of carbon nanotube field effect transistors (FETs) and reliably achieve S ~ 60 mV/decade at room temperature, by non-covalent functionalization of single walled carbon nonotubes (SWNTs) with ploy-T DNA molecules, which can impart functional groups of sufficient density and stability for uniform and conformal ALD of high-κ dielectrics (HfO_2) with thickness down to 3 nm on SWNTs. Moreover, the small top gate stack capacitance (~300aF/ μ m) of the SWNT FET has been successfully measured directly, using a special technique. The mobility of the SWNT FETs at room temperature is also extracted by the capacitance measured directly.

Keywords: carbon nanotube, FET, 60mV/decade, capacitance, mobility

1 INTRODUCTION

SWNT field effect transistors (FETs) outperform state-of-the-art Si FETs owing to near ballistic electrical transport, chemical robustness, lack of surface dangling bonds and sustained electrical properties when integrated into realistic device structures [1-7]. One of the goals of transistor down-scaling is to obtain low subthreshold swing S approaching the theoretical limit of 60mV/decade for device operations at low voltages and power dissipations.

On the device application side, relatively thick films (~8nm) of high-κ materials (ZrO_2 and HfO_2, κ~15-25)[4] have been used for SWNT FETs. Recently, we developed non- covalent functionalized SWNTs with ploy-T DNA molecules (dT40) for uniform and conformal atomic layer deposition (ALD) of high-κ dielectrics on SWNTs with thickness down to 3 nm (Fig.1a, 1b) [1].

High mobility is also another key advantage for SWNT FETs. The extraction of hole mobility from the capacitance measured directly for p-SWNT FETs is also achieved.

2 DEVICE FABRICATION

SWNTs were grown by chemical vapor deposition on SiO_2/Si substrate from an array of patterned catalyst sites [8]. The substrates were prepared by wet thermal oxidation of heavily doped p-type Si wafers at 1000 ºC to afford 100nm thermal SiO2. Small diameter semi-conducting SWNTs (d<1.5nm, measured by atomic force microscopy) were chosen for device fabrication in the current work. The small diameter tubes have large band-gaps and can afford higher on/off ratios for SWNT FETs. Source(S) and drain(D) electrodes (distance between opposing edges of S/D was 3 micron) were fabricated by electron beam lithography (EBL) patterning of PMMA spun on the substrate, development of the EBL exposed S/D regions, 0.5nm Ti/20nm Au deposition by electron beam evaporation, and then liftoff of PMMA in acetone. The chip

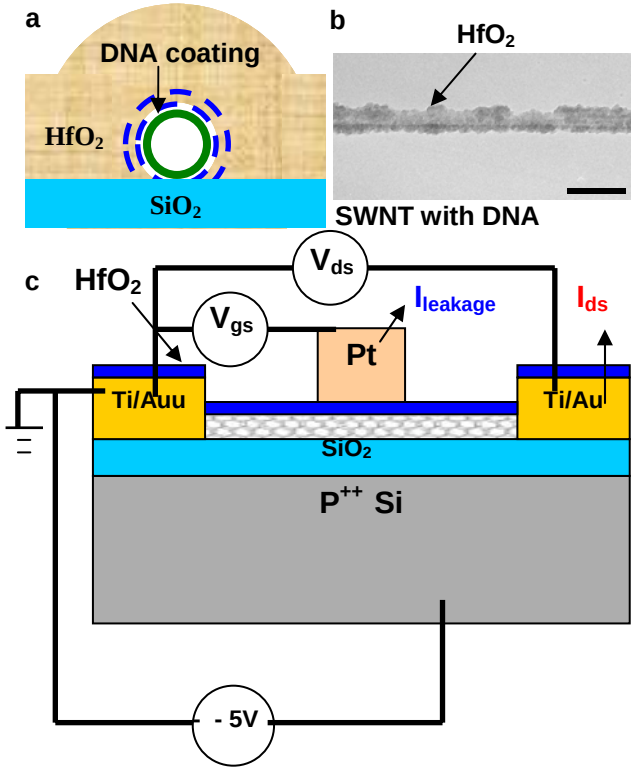

Figure 1: a) A schematic of conformal HfO_2 coating on a DNA functionalized SWNT. (b) A TEM image. (c) Schematic of side view of the device and its probing measurement set up.

was annealed in argon at 300ºC for 10min to improve the contacts between the SWNTs and the S/D metal. For DNA functionalization of the SWNT segments between the S/D electrode pairs, an oligonucleotide consisting of 40 thymine residues (dT40, Stanford PAN Facility) was used. The SWNT device chip was placed and nutated in a 10 μM dT40 S 2 DNA water solution for 30min, followed by 2-min gentle sonication of the chip in pure water and then rinsing and drying under a nitrogen stream. ALD of HfO_2 on the chip was carried out at 90ºC using tetrakis (dimethylamido) hafnium(IV), Hf(N(CH3)2)4 (Sigma-Aldrich) and H_2O vapor as precursors. For each cycle of ALD, the H_2O vapor pulse was 0.5s in duration, followed by a 360s purging time, a 2s Hf-precursor pulse and then a 120s purging time. The deposition rate under such ALD condition was ~ 0.13nm per cycle. After the ALD step, top-gate (Pt) under-lapping the S/D (gate length ranging from 100nm to 1 μ m) was formed by EBL patterning of PMMA, Pt (18nm) metal evaporation and lift off in acetone.

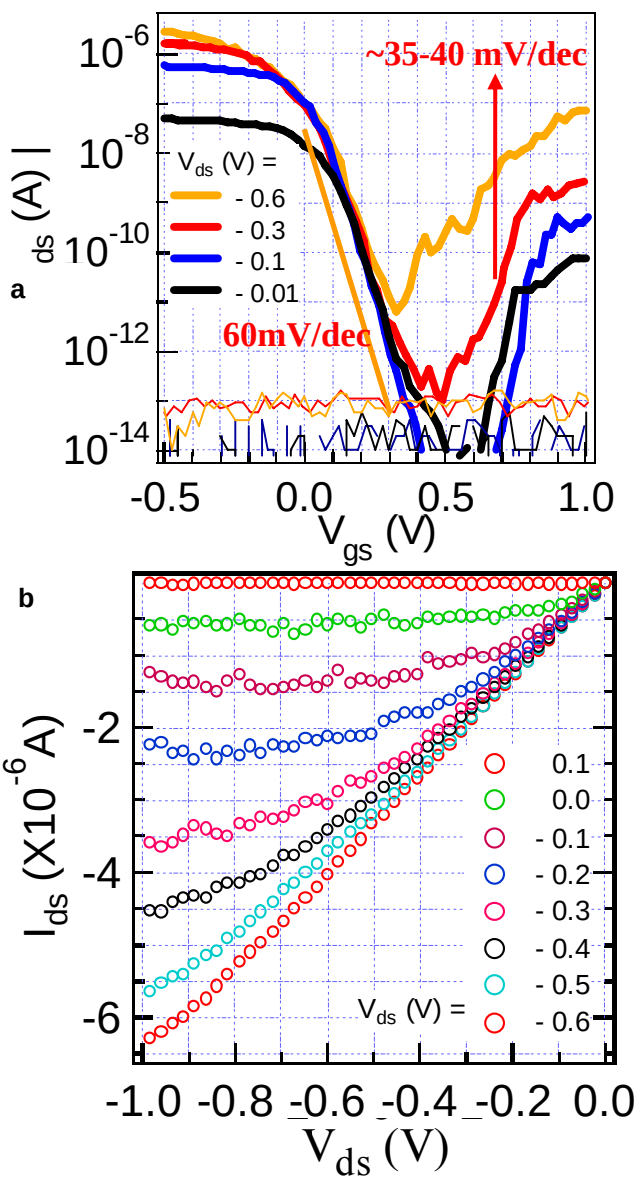

Figure 2: A DNA-functionalized SWNT-FET with ~3nm high κ gate dielectrics. (a) Current vs. top-gate voltage (I_{ds}-V_{gs}) curves of the device in Fig.1c recorded at various bias (V_{ds}) indicated. Top-gate leakage currents (bottom traces) under various V_{ds} during V_{gs} sweeps are negligible. (b) Source-drain current-bias (I_{ds}-V_{ds}) characteristics of the device recorded at various top-gate V indicated.

3 DEVICE PERFORMANCE

Here, we show that by non-covalent functionalization of SWNTs with ploy-T DNA molecules (dT40, Fig.1a), one can impart functional groups of sufficient density and stability for uniform and conformal ALD of high κ dielectrics on SWNTs with thickness down to 3nm (Fig.1b). This enables us approaching the ultimate vertical scaling limit of nanotube FETs and reliably achieving S ~ 60mV/decade at room temperature. Without DNA functionalization, severe gate leakage and shorts were observed for most of SWNT FETs with high κ thickness $t_{ox} \leq$ 5nm. With DNA functionalization, high performance nanotube-high κ FETs free of gate-leakage currents were reliably obtained with HfO_2 t_{ox} ~3nm (Fig.2, diameter of SWNT d~1.4nm). All of our t_{ox}=3nm DNA functionalized SWNT FETs reproducibly reached theoretical limit of S ~ 60mV/decade at 300K (Fig.2a) and high transconductance of 5000 Sm^{-1} (Fig.2b). For our SWNT FETs with underlapping top-gate, the subthreshold swing S is due to thermally activated on/off switching and $S= \ln(10)[dV_{gs}/d(\ln I_{ds})] = (k_BT/e)\ln(10)(1+\alpha)$, where k_B is the Boltzmann constant, and α depends on various capacitances in the device. The fact that we are reaching the theoretical limit of $S=(k_BT/e)\ln(10) \approx 60$ mV/ decade at 300Ksuggests $\alpha \sim 0$ and that the gate capacitance is much higher than other capacitances in the device. For 3nm HfO_2, the gate dielectric capacitance per unit length is $C_{OX} \sim 2\pi\varepsilon_0\varepsilon/\ln(2t_{ox}/R) \sim$ 6pF/cm, where $\varepsilon \sim 25$ for HfO_2 and R is the radius of the SWNT. This exceeds that of the quantum capacitance $C_{QM} \sim$ 4pF/cm of SWNTs resulted from the finite density of states in the nanotube electronic structure. Thus, with t_{ox} = 3nm HfO_2 gate dielectrics, we are well into a regime where the total gate capacitance of a SWNT FET is dominant by C_{QM} [1].

Notably, with non-covalent DNA functionalization, we observed no degradation in the SWNT FET conductance after the functionalization and subsequent ALD. The hysteresis is pretty small, near zero, which indicates that the DNA molecule will not give a negative effect to the performance of the device.

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061828 Vol. 1, 2007

From n-channel of the I_{ds}-V_{gs} curve of the device (Fig.2a), 35~40mV/dec switching could be achieved, which is due to band to band tunneling (BTBT) [10].

Vertical scaling of high κ dielectrics for SWNT FETs below the t_{ox}~4 -5nm scale affords no further enhancement in transistor switching once S~60mV/decade and quantum capacitance are reached. Nevertheless, such scaling is useful for investigating interesting device physics in quasi-1D systems such as electron tunneling. In a 1D channel, electrostatics is dependent on the gate dielectric thickness and widths of tunnel barriers (Schottky, band-to-band tunneling BTBT[10]etc) are often set by t_{ox}.

The n-channel currents are due to BTBT and a thinner high-κ affords sharper band bending at the edges of the top-gate by the gate potential, thus giving rise to a smaller BTBT width and higher tunnel current. It is proposed recently that BTBT may be utilized to obtain tunnel transistors [10-11]with S beating the 60mV/decade limit of conventional FETs. The ultra-thin high κ described here should be desirable for such devices.

Thus, non-covalent functionalization can used to enable ultra-thin dielectrics for advanced nanotube electronics.

4 CAPACITANCE MEASUREMENT

Capacitances of the SWNT FETs were measured at room temperature, using a capacitance bridge with a sensitivity of 50e/$\sqrt{Hz}$ and long averaging times at 1kHz.

The parasitic capacitance between the top-gate and source (or drain) electrodes is shielded by a nearby back gate, with thin 100nm thermal SiO_2. Direct capacitive coupling between the wiring and probing tips is eliminated by using a grounded copper plate positioned between the S/D and G probe tips, which reduces background capacitance from ~10fF to ~30aF. In order to get enough space for the copper plate be positioned between the probing tips, we made the probing pads to be far away, around 2 μm away.

When the device is turned on, we could measure the total capacitance to be around 350aF, while the background capacitance could be measured when the tube bridging the S and D is burned (disconnected). Then we could get the top-gate capacitance C_{gs} to be 320aF, by reducing the background capacitance (around 30aF) from the total capacitance.

In the low-bias linear-triode regions of the I_{ds}–V_{ds} curves (Fig.2b), the hole mobility μ_h can be deduced from $g_{ds}=I_{ds}/V_{ds}=2K(V_{gs}-V_T)$, where g_{ds} is the zero bias conductance, K is the conductivity parameter given by $K = \mu_h C_{gs}/2L^2$, and $V_T = 0.1$V is the threshold gate voltage for the device. We could get $\mu_h \sim 2{,}500$ cm^2 V^{-1} s^{-1}. This is the first time to extract mobility for SWNT FETs, using capacitance measured directly.

5 CONCLUSION

We have been able to approach the ultimate vertical scaling limit of carbon nanotube field effect transistors (FETs) and reliably achieve S ~ 60 mV/decade at room temperature, by non-covalent functionalization of single walled carbon nonotubes (SWNTs) with ploy-T DNA molecules, which can impart functional groups of sufficient density and stability for uniform and conformal ALD of high-κ dielectrics (HfO_2) with thickness down to 3 nm on SWNTs. Moreover, the small top gate stack capacitance (~300aF/ μ m) of the SWNT FET has been successfully measured directly, using a special technique. The mobility of the SWNT FETs at room temperature is also extracted by the capacitance measured directly for the first time.

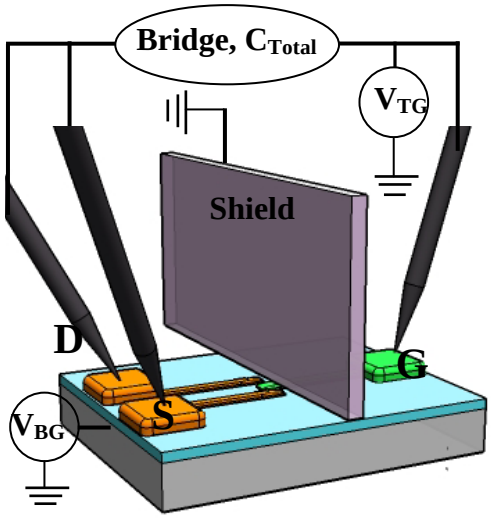

Figure 3: A schematic illustration of the capacitance measurement setup. A grounded copper plate is positioned between the source (S) /drain (D) and gate (G) probe tips, which reduces background capacitance from ~10fF to ~30aF, allowing for accurate measurement of small gate-capacitances of the SWNT FET.

REFERENCES

[1] Y. Lu, et al., J. Am. Chem. Soc. **128**, 3518, 2006.

[2] Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. Nano Lett. 4, 1319, 2004.

[3] Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. Nature, 424, 654, 2003.

[4] Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. Nature Materials, 1, 241, 2002.

[5] Rosenblatt, S.; Yaish, Y.; Park, J.; Gore, J.; Sazonova, V.; McEuen, P. L. Nano Lett. 2, 869, 2002.

[6] Lin, Y. M.; Appenzeller, J.; Knoch, J.; Avouris, P. IEEE Trans. Nanotechnology, 4, 481, 2005.

[7] Durkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. Nano Lett., 4, 35, 2004.
[8] Kong, J.; Soh, H.; Cassell, A.; Quate, C. F.; Dai, H. Nature, 395, 878, 1998.
[9] Zhou, C.; Kong, J.; Yenilmez, E.; Dai, H. Science, 290, 1552, 2000.
[10] Appenzeller, J.; Lin, Y. M.; Knoch, J.; Chen, Z. H.; Avouris, P. IEEE Trans. Elec. Dev., 52, 2568, 2005.
[11] Guo, J.; Wang, J.; Polizzi, E.; Datta, S.; Lundstrom, M. IEEE Trans. Nanotech., 2, 329, 2003.