1/f Noise and RTS(Random Telegraph Signals) and Read Errors in Nanoscale Memories

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ABSTRACT

Noise signals can be equivalently represented in either the frequency domain or the time domain. The representation or modeling in the frequency domain gives the mean square noise current of a transistor as a function of frequency. The representation or modeling of the RTS or l/f noise of nanoscale devices that is easiest to understand is that done in the time domain. The capture and emission of a single electron in a nanoscale NMOS transistor will be equivalent to a change in threshold voltage. Modern devices are now small enough that we can see RTS noise signals associated with single electron trapping. This electron trapping is equivalent to the electron trapping on nanocrystals in nanoscale memories and can cause data errors.

Keywords: nanoscale memories, random telegraph signals, noise, l/f noise, single electron noise, bit error rate

1 INTRODUCTION

The use of charge storage on nanoscale particles, Fig. 1, has been realized in silicon integrated circuit memories [1,2] and utilized in commercial products[2]. An analysis has previously been made of the increasing portion of the threshold voltage being occupied by thermal noise levels and the bit error rates in digital logic and memory circuits [3-6]. This analysis has led to the prediction that there are fundamental limits imposed in digital circuits by thermal noise and that the scaling predicted by Moore's law can not continue into the future.

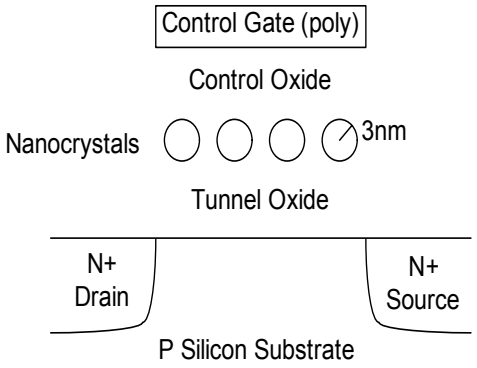

Fig. 1 Nanoscale silicon memory device with nanocrystals for charge storage embedded in the gate insulator.

No consideration was, however, given to the errors that might be caused by l/f noise or random telegraph signals. In small transistors such as used in read sense amplifiers the l/f noise is caused by and can be characterized by random telegraph signals(RTS). These random signals can cause errors in the sense amplifiers and limit the ability to read the data stored in nanoscale memories. These noise signals can be equivalently represented in either the frequency domain or the time domain, Fig. 2 .

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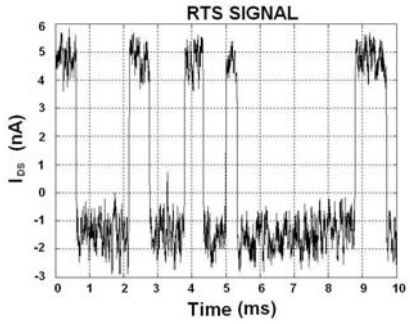
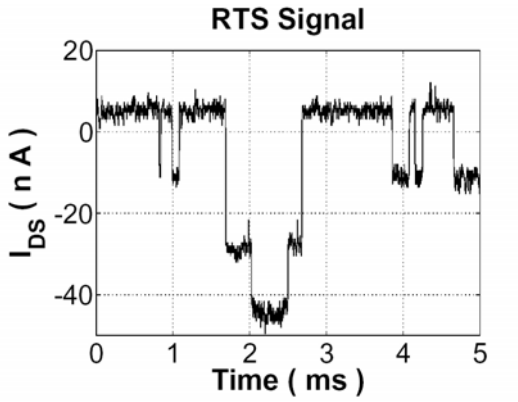
2 RTS ON NANOSCALE DEVICE

Fig. 2 illustrates the measured RTS noise in a submicron or nanoscale size MOSFET due to single electron and multiple electron traps.



(a) Single electron trapping in a nanoscale silicon transistor.



(b) Multiple electron trapping events in a nanoscale silicon transistor.

Fig. 2 Electron trapping in nanoscale transistors.

Each of the changes or steps in the drain current of the transistor in Fig. 2 corresponds to the emission or capture of a single electron, The transistors are biased at a normal level of drain current employed in circuit applications and they are operated in the saturation region.

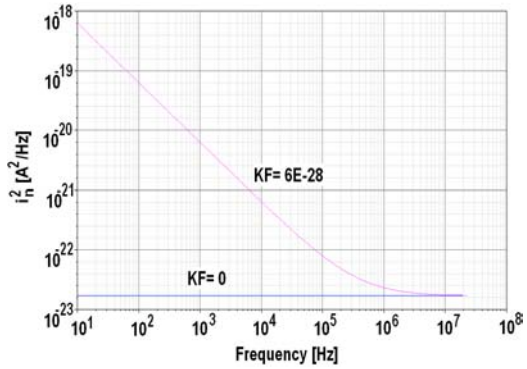


Fig. 3 l/f noise in the frequency domain resulting from a combination of many different single electron events with different time constants.

3 RTS IN READING DEVICE

The mean square noise of the read transistor is

$$I^2 = KF\ \mu\ W\ (Vgs\text{-}Vt)^2 / (2\ L^3\ f) \qquad (1)$$

where, KF is the l/f noise parameter, L the length and W the width of the transistor channel, μ the mobility and (Vgs-Vt) the excess of gate voltage above threshold. The charge read error of a sense amplifer transistor, Fig. 4, can be expressed as

$$\Delta I\ \Delta t = ((KF\ W\ \mu / 2\ L^3)\ (\ln (fh/fl)))^{1/2} (Vgs\text{-}Vt)\Delta t \qquad (2)$$

where, fl and fh the low and high frequency bandwidth limits. Δt is the read interval time of the signal at the sense amplifier. The charge signal due to the memory element or transistor with 3nm nanoscale storage sites can be given as

$$\Delta Ids\ \Delta t = (q\ \mu\ (Vgs\text{-}Vt) / L^2)\ \Delta Nt\ \ \Delta t \qquad (3)$$

The minimum number of stored electrons, ΔNt, which can be sensed by the is then

$$\Delta Nt = ((KF\ \mu\ W\ L / 2)\ (\ln (fh/fl)))^{1/2} / (q\ \mu) \qquad (4)$$

This is limited or increases with the magnitude of the l/f noise and as the lower bandwidth decreases

or time differences between read signals increases. This is the minimum number of electrons in a single memory element which can be detected. If one electron is stored, $\Delta Nt = 1$, then the time until there is an error can be calculated as the time to failure, $tf = 1/fl$. For a single memory element or cell this can be a very long time.

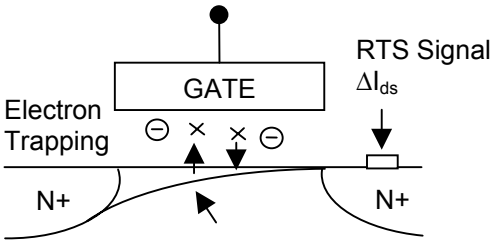


Fig. 4 Nanoscale memory showing charge stored on nanocrystals and the trapping and emission of electrons from traps in the gate insulator.

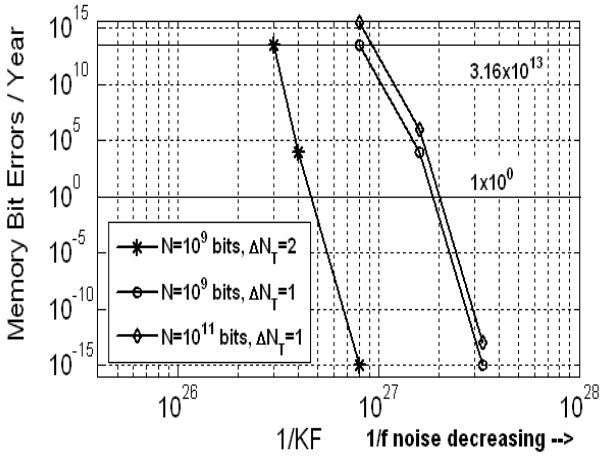


Fig. 5 Calculated error rate in a nanoscale memory due to l/f noise or RTS noise.

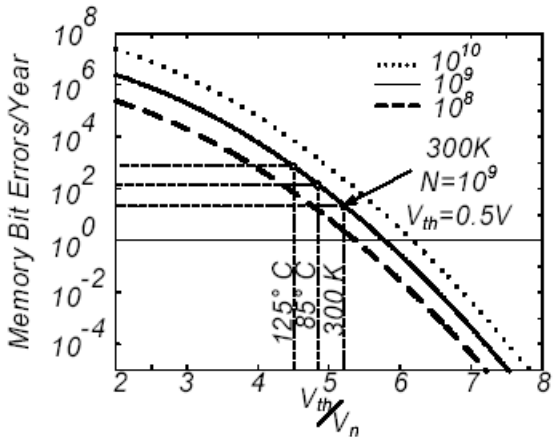


Fig. 6 For comparison the bit error rate calculated in nanoscale memories due to thermal noise.[4]

4 BIT ERROR RATES

Practical memories, however, have a very large number of individual elements or bits, N, typically a gigabit, and require very low bit error rates. If the failure rate is constant, $1/tf = fl$, and there are $N = lG$ bits then for a nanoscale memory the bit error rate will be around 10^{-6} or there will be more than one bit error per year. This is higher than the desired rate of one per year. [4,6]

As a matter of comparison Fig. 6 shows the calculated error rate in nanoscale memories due to thermal noise. [4] Both of these error rates have the same functional form and are comparable at and higher than one per year.

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4 CONCLUSIONS

These fundamental limits on nanoscale memories can be explained by RTS, random telegraph signals, or equivalently l/f noise in the frequency domain resulting from a combination of many different single electron events with different time constants.

The trapping of electrons in the gate insulator is equivalent to the trapping and storage of charge on nanocrystals in a nanoscale memory. During the read operation of a nanoscale memory it is impossible to distinquish whether the trapped charge is stored on nanocrystals or at trapping centers in the gate insulator. RTS and trapped charge can and will result in data errors in nanoscale memories.

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