A novel nonvolatile memory using SiO_x-cladded Si quantum dots

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ABSTRACT

This paper presents characteristics of a novel quantum dot gate nonvolatile memory (QDNVM) whose threshold shift can be varied by adjusting the duration and magnitude of the Programming Voltage pulse applied at the drain end. For example, in long-channel FET like structures, we observed a threshold voltage shift (ΔV_t) of 1 V for 10V/10μs stress pulse. Our preliminary data suggest: (i) faster 'Write' time and (ii) longer retention time for these devices as compared to conventional Si nanocrystal gate nonvolatile memories reported in the literature.[1, 2]

Keywords: silicon nonvolatile memory, silicon technology, silicon quantum dots, self-assembly, nanoscale memory

The schematic cross-section of the fabricated long channel nonvolatile memory device is shown in figure 1.

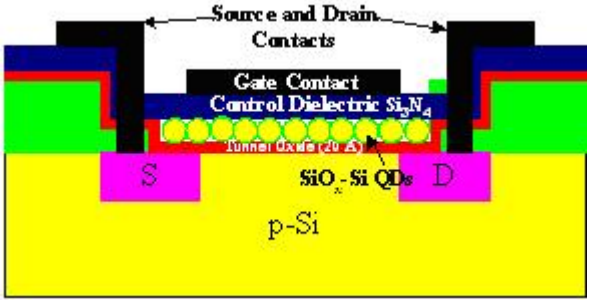

Fig 1 Schematic of a quantum dot gate nonvolatile memory (QDNVM) device.

Figures 2(a) describes the threshold shift in the transfer characteristics. The preliminary data exhibiting excellent data retention is shown in Fig. 2(b). The high data retention is attributed to the cladding SiO_x on Si QDs. This avoids the lateral dot-to-dot conduction, thereby avoiding any gate charge leakage path. It may be noted that the threshold shift in Fig. 2(b) is higher as here we used a longer duration 'Write' pulse. Channel Hot Electron Injection (CHEI) is believed to be the mechanism of programming the memory devices.

The gate of the above nonvolatile memory was formed by site-specific self-assembly (SSA) of SiO_x-Si quantum dots (QDs).[3] These monodispersed dots have an average

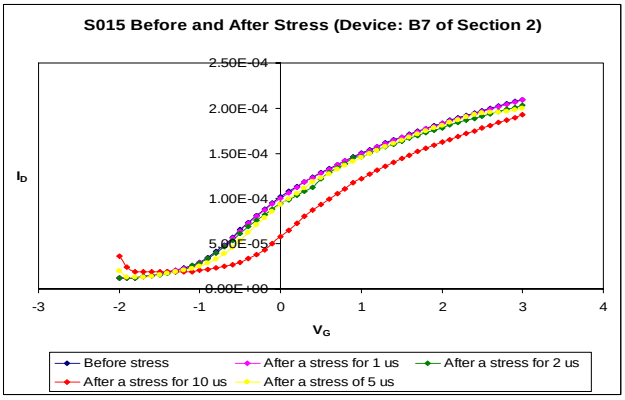

Fig. 2(a) Transfer characteristics showing threshold shift as a function of "Program" pulse duration.

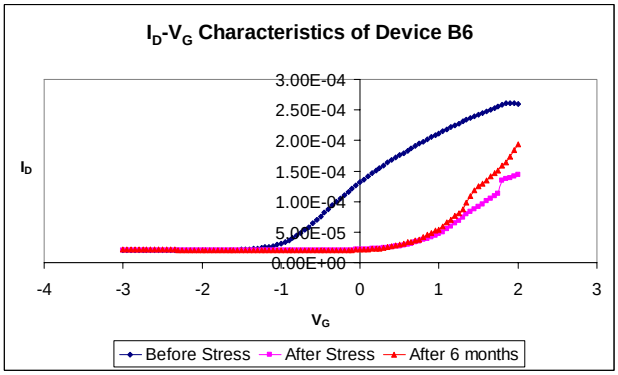

Fig. 2(b) Transfer characteristics showing threshold shift and data retention.

silicon core diameter of 4 nm and a SiO_x cladding thickness of 1-2 nm. Figure 3 shows the high-resolution transmission electron micrograph showing dot size and cladding thickness. QDNVM devices exhibit program/erase characteristics similar to the conventional floating gate nonvolatile memory devices.

The long-channel QDNVM devices reported here are fabricated on a 10 Ω-cm p-type (100) oriented silicon wafer. An ultra-thin tunnel oxide is grown by thermal oxidation at 900 °C. Next, a layer of 4 nm silicon nanoparticles with a 1 nm silicon dioxide cladding (SiO_x-Si quantum dots) was deposited. This was followed by deposition of a ~7 nm silicon nitride layer as control dielectric by plasma-enhanced chemical vapor deposition (PECVD) technique. The devices are tested using HP 4156A with a pulse generator. The fabrication process is

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061828 Vol. 1, 2007

CMOS compatible, and only differs from conventional processing by the step involving SSA of SiO_x-Si QDs. This makes the QDNVM a potential candidate for economic nonvolatile memory applications.

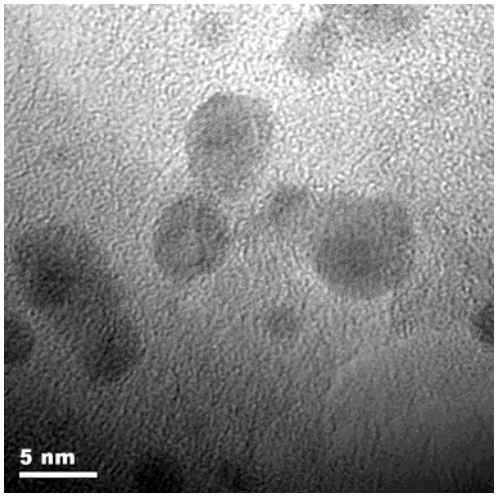

Fig 3. Transmission electron micrograph of SiO_x-Si cladded quantum dots.

ACKNOWLEDGEMENTS

This work was supported by Office of Naval Research Contracts N00014-05-1-0346 and N00014-06-1-0016 (Program Director: Dr. Daniel Purdy). The authors gratefully acknowledge the assistance of Prof. T-P. Ma, C-C. Yeh and Mr. C. Tillinghast (Yale University) for permitting the use of their laboratory facilities complementing University of Connecticut laboratories.

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