THE INITIAL REVERSE-BIAS INJECTING P+-N JUNCTION MODE IN P+-N-P+- STRUCTURES WITH PUNCHTHROUGH

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ABSTRACT

P+NP+ (N+PN+) – structures with the punchthrough (PT) effect and their modifications are used widely in different semiconductors' devices. All of them can split into two groups of the operating mode: 1. schemas with the floating base (FB); and 2. structures with the short-cut (SC) of the emitter-base p-n-junction.

We described behavior of P+NP+ (N+PN+) - structures with the initial reverse-bias injecting P+-N junction with the current punchthrough process; provided calculation drop voltages and volt – ampere (current) characteristics.

Keywords: Design, Devices, Current, Nanostructures, Punch-off, Punchthrough, Reachthrough, Voltage

1 INTRODUCTION

We describe behavior of P+NP+ (N+PN+) - structures with the initial reverse-bias injecting P+-N - junction and the punchthrough (PT) mode. The punchthrough, reachthrough, and punch-off processes are used widely in different semiconductors' devices: MOS- and JFETs, BJTs, Photo devices, CCD, memory cells, ESD, protection and stabilitrons (Zener diodes), different detectors and sensors.

All of them could be split into two groups of the operating modes: 1. schemas with the floating base (FB) and 2. structures with the short-cut (SC) of emitter-base p-n-junction. A development of the PT effect and its integration in conventional components of ICs requires the analyzing of sandwich structures with the initial RB emitter-base junction and the PT mode.

Devices with the short-cut emitter-base were researched in classical article [1]. The FB mode and its interconnection with the short-cut scheme were described in articles [2, 3].

2 CALCULATIONS OF DROP VOLTAGES

The transistor structure with the initial RB emitter and the conventional bias between collector-emitter is represented conventional bias between collector-emitter is represented on the Fig.1

In according to [4] a balance in P+NP+ transistor is

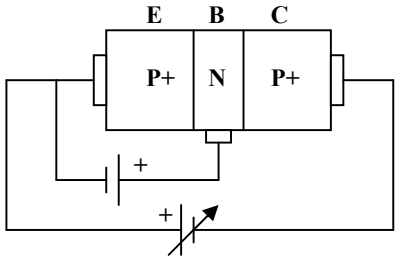

Fig. 1Sandwich P+NP+ - structure in the schema with the initial reverse-bias emitter

established when:

jgc –generation component of the collector current and

jre – recombination component of the emitter current are equalized.

The through current – Iceo in this structure with the FB is:

$$Iceo = jgc* Sc = jre*Se, \quad (1)$$

where: Sc, Se – collector and emitter squares, respectively.

In our case, Ne>>Nb<<Nc, where Nb, Nc, Ne – concentrations of doping purities in the base, both collector and emitter.

The dropping voltages on the P+Njunctions are [4]:

$$(\varphi cc + Uc)(\exp(-Uc/2\varphi t)-1)^2 = (Se/Sc*\tau oc/\ \tau oe)(\varphi ce - Ue)(\exp(Ue/2\varphi t)-1)^2 = Aabr(\varphi ce - Ue)(\exp(Ue/2\varphi t)-1)^2, \quad (2)$$

where: Aabr – the coefficient, which accounts design–technological parameters in the rate of noted quantities of abrupt P+N - junctions;

Sc, Se – squares collector and emitter P+N-junctions;

Uc, Ue – drop of voltages on collector and emitter P+N-junctions;

τoc, τoe - the effective time of the life of carriers in space charge regions (SCR)s collector and emitter P+N-junctions;

φcc, φce – contact potential difference for collector and emitter P+N-junctions;

φt – temperature potential.

The voltage –Uceo, which applied between collector and emitter terminals, is equal to a sum of drops' voltages on P+N-junctions:

$$Uceo = Uc + Ue \quad (3)$$

A width of the neutral base –Wn becomes zero by the punchthrough voltage – Uceo.pt:

$$Wn = W - (dc + de), \quad (4)$$

where: dc, de – sizes of SCRs collector and emitter P+N-junctions placed in N – base;
W – the metallurgical base width.
For abrupt P+N junctions are:

$$de = [2\varepsilon\varepsilon_o(\varphi ce - Ue)/qN_D]^{1/2} \quad (5)$$

$$dc = [2\varepsilon\varepsilon_o(\varphi cc + Uc)/qN_D]^{1/2}, \quad (6)$$

where: N_D – the concentration of the donor purity in the base region;
q – electron charge;
ε_o, ε – the permittivity of vacuum and relative permittivity of the semiconductor, respectively.
The consistent solution of equations (2-4) with using expressions (5, 6) allows the determent of the magnitude of the Uceo.pt and the distribution of the full applied voltage between collector and emitter P+N-junctions at prescribed bases' widths.
The punchthrough voltage for the SC schema – Uce.pt can be determined from [5]:

$$Uce.pt = q\,N_D\,W^2/2\varepsilon\varepsilon_o - W\,(2q\,N_D\,\varphi ce/\varepsilon\varepsilon_o)^{1/2} \quad (7)$$

The equation (2) transformed to the next identity for the RB schema:

$$(\varphi cc + U'c)(\exp(-U'c/2\varphi t)-1)^2 = Aabr(\varphi ce - U'e+Uer)(\exp((U'e-Uer)/2\varphi t)-1)^2, \quad (8)$$

where: U'c, U'e - drops of voltages on collector and emitter P+N-junctions in the RB schema;
Uer - the initial reverse-bias voltage on the emitter P+N-junction
The full applied voltage –U'ce is equal to the sum of voltages on the P+N – junctions:

$$U'ce = U'c + U'e + Uer \quad (9)$$

There are two conditions in the structure for the PT effect:

$$\begin{cases} Wn = W\ (dc + de) = 0 \\ Uer - U'e \le 0 \end{cases} \quad (10), (11)$$

In this case the base N- layer would be completely depleted with mobile carriers. The height of the potential barrier of the emitter P+N - became lower and started the injection holes through the depleted base into the collector. Equations (5, 6) are changed with new voltages (U'e –Uer) and U'c:

$$d'e = [2\varepsilon\varepsilon_o(\varphi ce - U'e + Uer)/qNd]^{1/2} \quad (12)$$

$$d'c = [2\varepsilon\varepsilon_o\,(\varphi cc + U'c)/qN_D]^{1/2} \quad (13)$$

The consistent solution of equations (8-13) by the condition in the Eq. (11) Uer – U'e = 0 determines the punchthrough voltage for the RB schema – U'ce pt.
For the calculation: Se = Sc; the effective time of life carriers in SCRs the collector and the emitter P+N-junctions are the same; the collector and the emitter have the uniformed meaning of the contact potential difference. The difference between voltages - Δ Upt in the SC and the RB schema over the range of the concentration base layer $10*14 \le N_D \ge 10*17$ (cm-3) practically does not depend on the concentration and the width of the medium layer and close to twice reverse-bias voltage of the emitter P+N – junction, namely:

$$\Delta Upt = U'ce.pt - Uce.pt \approx 2Uer \quad (14)$$

Calculated parameters were verified by experimental measurements [6], which are shown on the Fig. 2.

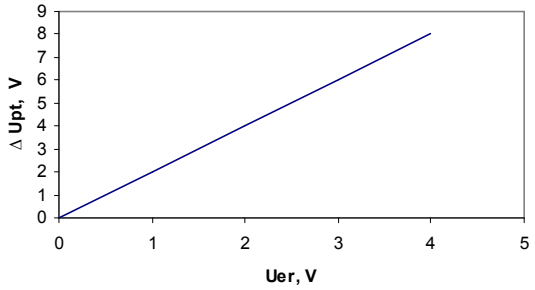

Fig.2 The change of the punchthrough voltage (Δ Upt) in the transistor structure is displayed against increasing of the reverse voltage on the emitter P+N – junction

3 VOLT – AMPERE CHARACTERISTICS

We need to determine volt-ampere (current) characteristics (VAC, VCC) for devices, based on the PT effect with the tuning PT voltages by the change of the rate of initial RB voltages.
The analysis is based on the assumption that currents' densities are so small that the mobile charge in the medium layer is less than concentration of the donor's purity and, therefore, a mobile charge can be disregarded.
The distribution of voltages in the P+NP+ - transistor structure with the reverse-bias emitter P+N- junction - I is represented on Fig.3. The drop voltage on the collector junction – U'c is less then the voltage-U'ce.pt for RB schema:

$$I.\ U(x) = (\varphi ce - U'e + Uer)\{1-[(x- d'e)/d'e]^2\} \quad (15)$$

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When the SCRs both of junctions touch each other (like the punch-off mode in two gates JFETs) it

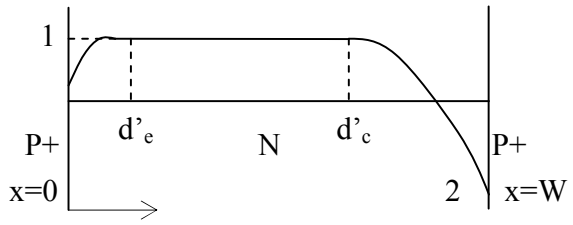

Fig. 3 The distribution (I) of the voltages in the P+NP+ - transistor structure with the reverse-bias emitter P+N- junction – (φce –U'e+Uer) - 1 by voltage on collector P+N-junction – (U'c) - 2 is less than the punchthrough voltage – U'ce.pt is shown

starts two processes: 1.deformation of space-charge regions of periphery parts of both junctions; 2. penetration of the collector the space-charge region under bottom emitter body – Fig. 4

Fig.5 shows the distribution - II of voltages in the structure with the SC emitter P+N- junction by applied voltage - Uce is equal to the PT voltage – Uce.pt :

$$\text{II.}\quad U(x) = (\varphi ce)\{1-[(x- deo)/deo]^2\}, \qquad (16)$$

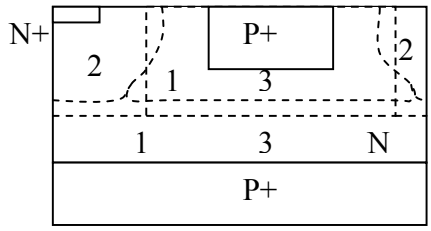

Fig. 4 The behavior of space-charge regions of the collector and emitter P+N – junctions:
1. Punch-off mode;
2. Deformation and penetration of SCRs (voltage – U'ce leve1 less then U'ce.pt);
3. U'ce = U'ce.pt

where: deo – width of SCR of the emitter P+N – junction by the condition of zero voltage;
x varies from zero to W.

The distribution of voltages (III) represents the case (Fig.5) of the RB schema and the condition of the voltage - U'ce is equal to the voltage – U'ce.pt:

$$\text{III. } U(x) = (\varphi ce –U'e+Uer)\{-[(x- d'e)/d'e]^2\} –$$

$$2Uer*x/W \qquad (17)$$

The member - 2Uer*x/W calculates an additional electrical field, applied to the structure. The distribution is performed by the solution system of Eq. (10, 11). The emitter junction is biased positively (Uer – U'e < 0) and the width of neutral base is equal to zero. The voltage collector-emitter – U'ce is equal to the PT voltage – U'ce.pt.

By increasing the voltage U'ce over U'ce.pt in the structure, distribution is in executed mode, which is described by the next relationship – the distribution – IV (Fig.5):

$$\text{IV.}\quad U(x) = (\varphi ce –U'e+Uer)\{1-[(x-d'e)/d'e]^2\} – 2Uer*x/W - \Delta U'ce*x/W \qquad (18)$$

An increment in the voltage - ΔU'ce reduces the height of the potential barrier of the emitter P+N-junction.

The PT current density – jce.pt in the P+NP+ - structure is described in the next Equation [1]:

$$jce.pt = jo* \exp\{\varphi t-1[deo/W*\Delta Uce – deo^2/4W^2*(\Delta Uce)^2/\varphi ce]\}, \qquad (19)$$

$$jo = qDpn_i^2/2\sqrt{\pi}L_D N_D\,[1 – \exp(-Uce/\varphi t)], \qquad (20)$$

where: Dp – the coefficient hole diffusion, $Dp = \varphi t*\mu_p$;
μ_p – holes mobility in N-base region;
L_D – Debay length for holes in base,
$L_D = [(\varphi t*\varepsilon\varepsilon o)(2gN_D)^{-1}]^{1/2}$;
n_i - intrinsic semiconductor conduction;
Δ Uce – increment in the voltage, Δ Uce = |Uce| - Uce.pt

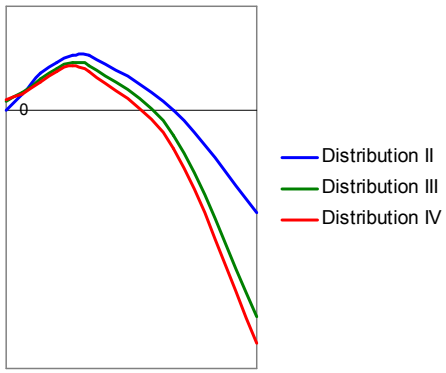

Fig.5 1.The distribution - II of voltages in the base of the P+NP+ - structure with the SC schema by Uce is equal to the punch-through voltage – Uce.pt.
2. The distribution - III represents the RB schema and the condition: voltage - U'ce = the voltage – U'ce.pt.
3. The distribution - IV describes the process of the increasing voltage U'ce over U'ce.pt in the structure.

The transport of holes from the emitter into the collector is determined by two components: diffusion and drift. By x = deo electrical field is equal to zero and the through current is diffusion one. The electrical field has a maximum magnitude on the collector P+N –junction and, therefore, by x = W drift component will be dominating:

$$jce.pt = \mu_p qpEmax, \qquad (21)$$

where: p – concentration of holes by x = W;
Emax – the maximum electrical field by x = W – dj, Emax = Uc/(W-dj) + ΔUce/W;
dj – the width of the emitter SCR in the punch-through mode an increment in the voltage - Δ Uce

$$jo^* \exp [\varphi t\text{-}1(deo/W^*\Delta Uce - deo^2/4W^2*(\Delta Uce)^2/\varphi ce)] = \mu_p qpE, \text{ or} \quad (22)$$

$$p = \frac{jo^* \exp [\varphi t^{-1}(deo/W^*\Delta Uce - deo^2/4W^2*(\Delta Uce)^2/\varphi ce)]*(W - dj)}{\mu pq\,[Uce.pt + \Delta Uce(1 - dj/W)]} \quad (23)$$

The additional electrical field is applied in the PT mode with the initial RB schema. The current density –j'ce.pt in P+NP+ - transistor structure with the RB in the PT mode, based on Eq.(19,23) is described, as:

$$j'ce.pt = qDpni2/2\sqrt{\pi L_D N_D}*[1 - \exp(-(Uce.pt + 2Uer)/\varphi t)]*[1 + 2Uer\,(1 - dj/W)/\,(Uce.pt + \Delta U'ce\,(1 - dj/W)]* \exp\,\{\varphi t\text{-}1[(deo/W*\Delta U'ce - deo^2/4W^2*(\Delta U'ce)^2\,/\,(\varphi ce + Uer - U'e)]\}, \quad (24)$$

where: U'ce = Uce.pt + 2Uer + ΔU'ce, or ΔU'ce = |U'ce| - U'ce.pt

The comparison of the two Eq. (19) and (24) is shown that last one has excess on the value -

$$1 + \frac{2Uer*(1\text{-}dj/W)}{Uce.pt + \Delta Uce(1\text{-}dj/W)} \quad (25)$$

and, therefore, the through current in the structure will be higher in the RB mode by the same magnitude of bias voltage - ΔUce.

4 EXPERIMENTAL RESULTS

The slopes of VACs are determined by the factor (25). In the beginning PT process the fraction in the Eq. (25) has the maximum influence on the VAC. When on the VACs appear an indication of the start of saturation (current limited of space-charge region) value of the fraction becomes lower and VACs converge to each other Fig.6 shows the experimental VACs P+NP+ -structures in the schema with the RB emitter P+N- junction

The Eq. (8-13) and Eq. (24) define drop voltage on the collector and emitter P+N junctions; VACs for the schema with the initial RB in the PT mode.

5 CONCLUSION

At the beginning we started studying the punchthrough effect to provide reliable protection for wideband, low flicker- and HF- noise in precision measuring equipment, for sample [6]. The combination of different behaviors

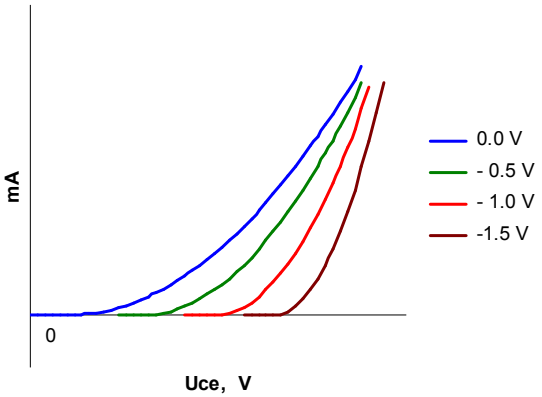

Fig.6 The experimental VACs P+NP+ -structures in the scheme with RB emitter P+N- junctions for the lateral P+NP+ structure with n – substrate (N_D = 3.10 ^{14} cm^{-3}, ρ = 25 Ohm.cm).
1. Uer = O; 2. Uer = -0.5 V; 3. Uer = - 1V; 4. Uer = -1.5V

established the PT, reach-through and punch-off modes for design of perspective devices. The name "The bipolar transistor with field operating in punchthrough mode" sounds strange today, but "Punch-through MOSFET – transistor" [7] is a reality.

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