Novel lithography technique using an ASML Stepper/Scanner for the manufacture of display devices in MEMS world

ASML US, Inc - Special Applications, 6580 Via Del Oro San Jose, CA 95119
Keith Best, Pankaj Raval, Norbert Kappel
SVTC, 3901 1st Street, San Jose CA 95134
Nazneen Jeewakhan, Milan Prejda, Kevin Kassekert, Michael Moore
Miradia, 281, E. Java Drive, Sunnyvale, CA 94089
Charles Yang, May Wang, Ye Wang

ABSTRACT

In the MEMS and MOEMS product world, manufacturers of display/micro-devices require bonding of two wafers. The front side pattern of the top wafer needs to be aligned with aggressive overlay requirements with the remaining portion of the device that is to be patterned on the backside of the same wafer. The most important first challenge here is to devise a lithography technique that will allow the alignment of layers on the backside of the wafer to the pattern on the wafer's front surface after bonding (thereby encapsulating the patterned surface) without significant hardware changes to ensure that the resulting overlay will support the product performance specifications. ASML's Special Applications Business unit jointly with SVTC and Miradia came up with a simple but elegant lithographic technique that can be applied on ASML's advanced patterning tools as solution to this challenge. Paper will discuss the lithographic technique and processes developed to overcome these challenges for device production including supporting technical details and data as applicable.

Keywords: MEMS, MOEMS, alignment, device, micro mirrors, bonding

1 INTRODUCTION

The Micro-Electro-Mechanical Systems (MEMS) applications world has been growing in last few years and continues to grow at a rapid pace. As new applications are being developed in this industry with ever decreasing critical dimension and overlay requirements, many manufacturers are using presently available standard semiconductor processing equipment such as wafer steppers and advanced metrology equipment with their available processes and alignment schemes.

In order to accomplish this, MEMS manufacturers face a unique challenge. To gain cost advantages or simply to get reliable manufacturing processes for their product, they need to develop unique or different techniques or solutions by adapting or improving existing toolsets and process solutions that are developed for semiconductor manufacturing.

Miradia, a developer of advanced MEMS based devices, faced such a challenge in developing a manufacturing process for their micro mirror based display device. Like other typical MEMS processes, Miradia's production process also required that one wafer was bonded to a second wafer, which needed to be patterned on both sides. Important requirement here was to align patterns from the backside of the second wafer with layer(s) patterned on the front side of the first wafer with a certain level of accuracy using readily available lithography tools (stepper/scanner). This should be done without any significant hardware modifications for obvious reasons of time and cost. SVTC, with its state of art fab in San Jose, CA, works closely with customers like Miradia in development of such new product(s) in the R&D and pre-production stage. Since SVTC uses ASML stepper and scanners, a joint project was initiated between Miradia, SVTC, and ASML to develop an alignment scheme for Miradia's production process.

In the first early phase of development, ASML's Special Applications Business unit jointly with SVTC and Miradia brainstormed and came up with a simple but elegant lithographic technique that can be applied on ASML's advanced litho tools as solution to this challenge. These three companies then, using this novel litho technique developed a complete process that can now be applied in the large scale production of this display device.

The basic methodology of patterning structures on the wafer's front side, then flipping/bonding/back grinding, and again patterning a second layer on the wafer's backside was carried out without Front-To-Back Alignment (FTBA) hardware or a specialized FTBA tool. All layer patterning as well as metrology was performed on an ASML tool. All other processes between first and second layer were performed using standard semiconductor and MEMS (bonding) processing techniques by SVTC and Miradia.

2 BACKGROUND

The Miradia process flow can be divided into three parts: 1) IC wafer; 2) Back Etch processing; 3) Front processing. See schematic below.

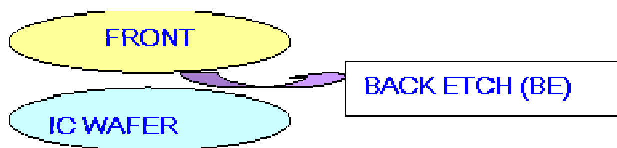

Fig 1: Miradia Process Flow

The Back Etch process (litho+etch) is completed at SVTC where the wafer is bonded to an IC wafer and thinned down using a grinding process. The alignment between the IC wafer and the Back Etch is mainly dependent on the bonding accuracy and not considered critical in Miradia's manufacturing process. However, the alignment between Back Etch and the Front Layers is very critical for the final device performance.

In order to meet this critical requirement, three party work schemes were developed. The testing and development tasks were carried out in team fashion among the three companies:

– ASML-SA (as OEM and Tool Applications expert) with help from SVTC (as process integrator in their advanced lab equipped with ASML tools) had the first responsibility to setup first phase of tests to provide alignment solution with proof of concept.
– Once that was completed, in the second and final phase Miradia (as device developer and actual product process expert) and SVTC ran pre-production tests on actual devices using proven alignment scheme from phase 1 and fine tuned other process related parameters at the SVTC or any other production facility.

The following paragraph describes the basic concept of the alignment scheme in detail.

2.1 ASML Alignment process

ASML uses PM (Primary marks) or XPA (eXtended Pattern Area) marks for global alignment of individual marks. The standard PM or XPA marks are made up of four phase gratings.

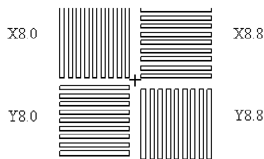

Fig 2: ASML Standard Alignment Mark

Two gratings are for alignment along the X-Axis (X8.0 and X8.8) and two gratings are for alignment along the Y-Axis (Y8.0 and Y8.8). The two gratings of 8.0um and 8.8um significantly increase the capture range and reliability of the alignment system. These marks are usable as long as the marks and the layers aligning to these marks are on the same side of the wafer. Once the wafer is flipped by 180degrees, the 8.0um and 8.8um are also flipped and the alignment system no longer recognizes these marks.

2.2 The Reverse XPA mark (RXPA)

Since the standard PM mark cannot be used once the wafer is flipped, ASML Special Applications developed a mark that could be used post-flipping to align the FRONT to the Back-Etch in Miradia's process. This mark is called the Reverse XPA (mirrored-XPA) or the RXPA mark.

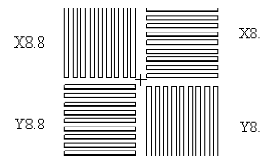

Fig 3: Example of ASML Reverse Primary Mark (RPM)

The std XPA mark is flipped in the Y direction to generate the RXPA mark. When these marks are printed on a wafer and the wafer is flipped, the 8.0um and 8.8um gratings will have the same orientation as the std XPA mark. Stated differently, the RXPA mark would become a std XPA mark after the wafer is flipped.

3 EXPERIMENTAL METHOD AND SETUP

The process sequence using the RXPA mark was:

- Print standard XPA marks and Reverse XPA mark at the same time.
- Align BE to the standard XPA.
- The wafer would be flipped and bonded to the IC wafer.
- Post flipping, Reverse XPA mark printed on the BE side of the wafer now becomes the standard Zero mark.
- Print a new set of XPA marks (XPA_Reversed) on the front side of the wafer
- Align these zero marks to the Zero mark on the backside of the wafer.
- Align the front layers to these new zero marks.

The reason behind printing the XPA and the RXPA marks at the same time is that BE would then indirectly be aligned to the RXPA marks. The purpose of printing a new set of alignment marks after flipping is that we expect the signal strength of the RXPA to be weaker through a few microns of Silicon post-flipping, and subsequent processes (Metal Deposition etc) would only weaken the signal strength even further. See schematic below:

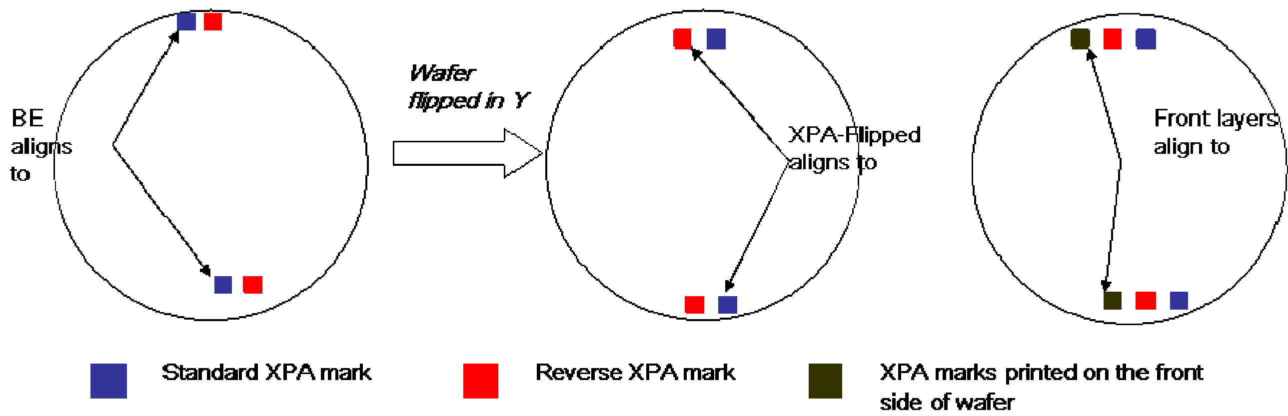

Fig 4: Schematic showing alignment scheme through the Miradia process flow

An additional complication faced by the Team was that SVTC fab had multiple ASML toolsets that were matched to each other by applying some corrections to the machine constants. This would impact Miradia flow, because after the wafer was flipped, the sign of the machine constants would also get reversed and result in a high non-correctable overlay term. For e.g. if there was a 10nm X Translation applied to the machine constants, after reversing the wafer, if the machine constants were not changed, there would be a 20nm translation term that would not be correctable. To overcome this issue, SVTC had to alter the machine setup to run Miradia's lots.

In the 1st COL (cycle of learning) the standard ASML Overlay metrology reticle was used to test this alignment scheme and get proof of concept.

Two 8" SOI (Silicon-on-Insulator) wafer sets were exposed through the initial steps of the Miradia process. Standard XPA marks and RXPA marks were patterned. This was followed by a 1st layer, which was patterned with the Overlay reticle. This pattern was then etched into the substrate approximately 1200A. The two layers processed to this point were patterned at SVTC on ASML PAS5500/100 system. All wafers were returned to Miradia foundry who bonded the SOI wafer, face down to standard 8" CMOS wafers. The patterned wafers were then back-grinded and wet etched to within 2-3µm of the front side pattern, after which the front layer patterning was done on a ASML PAS5500/500 system. Miradia's critical alignment requirement of less than 200nm had to be achieved between two sets of ASML systems including machine to machine alignment error consideration.

4 RESULTS AND DISCUSSIONS

4.1 Alignment Test for Concept Proof at ASML/SVTC

The two bonded wafers were exposed on the ASML PAS5500/500 tool. The bonding process at the time this work was completed was not mature, and there were a number of locations on the wafer where bonding had not occurred and de-lamination had begun. However, the wafers aligned on the tool, and the alignment data was taken as shown below:

Wafer	R-magn [ppm]	R-rot [urad]	Worst W-qual M1 [%]	Worst W-qual M2 [%]	8.0 to 8.8 [um] X-M1	Y-M1	X-M2	Y-M2
1	0.21	17.90	4	4	-0.030	-0.039	-0.069	-0.070
2	0.54	18.27	5	7	-0.118	-0.077	-0.063	-0.089

Table 1: Alignment results of the 2nd layer exposed on ASML PAS5500 /500.

The signal strength obtained from the marks was sufficient to align the wafers considering the quality of the incoming wafers.

The overlay was measured on the ASML PAS5500/500 itself, since there were no overlay targets on this reticle. The overlay results are shown below:

	Filtered Overlay Error		
	X [nm]	Y [nm]	Vector [nm]
Mean	-101.6	-108.3	
Std. Dev	89.0	60.1	
|Mean| + 3 Sigma	368.6	288.5	
Maximum 99.7%	309.9	280.0	387.7

Table 2: Overlay performance of the 2nd layer exposed on ASML PAS5500 /500

The measured overlay was larger than the final product level requirement for these test wafers during this first cycle. However, it helped identifying process induced

issues. The classification of the individual components of the overlay error are shown in Table 3.

	Component	Model Parameters		Max Resulting Errors	
		Mean	Std. Dev	Mean [nm]	Std. Dev [nm]
Inter field	Translation in X [um]	-0.102	0.029	-101.9	29.2
	Translation in Y [um]	-0.108	0.003	-108.2	3.5
	Wafer Rotation [urad]	-0.189	0.353	-14.4	26.9
	Non-orthogonality [urad]	-0.252	0.081	-19.2	6.1
	Scaling in X [ppm]	1.321	0.057	100.7	4.3
	Scaling in Y [ppm]	0.249	0.05	19.0	3.8
Intra field	Translation in X [um]	-0.102	0.074	-101.9	73.7
	Translation in Y [um]	-0.108	0.036	-108.2	36.1
	Rotation [urad]	4.242	1.556	66.0	24.2
	Magnification [ppm]	2.823	2.755	43.9	42.8

Table 3: Uncorrected Overlay Error Classification

The Interfield translation terms and the Scaling terms were the major contributors to the overlay error. Corrections were applied to the exposure tool, to check if the overlay error would reduce by applying corrections.

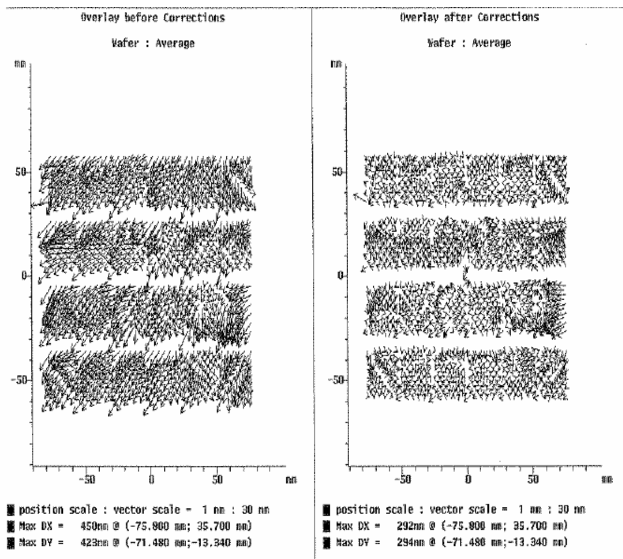

Fig 5: Overlay vector plot - before & after applying corrections.

It is shown in figure 5 that, after applying appropriate system level corrections, the overlay got slightly improved but still would not achieve required specification for the product. The observation of significant randomness in the remaining error indicated, that the error was too large to be attributed to lens distortion alone. It was noticed that the bonding quality was very poor on all the wafers. That was identified to be the one of the main causes of the high randomness.

However, the test also gave the required proof of concept, showing that the alignment between two layers on different sides of a substrate can be achieved using a novel technical solution employed by ASML/SVTC to align front and back of wafer using ASML's Reverse XMA target. In future iterations the overlay will improve further once the bonding process is mature and robust.

4.2 Miradia Product Test

Once the concept for the front to back alignment using ASML's new Reverse XPA mark strategy was proven the test was shifted to SVTC/Miradia (Fab environment) to resolve bonding issues in order to validate the concept on actual production wafers.

For the actual device, the allowed misalignment budget for this specific process step was less than 200nm. Otherwise, the micro-mirror structure will not be released from the supporting wall as shown in the following pictures (Fig 6):

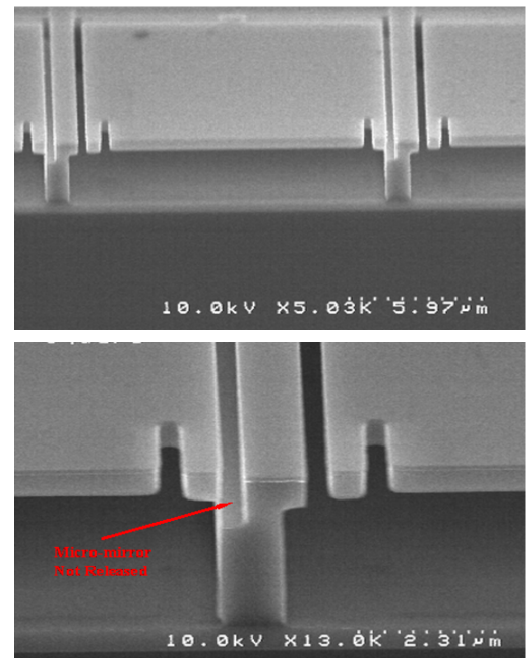

Fig 6: Misaligned and unreleased micro mirror structure

ASML/SVTC test had uncovered that Miradia's process flow of flipping and bonding the wafer, had induced significant amount of wafer level pattern translation and expansion. At the same time, two critical layers involved used different tools (I-line and DUV) for the exposure because of the different photo resist budget requirement. Due to the factors outlined above, it was clear that it was not easy to achieve less than 200nm

misalignment required for reliable device performance for Miradia unless some additional manufacturing process improvement as well as device level overlay measurement and correction scheme were implemented.

After Miradia implemented the alignment method, improved bonding process and also designed an OVL box to do actual measurement and correction, the team could achieve |Mean|+3sigma <=200nm after corrections. The following table lists the OVL data from one lot to show the mis-alignment with pre and post OVL correction:

First Pattern:

	X	Y
Average	69.1	75.1
Max	167	139
Min	10	8
3sigma	236	230

0, 0	X	Y	OVL Error Magnitude	
1	100	67	120	Average
2	167	139	217	
3	80	-62	101	
4	51	-8	52	123
0, -4	X	Y		
1	25	116	119	
2	-68	86	110	
3	-62	-38	73	
4	41	39	57	89
-4, 0	X	Y		
1	-36	-61	71	
2	-128	-97	161	
3	-68	-111	130	
4	63	-102	120	120
0, 4	X	Y		
1	92	-62	111	
2	-29	-55	62	
3	-33	-106	111	
4	96	-113	148	108
5, 0	X	Y		
1	-10	-70	71	
2	-78	-28	83	
3	-56	-51	76	
4	98	-90	133	91
Average	69.1	75.1	106.2	

Second Pattern with Corrections

	X	Y
Average	40.0	49.5
Max	89	78
Min	8	22
3sigma	136	53

0, 0	X	Y	OVL Error Magnitude	
1	70	-26	75	Average
2	81	-41	91	
3	-18	-74	76	
4	8	-44	45	71
0, -4	X	Y		
1	16	-31	35	
2	-48	-43	64	
3	-68	-71	98	
4	9	-44	45	61
-4, 0	X	Y		
1	-58	-57	81	
2	-89	-65	110	
3	-20	-23	30	
4	14	-34	37	65
0, 4	X	Y		
1	74	-73	104	
2	-15	-42	45	
3	-52	-47	70	
4	20	-78	81	75
5, 0	X	Y		
1	-17	-66	68	
2	-52	-66	84	
3	-55	-43	70	
4	-15	-22	27	62
Average	40.0	49.5	66.8	

Table 4: Actual Product Overlay Data

With this improved alignment, micro mirror devices were released properly as shown in the SEM pictures in Figure 7. As depicted, the micro mirror is a flat reflective membrane and suspended by a pair of tortional hinges that are anchored at a honeycomb-like wall. The entire mirror structure is made of a single crystal silicon material that gives superior optical performance and long-term reliability.

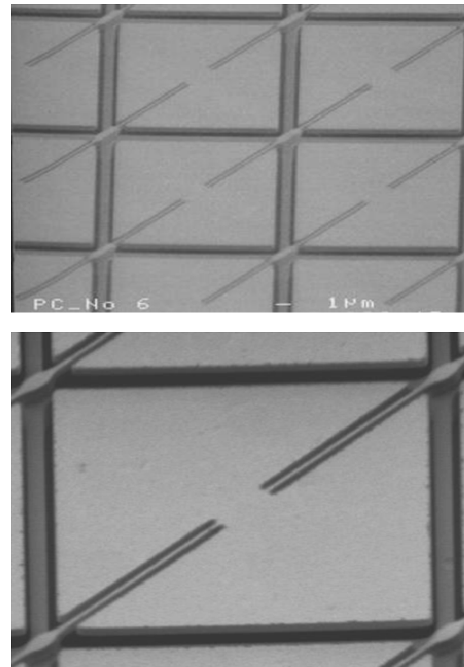

Fig 7: Aligned and released micro mirror structures

The front to back alignment is not only crucial for proper mirror structure release but also important to the operation of the micro mirror device. As depicted in Figure 8, the mirror is bi-stable electrostatically driven by a pair of underlying electrodes. Therefore, a precise mirror-to-electrode alignment is critical to controllability of the mirror, i.e. operational margin of the device. The improved alignment scheme was able to meet the stringent requirements and yielded fully functional devices.

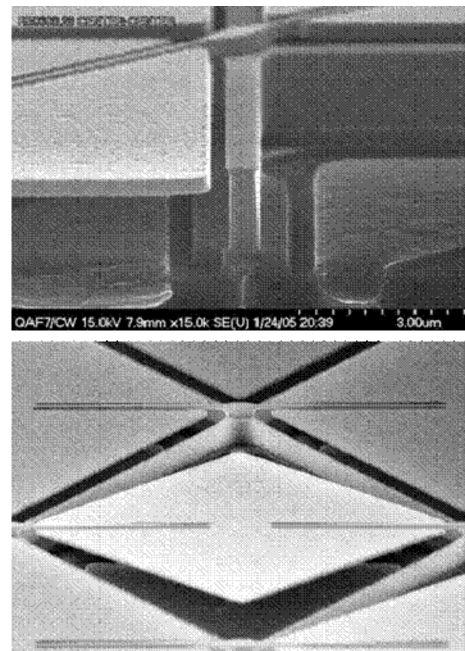

Fig 8: Released functional micro mirror

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061828 Vol. 1, 2007

An array of micro mirrors was fabricated in various formats such as VGA and XGA. Each mirror is a pixel and controlled independently by an underlying high-V SRAM cell. The bi-stable mirrors modulate light digitally and switch in few micro seconds from an ‘on’ state to an ‘off’ state. Grey scale and colors are created by a PWM (Pulse Width Modulation) and complex control algorithm. Detailed imaging processing and optical engine architecture are beyond the scope of this paper.

As shown in Figure 9, test patterns and full videos have been demonstrated with the mirror device.

Fig 8: Images produced by micro mirrors

5 SUMMARY CONCLUSIONS

The front to back alignment is not only crucial for proper mirror structure release but also important to the operation of the micro mirror device. Using ASML’s special Reverse XPA (RXPA) targets strategy along with controlled wafer bonding processes and improved overlay measurement/correction scheme, this front to back alignment for a critical layer is accomplished.

Properly working micro mirror devices are now manufactured in the production fab successfully.

This paper also shows that a novel idea or design concept can be successfully converted into a volume manufacturing process. The final commercial product is achieved by close cooperation and team effort among the device developer (Miradia), high end development lab or foundry services provider for such applications (SVTC), and OEM and tool technology partner (ASML- SA) that can provide application support and technical expertise for their equipment

A true “Lab to Fab” success story. This three party cooperative solution provides the fabless designer/entrepreneur, a cost effective way to turn his novel technology ideas in to a real product.

ACKNOWLEDGEMENTS

The authors acknowledge with thanks the contribution made by Alex Friz (ex-ASML) in setting up the initial testing at ASML for the project. In addition, the authors would also like to thank Binder Mann of ASML-SA for collecting the data at ASML.