High Frequency Characteristics of Nanoscale Silicon Nanowire FET

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ABSTRACT

Nanoscale multigate field effect transistors (FETs) are potentially next-generation device candidates for achieving high performance targets of the ITRS due to their superior reduction of the short channel effects and excellent compatibility with planar CMOS fabrication process [1, 2]. In this work, we for the first time numerically explore the high frequency characteristics of the sub-45nm silicon nanowire FET. Three-dimensional (3D) density-gradient-based device transport equations directly coupling with circuit equations are simultaneously performed for calculating the property of frequency response. Our result shows that the cut-off frequency of a well-designed sub-45nm nanowire FET with 100% surrounding gate is approach to 10 THz, which substantially benefits from the nature of infinite gate in the nanowire FET. Silicon-based nanowire FET devices as active components in microwave circuits draw people's attention for their extremely rich high frequency property [3, 4]. The extensive results and analyses are presented on the promising devices for high frequency analog applications.

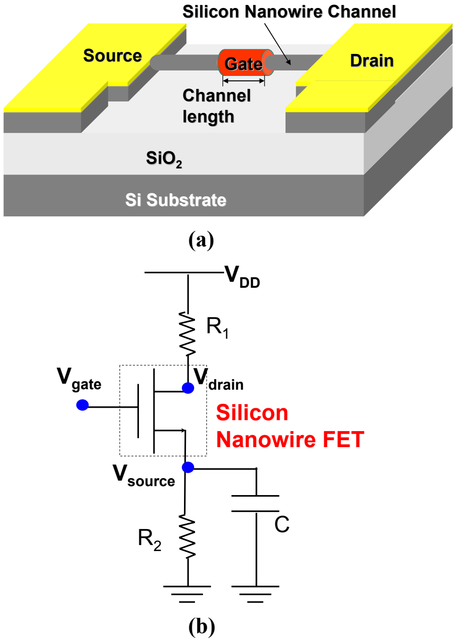
Keywords: Nanowire FET, High frequency characteristics, Surrounding gate, VLSI devices, 3D device simulation, Circuit simulation, Mixed-mode simulation.

1 INTRODUCTION

Recently, the microwave small-signal characterization of a 50nm-gate FinFET measurement has predicted the f_{max} of 250 GHz with an optimized fabrication process [4]. Using high frequency and wide bandwidth for next-generation electronic application have become more and more important. Especially, the nanoscale multiple-gate FET devices have been of great interest and relatively present better scaling properties than that of conventional bulk MOSFETs [5-11]. Among the multiple-gate FET devices, the fascinating high cut-off frequency and low noise characteristics of surrounding-gate over single-gate and double-gate has benefited the high frequency application [3]. The inherent good suppression of short-channel effects and ideal subthreshold swing (SS) of surrounding gate have received much attention for advanced usages, such as DRAM, Flash EEPROM, low-noise amplifier and oscillator [12]. Although there has been reported several short channel effects on the DC properties of surrounding gate [3,13-16], high frequency characteristics of the sub-45nm silicon nanowire field effect transistors have not been intensively described [3-4].

In this paper, three-dimensional density-gradient device simulation with different geometry ratio including the gate length and the radius of cylindrical gate are performed to evaluate the DC characteristics of silicon nanowire FET, shown in Fig. 1(a) first. Then the three-dimensional density-gradient device equations directly coupled with circuit equations are simultaneously performed for the calculation of the property of the frequency response. The circuit topology is shown in Fig. 1(b). Result shows the cut-off frequency and bandwidth of a well designed sub-45nm nanowire FET with 100% surrounding gate are approach 10 THz and 210GHz, respectively.

This paper is organized as follows. The simulation flow is described in Sec. 2. In Sec. 3, the DC and high frequency characteristics are discussed. Finally, we draw conclusions.



(a)

(b)

Figure 1: (a) The studied silicon nanowire field effect transistors, where the 100% surrounding-gate structure is assumed. (b) The circuit topology used in the 3D mixed-mode simulation.

2 SIMULAITON METHODOLOGY

To investigate the geometric impact on the electrical characteristics for the small nanowire FinFET with 100% gate coverage, the simulated nanowire FinFETs are with different radius, 4nm and 6nm, and different gate length, 16nm, 22nm, 45 nm, respectively. The devices' channel doping concentration is $2.3\text{x}10^{17}\text{cm}^{-3}$, where the gate oxide thickness is 1.2nm and the work function used is 4.6eV. Outside the channel, the source/drain doping is $3\text{x}10^{20}\ \text{cm}^{-3}$. A density-gradient equation together with the classical 3D drift–diffusion model [18-21] is adopted and solved numerically in this study. To capture the characteristics of device and circuit concurrently, the device simulation directly coupling with circuit equations are simultaneously performed for the calculation of the property of the frequency response. The simulation procedure consists of the following steps.

Step 1. Construct a 3D silicon nanowire FET with different geometry.
Step 2. Formulate the device's quantum mechanical transport model.
Step 3. Solve the device's transport model and obtain the device's DC characteristics.
Step 4. Formulate the circuit's network equation in a sparse tableau formulation.
Step 5. At a given frequency, solve the device's and circuit's equations simultaneously till the specified stopping criteria for the inner and outer iteration loops are satisfied.
Step 6. Repeat *Step 5* and sweep the frequency from $1\text{x}10^{8}$ GHz to $1\text{x}10^{13}$ GHz.
Step 7. Post-process to obtain the circuit characteristics.

3 RESULTS AND DISCUSSION

The threshold voltage roll-off of different device radius (*R*) in nanowire FETs' is shown in Fig. 2. The devices with a larger radius show a steeper slope due to the weaker gate controllability. Such trend of threshold voltage roll-off could be explained with the analytic model in [3, 13-17].

$$V_{th} \propto V_{FB} + 2\phi_f + C\left(t_{si}\right)^2 \ln\left(1+\frac{2t_{ox}}{t_{si}}\right), \qquad (1)$$

where V_{FB} is flat-band voltage, ϕ_f is difference of Fermi level and intrinsic Fermi level, C is a constant, t_{ox} is gate oxide thickness, and t_{si} is cylindrical diameter. This phenomenon can also be verified by Fig. 3(a). The nanowire FET with smaller radius exhibits significantly better on-off current ratio, SS, and drain-induced barrier lowering than that of the device with the larger radius. To further examine this phenomenon, the on-off current ratio with different gate length and radius are shown in Fig. 3(b). Results show that the devices with a smaller radius perform better electrical characteristics; moreover, the on-off current ratio decreases as the channel length decreases. Figure 3(c) shows the comparison of the devices with the same radius but different gate length. In this case, as the device's gate length scaling down, both the on-state and off-state currents are increased due to the threshold voltage roll-off, as shown in Fig. 2. However, the increasing magnitude of off-state current is significantly larger than the on-state current, and thus results in worse on-off ratio in the shorter channel length. Figure 4 shows (a) the transconductance (*gm*), (b) the output resistance (*Rout*), and (c) the gate capacitance (*Cg*) of the silicon nanowire device with different radius (*R*) and gate length. The relationship of these characteristic between gate length and radius are shown as follows and the electrical characteristics are summarized in Tab. 1.

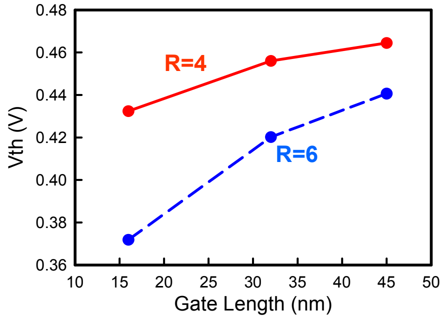
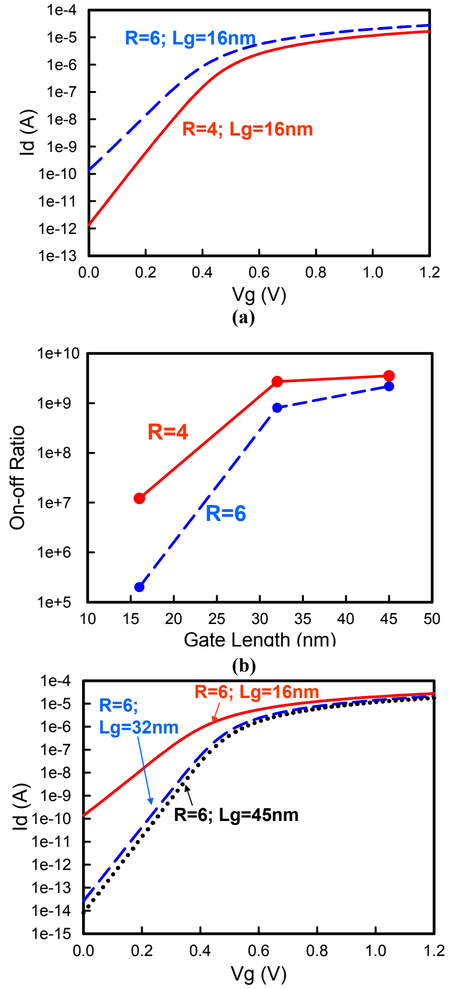


Figure 2: The trend of *Vth* roll-off with respect to *R*.



(a)

(b)

(c)

Figure 3: (a) The Id-VG curves of device with the same radius but different gate length. (b) The corresponding on-off ratio with different *R*. (c) The Id-VG curves of the device with same *Lg* but with different *R*.

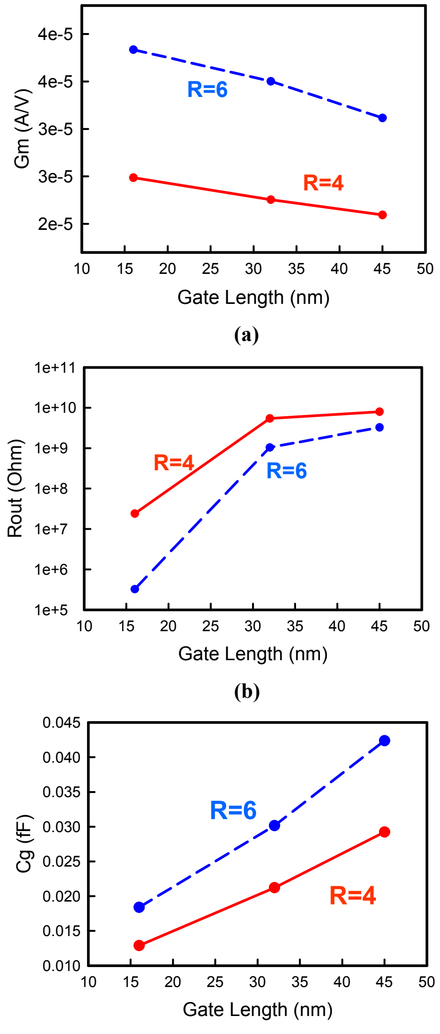
$$G_m \propto \frac{R}{L_g}(V_{gs} - V_{th}) \qquad (2)$$

$$R_{out} \propto \frac{L_g}{R} \qquad (3)$$

and

$$C_g \propto \frac{L_g}{\ln(1 + t_{ox}/R)} \qquad (4)$$

The high frequency characteristics of the studied circuit are shown in Fig. 5. Figures 5(a) and 5(b) show the high frequency characteristics of devices with same device radius but different gate length and devices with same gate length but with different device radius, respectively. The relationship between the device characteristics and the behavior of the given circuit topology are shown below.



(a)

(b)

(c)

Figure 4: The plots of (a) transconductance, (b) output resistance, and (c) gate capacitance of the silicon nanowire with different device radius and gate length.

$$Gain \propto G_m R_{out} \qquad (5)$$

$$F_T \propto \frac{Gain}{C_g} \qquad (6)$$

and

$$Bandwidth \propto \frac{1}{C_g} \qquad (7)$$

As the gate length scaling down, the device's G_m is increased and the *Rout* is decreased; therefore, the resulted circuit gain shows a maximum gain at 32nm-gate length, shown in Fig. 5(a). Moreover, since the cut-off frequency (*Ft*) is proportional to circuit gain and in proportional to gate capacitance (*Cg*), the cut-off frequency also exhibits similar trend as circuit gain. The results are summarized in Tab. 2. As shown in Fig. 5(b), since the device's G_m is decreased with the decreasing radius, the result of circuit gain also reflects this phenomenon. Moreover, the bandwidth is in proportional to gate capacitance in Eq. (7), the smaller gate capacitance of device with the 4nm radius show larger bandwidth than device with the 6nm radius shown in Tab. 2.

Table 1: The summarized DC characteristics of the studied silicon nanowire transistors.

R (nm)	**Lg (nm)**	**Vth (V)**	**Ion (A)**	**Ioff (A)**	**DIBL (mV)**
4	16	0.383	1.65E-05	1.36E-12	47.81
4	32	0.456	1.30E-05	4.81E-15	10.43
4	45	0.464	1.16E-05	3.29E-15	9.89
6	16	0.287	2.76E-05	1.38E-10	92.89
6	32	0.420	2.09E-05	2.59E-14	14.88
6	45	0.441	1.76E-05	8.06E-15	11.15
R (nm)	**Lg (nm)**	**S.S (V/A)**	**Gm (A/V)**	**Rout (Ohm)**	**Cg (fF)**
4	16	75.06	2.49E-05	2.41E+07	0.013
4	32	60.32	2.25E-05	5.44E+09	0.021
4	45	60.10	2.09E-05	7.98E+09	0.029
6	16	98.19	3.84E-05	3.25E+05	0.018
6	32	62.07	3.50E-05	1.04E+09	0.030
6	45	60.39	3.12E-05	3.26E+09	0.042

Table 2: The summarized high frequency characteristics of the studied silicon nanowire circuit.

R(nm)	**Lg (nm)**	**Gain (db)**	**Ft (Hz)**	**BW (Hz)**
4	16	17.69	9.67E+12	2.10E+11
6	16	18.16	9.70E+12	1.72E+11
6	32	18.95	9.80E+12	1.03E+11
6	45	18.32	1.94E+12	9.14E+10

4 CONCLUSIONS

In this paper, the DC and high frequency characteristics of nanoscale silicon nanowire FET with 100% surrounding gate FET have been numerically studied by using a 3D mixed-mode simulation. Our results have shown that the cut-off frequency of a well designed sub-45nm nanowire FET with 100% surrounding gate can be greater than 10 THz. Moreover, we have for the first time show the high-frequency characteristic of sub-45nm nanowire FET and using the device's DC characteristics to explore the high-frequency phenomenon of the given circuit topology. We notice that the gain, the cut-off frequency and the bandwidth of the silicon nanowire circuits are 1.6, 18 and 3 times (not shown in here) larger than that of bulk-FinFET circuits in our study.

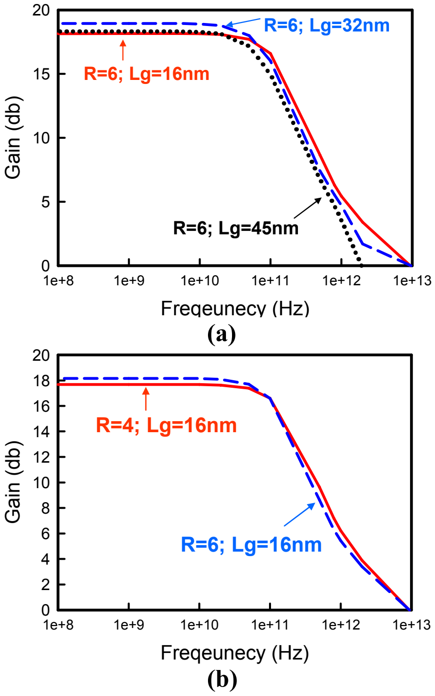


Figure 5: The plot of high frequency characteristics of the studied circuit. (a) Devices with the same *R* and different *Lg*. (b) Devices with the same *Lg* and different *R*.

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