

Silicon Nanoparticles Contacted by Metal Nanogaps for FET Applications

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ABSTRACT

A low-cost and simple fabrication technique is proposed to prepare a bottom-gate FET applying nanometer scale particles of silicon (*nc-Si*). The described advantageous approach renounces non-optical lithography techniques and utilizes effectiveness of conventional optical lithography in terms of alignment and large-area processing in fact. Nanoscale FETs are contrivable with a small number of nanoparticles though. The functional principle and the processing of the proposed device, particularly with regard to the application of nanocrystalline silicon and their contacting to metal electrodes are shown. The applied nanoparticles are characterized and first results of a potential field effect within the *nc-Si* are presented afterwards. Device characteristics show reasonable turn-off characteristics and ON/OFF-ratios up to $2 \cdot 10^2$.

Keywords: nanoparticle, nano gap, FET, silicon

1 INTRODUCTION

Currently almost all technologies of semiconductor manufacturing are based on bulk substrates. The integration of micro- and nanoelectronic circuits and memory devices uses substrates of the optimal material processed more or less intricately and costly respectively. The processing mostly belongs to top-down fabrication techniques, whose performance is dependent on lithographic structuring exceedingly. Furthermore the total process cost is also dominated by lithography up to 35% because of the use of advanced optical lithographic techniques [1]. Many efforts have been spent on decreasing critical dimensions of the lithography down to 40 nm, resulting in switching over to e-beam or EUV (extreme ultraviolet) lithography. Hence, if one could devise processing techniques, which still involve low-complex optical lithography, nanometer scaled electronics can be produced cost-effectively at high yield.

Various technological proposals base on bottom-up approaches. Basically, the deposition of crystalline material through self-assembly has been pioneered [2],[3], just as well as the deposition of CNTs (carbon nanotubes) [4]-[6] or nanowires. However, all these approaches are limited profoundly in terms of circuit manufactur-

ing. In addition to the control of wire size, surface states of nanowires, shape and chirality of CNTs, control of position is complicated or even impeded [7]-[10].

Other approaches focus on techniques involving nanocrystallite semiconductors. In contrast to devices made of thin films of *nc-Si* [11], this paper concentrates on devices formed by single silicon nanoparticles connected in parallel within metal nanogaps. The conduction path crosses one nanoparticle only. If the dimension of the nanogaps matches to the particle diameter, there is no need for further process steps than the application itself in order to localize the *nc-Si* within the gaps efficiently. The structuring of the metal nanogaps, which is essential for the adjustment of the gap width to the particle diameter, only requires optical lithography. Once the nanoparticles are placed into the nanogaps, the *nc-Si* can be characterized and used as a controllable, semi-conducting section afterwards.

2 EXPERIMENTAL DETAILS

As mentioned before this approach bases neither on thin films of *nc-Si* nor on single particles. In fact, it utilizes metal nanogaps for localization centers of nanoparticles and their side-walls for contacts to the nanoparticles. A dielectric layer underneath the metal nanogap layer insulates the *nc-Si* from silicon substrate. The schematic cross-section of the device is shown in Fig. 1. According to the nomenclature of transistor geometries, in the following the gap length and width are defined in transverse and longitudinal direction, respectively.

2.1 Fabrication of Metal Nanogaps

The technique used for the fabrication of the metal nanogaps is not to be revealed in this paper, but will be published elsewhere. Some remarkable features are mentioned in order to highlight the advantages over other approaches using e-beam lithography [12], though. The metal nanogaps can be produced on a standard silicon wafer uniformly. The gap length is freely adjustable down to 30 nm. At the same time the width is adjustable down to 1 μm , limited by the optical lithography. This dimensional range allows to apply various sizes of nanoparticles. The metallization is virtually arbitrary, so

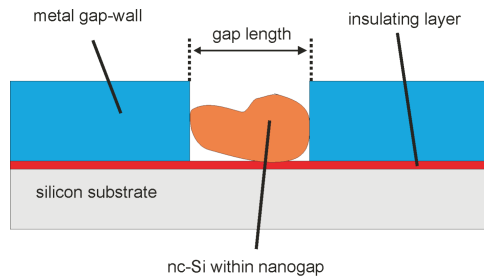


Figure 1: Schematic cross-section of the proposed device

other kinds of nanoparticles can be applied for further research instead. Figure 2 shows an example of a metal nanogap as described. The metal nanogaps are fabri-

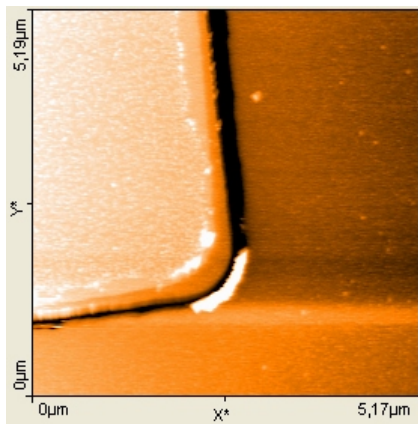


Figure 2: AFM-Image (contact-mode) of topography of metal nanogap. The metallization is made of gold. Gap length extends to 70 nm due to the tip effects. Maximum gap depth is about 50 nm.

cated on a two-layered dielectric subsurface insulating metallization from silicon substrate. The bottom layer is made up of about 15 nm of thermally grown silicon dioxide. Likewise, 15 nm of silicon nitride are deposited from ammonia and triethylsilane by LPCVD.

2.2 Application of Silicon Nanoparticles

One highlighting advantage of this approach is the simple way of application of silicon nanoparticles. The nc-Si is available in ethanol dispersion of diverse concentrations. The colloidal nc-Si has a size distribution of the agglomerates of 60–90 nm measured with dynamical light scattering. The primary particle size is 16–20 nm, determined by x-ray diffraction and TEM respectively. Therefore, the metal nanogaps are matched to the size of medium diameter.

Before the real application, the nanoparticles pass through a pre-treatment in an ultrasonic bath stirring the sample. Using a standard spin-coater nc-Si is spun on the nanogaps and subsequently baked to remove the residual ethanol. The nc-Si is distributed randomly within the nanogaps. AFM analysis determines an approximation of a medium nanoparticle line density $\lambda_l = 1 \mu\text{m}^{-1}$.

Because of the exceeding importance of interfaces between the walls of the metal nanogaps and the nc-Si, the sample has to be annealed afterwards in order to improve the electrical contact. Annealing temperature depends on the metal, which is being used, and its optimal conditions to form silicide contacts [13]–[15].

3 RESULTS AND DISCUSSION

Although many metals and different types of silicon nanoparticles are applicable, the following results refer to aluminum/nc-Si/aluminum-devices with gap lengths of about 60 nm. Secondary, the nc-Si is inherently undoped.

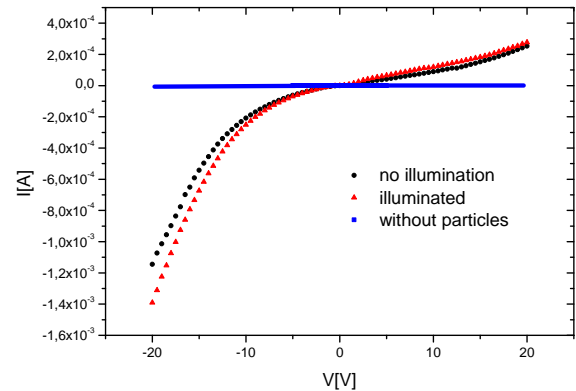


Figure 3: Light-dependent I-V characteristics of silicon nanoparticles within an aluminum nanogap of 60 nm length. Circles (black) represent data points of measurement without illumination, triangles (red) of illuminated measurements and squares (blue) of reference measurement without particles.

After spinning-on the silicon nanoparticles verification of deposition within the nanogaps was done. On this, I-V characteristics are measured illuminated, neither illuminated nor with nanoparticles acting as reference (Fig. 3). The samples without nanoparticles, however, are treated by spin-on of ethanol subsequently baked. The sample was lighted by a conventional halogen lamp because of no necessity for monochromatic light. The I-V characteristics obviously depend on in-

cidence of light. The photons increase the generation rate of charge carriers. Hence, the current increases, too. This result evidences the existence of nanoparticles within the nanogaps and working contacts. Without any particles there is a high insulation resistance of 30 GΩ between both gap contacts suggesting no influence of ethanol used as dispersing agent.

Eye-catching, the curves are formed asymmetrically. It is supposed to be reasoned by unknown and potentially asymmetrical alignment partly. As remarkable as the curve form, the devices grant relatively high currents up to 2 mA. The results correspond to other approaches made on both thin films and single nanoparticles qualitatively [16],[17].

In addition to the verification of semiconducting nano-

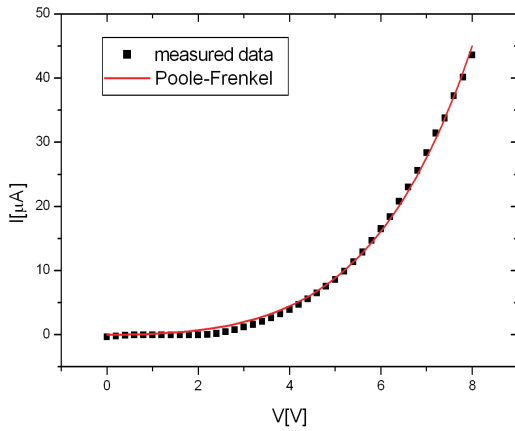


Figure 4: I-V trace of an aluminum/nc-Si/aluminum-device at medium strength of the electric field. The solid red line represents the best curve fit (Eq. (1)), experimental values are marked by filled points.

particles within the metal nanogaps, the nanogaps represent a well-working tool for characterization of the nanoparticles. An approximation of the doping concentration can be carried out as well as the modeling of conductance mechanisms. Although both properties play an important role in FET applications, this paper focuses on conductance mechanisms only, but mentions the possibility for doping analysis. The conductance characteristics are modeled voltage-dependently by sectioning in two ranges of electric field strength. Due to the trap density, which is expected to be relatively increased, hopping transport dominates the conduction mechanism for medium electric field strength. The Poole-Frenkel-effect is described by

$$I \propto V \cdot \exp \left(\frac{2a\sqrt{V}}{T} - \frac{q\phi_B}{kT} \right), \quad (1)$$

where T is the temperature, ϕ_B the contact barrier height and $a = \sqrt{\frac{q}{4\pi\epsilon d}}$ with the permittivity ϵ and the length d [18].

As shown in Fig. 4 the conduction mechanism fits to the Poole-Frenkel-effect well. Additionally the curve fitting leads to the determination of the barrier height with 0.53 eV corresponding to [18] in consideration of unknown density of surface-states and influence of potential grain-boundaries within the nc-Si.

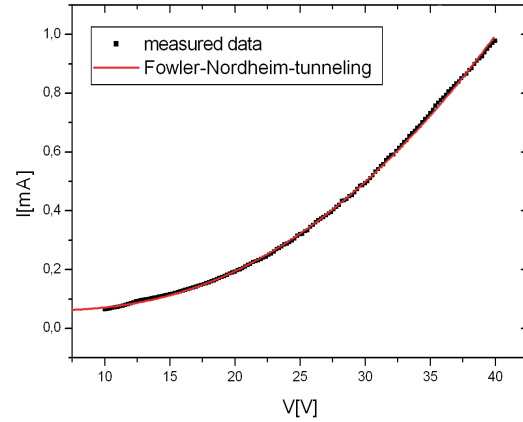


Figure 5: I-V trace of an aluminum/nc-Si/aluminum-device at high strength of the electric field. The solid red line represents the best curve fit (Eq. (2)), experimental values are marked by filled points.

For high strengths of the electric field, the transport mechanisms are not dependent on traps anymore, but on sufficient energy for tunnelemission:

$$I \propto V^2 \cdot \exp \left(\frac{-b}{V} \right) \quad (2)$$

with the positive constant b , which is independent of the applied voltage or the temperature. The experimental data and the best curve fit is plotted in Fig. 5.

Regarding the observed conduction and the barrier parameters, reasonable contacts between the nc-Si and the metallization are concluded. Starting from this, the applicability for FET applications is studied. As aforementioned, a dielectric layer of sufficient thinness insulates the metal nanogaps from the silicon substrate. Applying a voltage to the substrate functionalizes it to a kind of gate, which allows induction of an electric field into the nanoparticles. Hence a conduction channel with lowered resistance is expected to be formed. Indeed, control of the channel conductance can be obtained as shown in Fig. 6. The device does obviously not turn off adequately reasoned by suboptimal positions of

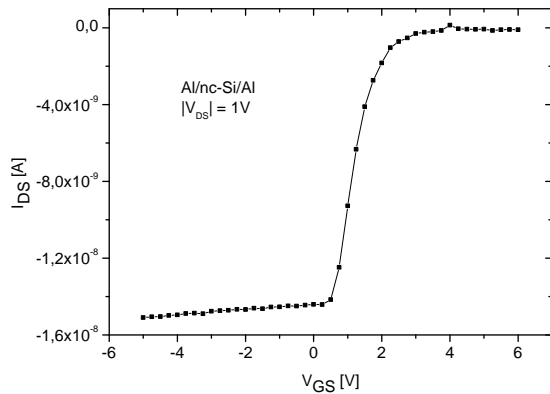


Figure 6: Input characteristics of an aluminum/nc-Si/aluminum-device. Due to an insufficient gate dielectric, voltage has reverse polarity. Data points are interconnected for heightened recognizability.

the nanoparticles. The cut-off current is about 10^{-10} A. A forward current of $2 \cdot 10^{-8}$ A reveals an ON/OFF-current-ratio of $2 \cdot 10^2$.

In the face of circuit integration, this technique surpasses latter approaches in terms of alignment and process complexity. The metal nanogaps can be fabricated at defined positions without any need for nonoptical lithography [19] or high dependence on statistical distribution of nanoparticles, which are synthesized in situ [20].

4 SUMMARY

A simple technique for the application of nanoparticles linked to metal nanogaps was presented as well as the forming of electrical contacts between the metallization and the nanoparticles. In particular, silicon nanoparticles were used for a semiconducting region between the aluminum electrode pair. It was shown, that the contacting succeeded and was improved by subsequent thermal annealing. Finally a proof of suitability for the usage in FET applications was given. The results evidences control over the channel conductance in principle.

5 ACKNOWLEDGEMENT

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