Compact modeling and performance analysis of Double-Gate MOSFET-based circuits

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ABSTRACT

This paper presents the implementation in an analog IC circuit simulator (Eldo™) of a compact model for symmetric Double-Gate (DG) MOSFET and the evaluation of performances of simple DG-based circuits. A compact model for intrinsic long channel DG devices including analytical drain current and node charges for both n- and p-channel DG transistors are implemented in Eldo. The model is firstly validated by DC numerical simulations in terms of drain current. Secondly, the transient characteristics of DG-based inverters and ring oscillators are simulated in Eldo. The inverter time responses as well as the inverter delays are finally compared to numerical results obtained via a mixed-mode simulation approach.

Keywords: Double-Gate MOSFET, drain current, node charges, inverter delay, ring oscillator, circuit simulation

1 INTRODUCTION

Double-Gate (DG) MOS transistors and related multiple-gate device architectures are nowadays widely identified as one of the most promising solutions for meeting the roadmap requirements for the end-of-the-roadmap integration [1-2]. One of the identified challenges for the developing of multi-gate devices remains the development of compact models dedicated to circuit simulation [3]. Although the operation of DG transistor is similar to the conventional MOSFET, the physics of DG MOSFET is more complicated. Therefore, new compact models, dedicated to the specific task of circuit simulation, have to be developed for DG devices [3]. The aim of this work is the implementation in an analog IC circuit simulator (Eldo™) of a compact DG MOSFET model and the evaluation of performances of simple DG-based circuits. Recently, we have developed an extended compact model [4] (based on the compact model presented in [5]) for intrinsic long channel devices including analytic drain current, node charges and also transconductances and intrinsic capacitances. In this work, we implement drain current and node charges for both DG NMOSFET and PMOSFET in Eldo. Drain current is validated by DC numerical simulations (using the Atlas™/Silvaco module [6]). In a second step we simulate in Eldo the transient characteristics of both inverters and ring oscillators composed of several DG MOSFETs. The inverter time responses as well as the inverter delays have been also compared with numerical results obtained using the module Mixed-Mode/Silvaco [6] for long channel DG MOSFET.

2 DG MOSFET COMPACT MODEL

The model is developed for a symmetric DG MOSFET with long channel and intrinsic Si film. Figure 1 schematically shows the geometrical parameters and the bias conditions of the DG structure. Also shown in Figure 1 are the key elements needed for the model implementation in a circuit simulator: the drain current I_{DS} and the different node charges (source – Q_S, drain – Q_D and gate – Q_G) as a function of the terminal polarizations V_G, V_S and V_D.

2.1 Analytical drain current

Circuit simulators need analytic expression of current depending on node polarizations. In this work, we first consider an analytical drain current originally given in [5]:

$$I_{DS} = \mu \frac{W}{L} \frac{4\varepsilon_{Si}}{t_{Si}} \left(\frac{2kT}{q} \right)^2 \left(g_r(\beta_S) - g_r(\beta_D) \right) \qquad (1)$$

where g_r function is described by:

$$g_r(\beta) = \beta \tan\beta - \frac{\beta^2}{2} + r\beta^2 \tan^2\beta \qquad (2)$$

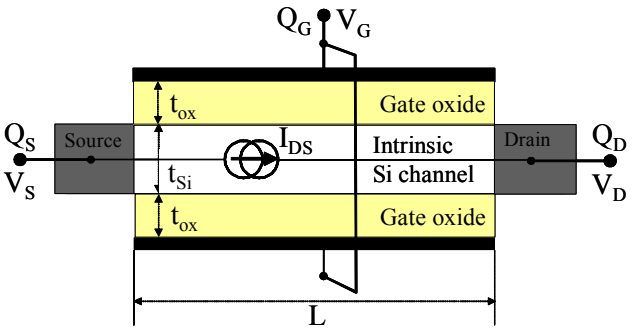

Figure 1: Schematic symmetrical DG MOSFET and main parameters used in this work.

$$r = \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox}} \quad (3)$$

The analytical drain current Eq. (1) does not explicitly depend on node biases: it rather depends on the two parameters β_S and β_D given by the following equations:

$$f_r(\beta_S) = \frac{q}{2kT}(V_G - V_0 - V_S) \quad (4)$$

$$f_r(\beta_D) = \frac{q}{2kT}(V_G - V_0 - V_D) \quad (5)$$

where f_r function and parameter V_0 are given by:

$$f_r(\beta) = ln\,\beta - ln(cos\,\beta) + 2r\beta\,tan\,\beta \quad (6)$$

$$V_0 = \phi_{ms} + \frac{2kT}{q} ln\left[\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}kT}{q^2 n_i}}\right] \quad (7)$$

and Φ_{ms} is the workfunction difference between the gate and the Si channel.

2.2 Node charge model

Our node charge model is based on the inversion charge along the channel. This inversion charge density is given by [5]:

$$q_i(x) = 2\varepsilon_{Si}\left.\frac{d\psi}{dy}\right|_{y=t_{Si}/2} = 2\varepsilon_{Si}\frac{2kT}{q}\frac{2\beta}{t_{Si}}tan(\beta) \quad (8)$$

where the parameter β depends on the position x through the quasi-Fermi potential by the following expression:

$$f_r(\beta) = \frac{q}{2kT}(V_G - V_0 - V_F) \quad (9)$$

To obtain the total inversion charge, Eq. (8) has to be integrated from 0 to L. This requires knowing the variation of the electron quasi-Fermi potential in the horizontal direction, which governs the distribution of the inversion charge. We adopt here the expression of $V_F(x)$ inspired from [7] which has been adapted and validated by numerical simulation for long channel DG MOSFETs:

$$V_F(x) = V_S - \alpha(V_{GS}, V_{DS})\frac{kT}{q} \times$$

$$\times ln\left[1 + \left(exp\left(-\frac{q}{kT}\frac{V_{DS2}(V_{DS})}{\alpha(V_{GS}, V_{DS})}\right) - 1\right)\frac{x}{L}\right] \quad (10)$$

where $V_{DS2}(V_{DS})$ is a smooth function given by:

$$V_{DS2}(V_{DS}) = V_{DS} - \frac{1}{2}\left(V_{DS} - V_1 + \sqrt{(V_{DS} - V_1)^2 + \varepsilon^2}\right) \quad (11)$$

and $\alpha(V_{GS}, V_{DS}) = \alpha(V_{GS}) \times \alpha(V_{DS})$ is the product of the two following expressions:

$$\alpha(V_{GS}) = 1 + 50\frac{kT}{q} ln\left(1 + exp\left(\frac{q}{2kT}(V_{GS} - V_2)\right)\right) \quad (12)$$

$$\alpha(V_{DS}) = 1 + 34\frac{kT}{q} ln\left(1 + exp\left(-\frac{q}{2kT}(V_{DS} - V_3)\right)\right) \quad (13)$$

with V_1=0.6V, V_2=0.56V, V_3=-0.52V are fitting parameters for the structure L=1µm, t_{Si}=5nm and t_{ox}=1.5nm.

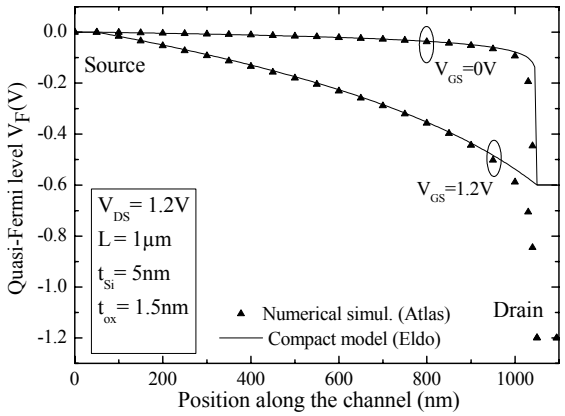

Figure 2: Profile of the quasi-Fermi level along the channel (x-axis) for two values of the gate voltage: V_{GS} =0V and V_{GS}=1.2 V; comparison between compact model and numerical simulation.

The quasi-Fermi potential distribution given by eq. (10) for long channel DG MOSFETs has been extensively verified by numerical simulation using Atlas/Silvaco. Figure 2 shows a good agreement between data obtained with both the compact model and numerical simulation for L=1µm, t_{Si}=5nm and t_{ox}=1.5nm in off-state (V_{GS}=0V) and in on-state (V_{GS}=1.2V). We have also investigated the influence of L, t_{Si} and t_{ox} on $V_F(x)$. Numerical simulations show that $V_F(x)$ profiles vary very slightly when t_{Si} and t_{ox} vary. When reducing the channel length, the model remains valid until L=200nm for t_{Si}=5nm.

Once $V_F(x)$ is obtained, the total inversion charge is then given by:

$$Q_I = \int_0^L q_i(x)dx \quad (14)$$

The node charge model is based on a classical charge sharing method to obtain the source charge Q_S and the drain charge Q_D [4]:

$$Q_S = \int_0^L \left(1 - \frac{x}{L}\right) q_i(x)dx \quad (15)$$

$$Q_D = \int_0^L \frac{x}{L} q_i(x)dx \quad (16)$$

The gate charge is finally calculated from the device neutrality condition that leads to:

$$Q_G = -Q_I \quad (17)$$

Figure 3 represents the three nodes charges versus the drain-to-source voltage. We observe that for V_{DS}=0V, the total inversion charge is equally shared between source and drain regions. For high V_{DS}, Q_S contributes to ~60% and Q_D contributes to ~40% of the inversion charge.

It is important to note that our compact model is completely continuous over all operation regimes and the drain current and node charges equations are derivable and their derivatives are also continuous over all bias regimes. We have also verified that the source and the drain electrodes can be permuted.

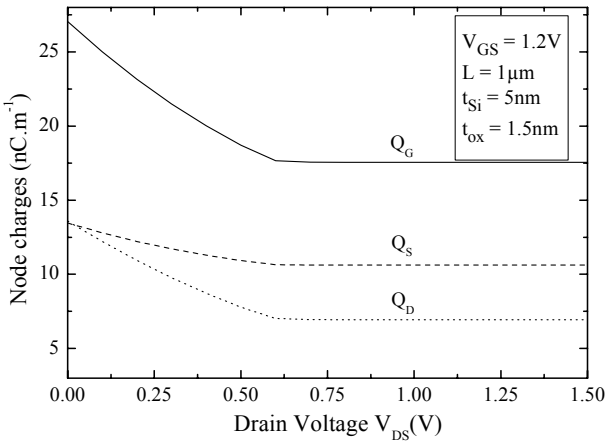

Figure 3: Variation of node charges as a function of V_{DS} for intrinsic long-channel symmetrical DG NMOSFET.

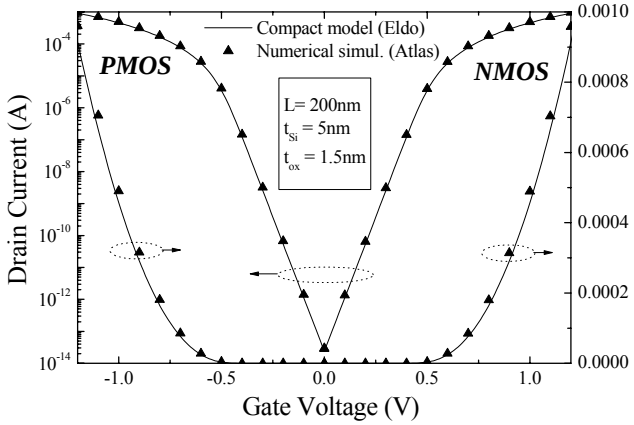

Figure 4: $I_D(V_G)$ characteristics for both n-channel and p-channel DG MOSFET: comparison between numerical simulation and compact model.

3 IMPLEMENTATION OF DG MOSFET MODEL IN ELDO

The DG NMOSFET model described previously has been implemented in Eldo using the analytical expression of the drain current (Eq. 1) and the expressions of the different node charges (Eqs. 14-17). A similar model has been considered for p-channel structures. The main difference between the two models comes from the permutation between the source and drain biases. In the analytical expression of the drain current (Eq. 1), this difference results in a new determination of β_S and β_D. For p-channel devices, Eq.4-5 thus becomes:

$$f_r(\beta_S) = \frac{q}{2kT}(V_S - V_0 - V_G) \quad (18)$$

$$f_r(\beta_D) = \frac{q}{2kT}(V_D - V_0 - V_G) \quad (19)$$

The quasi-Fermi potential is also reevaluated:

$$V_F(x) = V_S + \alpha(V_{GS},V_{DS})\frac{kT}{q} \times ln\left[1+\left(exp\left(\frac{q}{kT}\frac{V_{DS2}(V_{DS})}{\alpha(V_{GS},V_{DS})}\right)-1\right)\frac{x}{L}\right] \quad (20)$$

with the new expressions of Eq. (11) to (13):

$$V_{DS2}(V_{DS}) = V_{DS} - \frac{1}{2}\left(V_{DS} - V_1 - \sqrt{(V_{DS}-V_1)^2+\varepsilon^2}\right) \quad (21)$$

$$\alpha(V_{GS}) = 1 + 50\frac{kT}{q}ln\left(1+exp\left(-\frac{q}{2kT}(V_{GS}-V_2)\right)\right) \quad (22)$$

$$\alpha(V_{DS}) = 1 + 34\frac{kT}{q}ln\left(1+exp\left(\frac{q}{2kT}(V_{DS}-V_3)\right)\right) \quad (23)$$

with V_1=-0.6V, V_2=-0.56V, V_3=0.52V are fitting parameters for the structure L=1µm, t_{Si}=5nm and t_{ox}=1.5nm.

The DC characteristics of long channel DG MOSFETs (n- and p-channel) obtained with Eldo are compared to numerical simulation data in Fig. 4. This figure shows the excellent agreement between Eldo and Atlas/Silvaco results obtained on DG devices with a gate length L=200nm, a Silicon film thickness t_{Si}=5nm, and an oxide thickness t_{ox}=1.5nm. As the analytical drain current model is dedicated to long channel devices, we obtain a very good agreement between the model and numerical simulation for structure with channel longer than 200nm (t_{Si}=5nm and t_{ox}=1.5nm). A constant value for the electron mobility in the channel has been considered in both compact model and Atlas/Silvaco simulation. The model can be further enhanced by considering a realistic mobility model.

4 ANALYSIS OF DG INVERTERS AND RING OSCILLATORS

In the following, we used our compact model to simulate transient responses of DG-based inverters and ring oscillators. In the case of DG inverters, we compared the Eldo results with numerical simulated data (using the mixed-mode approach in which both n- and p-channel structures are fully numerically simulated). Figure 5a and 5b compares the responses of inverters to a rectangular input voltage obtained by Eldo and Atlas/Silvaco. The transient output given by Eldo very well fits data obtained with the mixed-mode approach for both gate length L=1µm and L=200nm. After this first validation step, we studied the inverter delay variation as a function of the gate length and oxide thickness: results for different L are reported in Table 1 and results for different t_{ox} are given in Table 2. As expected, the delay increases with the channel length because the inversion charge increases, and the delay increases when the oxide thickness is reduced (the gate capacitance is inversely proportional to t_{ox}). The delay values, as extracted from Eldo simulation, are very close to that deduced from Atlas/Silvaco (the error is less than 10%). We have also tried to compare the variation tendency

of the delay obtained by numerical (Atlas) and circuit simulation (Eldo) approaches. But for large t_{Si} values (typically > 15 nm), it must be noted that short channel effects, not included in this model, must be taken into account: this explains why no clear tendency of the variation of the delay with t_{Si} can be presently derived.

Finally, we investigated the response of 15-stage ring oscillators to a 100µA pulse input. Figure 6 illustrates the variation of the output voltage for two cases: (1) L=200nm and t_{Si}=5nm; (2) L=500nm and t_{Si}=10nm as obtained by Eldo simulation. Note that the simulation of a 15-stage ring oscillator is not possible in the mixed-mode approach because of the limited number of devices (10) which can be simultaneously simulated in 2D. Figure 6 shows that the oscillation frequency increases when the channel length decreases, because the propagation delay over the circuit is strongly reduced.

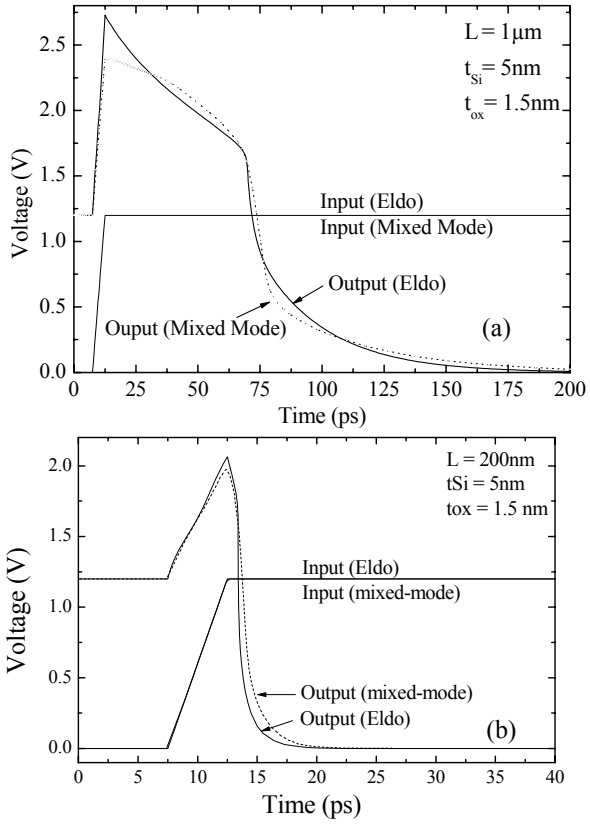

Figure 5: Transient analysis of a DG-based CMOS inverter: comparison between mixed-mode and compact model (Eldo) simulation for (a) L=1µm and (b) L=200nm.

Table 1: Comparison between inverter delay as extracted from mixed-mode (Silvaco) and from Eldo (compact model) for different gate lengths L (t_{ox}=1.5nm, t_{Si}=5nm).

Inverter delay (ps)		
	Compact model (Eldo)	Mixed-Mode (Atlas)
L=200nm	3.81	4.26
L=500nm	19.24	18.9
L=1µm	74.85	69.5

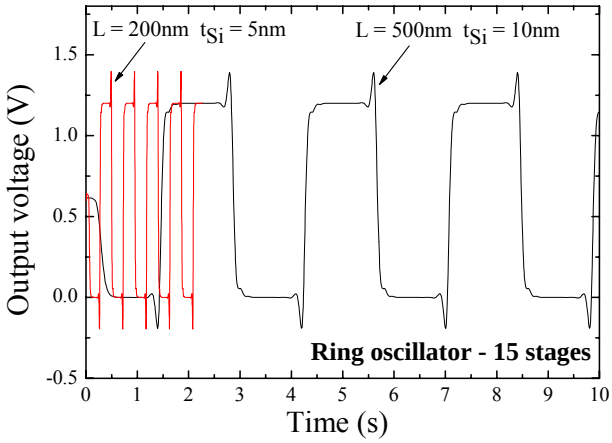

Figure 6: Transient analysis of a 15-stage ring oscillator composed of DG MOSFETs obtained by Eldo simulation.

Table 2: Comparison between inverter delay as extracted from Mixed-Mode (Silvaco) and from Eldo for different oxide thicknesses t_{ox} (L=1µm and t_{Si}=5nm).

Inverter delay (ps)		
	Compact model (Eldo)	Mixed-Mode (Atlas)
t_{Si}=1nm	75.4	70.75
t_{Si}=1.5nm	74.9	65.9
t_{Si}=2nm	73.9	69

5 CONCLUSION

In this work, we demonstrated the implementation in an analog IC circuit simulator (Eldo™) of a compact DG MOSFET model and the evaluation of performances of simple DG-based circuits. The compact model for intrinsic long n-channel and p-channel DG devices (including the analytical expression of the drain current and the node charges) was firstly validated by numerical simulation. In a second time, the model was implemented in Eldo and the transient operation of CMOS inverters has been analyzed and compared with numerical results obtained by 2D mixed-mode simulation. Finally, the compact model has been used to successfully simulate the transient response of a 15-stage ring oscillator.

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