Compact model of drain-current in Double-Gate MOSFETs including carrier quantization and short-channel effects

X. Loussier[1], D. Munteanu[1], J.L. Autran[1*], S. Harrison[1,2], R. Cerutti[2]

[1]*Laboratory for Materials and Microelectronics of Provence (L2MP), 49 rue Joliot-Curie 13384 Marseille France*
[*]*Also with Institut Universitaire de France (IUF)*
[2]*STMicroelectronics, 850 rue J. Monnet, 38926 Crolles France*
E-mail: daniela.munteanu@l2mp.fr, Phone: +33 4 96 13 98 19, Fax: +33 4 96 13 97 09

ABSTRACT

A continuous compact model for the drain current, including short-channel effects and carrier quantization in Double-Gate (DG) MOSFET is developed. The model is particularly well-adapted to ultra-scaled devices, with short channel lengths and ultra-thin silicon films. An extensive comparison step with 2D quantum numerical results fully validates the model. The model is shown to reproduce with an excellent accuracy experimental drain current in Double-Gate devices. The drain current model is supplemented by a node charge model and the resulting DG model is successfully implemented in Eldo^{TM} IC analog simulator, demonstrating the application of the model to DG-CMOS based circuit simulation.

Keywords: Double-Gate MOSFET, drain current, short-channel effects, carrier quantization

1 INTRODUCTION

Double-Gate (DG) structure has been in the last years the object of intensive research and an impressing number of studies have confirmed its enormous potentiality to push back the integration limits to which conventional devices are subjected [1-4]. Although the operation of DG transistor is similar to the conventional MOSFET, the physics of DG MOSFET is more complicated. Moreover, physical phenomena such as 2D electrostatics or carrier quantization have to be considered, since DG structure will be precisely used to design very integrated devices (with short channel and extremely thin films). Therefore, new compact models, dedicated to circuit simulation, have to be developed for DG MOSFET [4]. Several interesting models have been proposed for the classical (i.e. without quantum effects) drain current in long channels DG [3-7] or for short channel DG operating in the subthreshold regime [8]. Carrier quantization effects have been considered for the first time in [9]. In this work, we propose a compact model which combines short-channel with quantum-mechanical effects and applies to all operation regimes. In addition the model is continuous over all gate and drain bias range, which makes it very suitable for implementation in circuit simulators. The development is based on the calculation of the 2D potential distribution in the device taking into account the quantum-evaluated inversion charge. A full 2-D quantum mechanical numerical simulation code [10] is used for completely validating the model. The drain current as predicted by the model is compared with experimental data measured on scaled DG devices fabricated using the SON process [11-12]. Finally, the model is successfully implemented in Mentor Graphics Eldo^{TM} IC analog simulator.

2 DRAIN CURRENT MODELING

Figure 1a shows the schematic of a symmetric DG structure and the band diagram in horizontal cross-section is illustrated in Figure 1b, together with the first energy subbands. The drain current modeling starts with the calculation of the 2D potential distribution in the device. For this purpose several methods have been proposed, the most complete being the evanescent-mode analysis, where the potential is divided into two different parts $\Psi(x,y) = \Psi_L(y) + \Psi^*(x,y)$ [13]. The first term represents the long channel solution and the second term takes into account short-channel behavior. This last term is then approximated by a retaining only the lowest-order mode from a Fourier expansion of modes. The method can be very powerful for taking into account short-channel effects in the evaluation of the threshold voltage [13], but the mathematical development is very complicated. For simplifying the calculation, in this work we assume the following dependence for the potential:

$$\Psi(x,y) = \Psi_S(x) \times A(x,y) \tag{1}$$

where Ψ_S is the surface potential and A(x,y) is a vertical distribution envelope function. The 2D potential distribution is thus obtained by modulating the surface potential by an envelope function containing the potential dependence in the vertical direction. A(x,y) is then given:

$$A(x,y) = \frac{B(x,y)}{B(x,y=0)} \tag{2}$$

where B(x,y) is calculated as in [14]:

$$B(x,y) = \psi_0 - \frac{2}{\beta} ln\left\{cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}} e^{\frac{\beta(\psi_0 - V_F(x))}{2}} (y - \frac{t_{Si}}{2})\right]\right\} \tag{3}$$

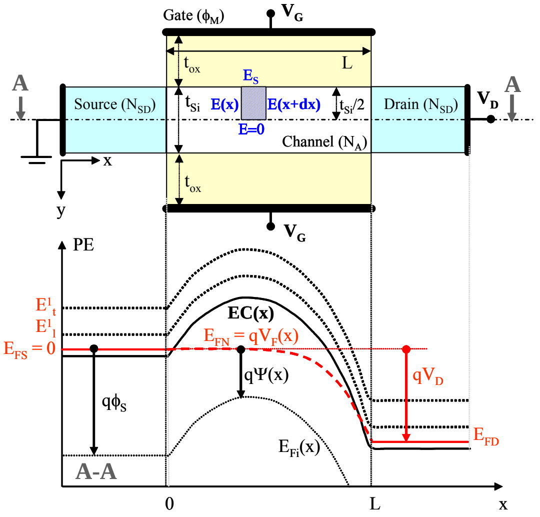

Figure 1. Schematic symmetrical DG MOSFET and band diagram in a horizontal cross-section.

where β=q/kT, $V_F(x)$ is the quasi-Fermi level and ψ_0 is calculated using the following equations [14]:

$$\psi_0 = U - \sqrt{U^2 - (V_G - V_{FB})\psi_{0\,max}} \qquad (4)$$

$$U = \frac{1}{2}\left[(V_G - V_{FB}) + (1+r)\psi_{0\,max}\right] \qquad (5)$$

$$\psi_{0\,max} = V_F(x) + \frac{1}{\beta} ln\left(\frac{2\pi^2\varepsilon_{Si}kT}{q^2 n_i t_{Si}^{\;2}}\right) \qquad (6)$$

In eq. (5) r is a smoothing parameter weakly dependent on t_{ox}, t_{Si} and V_F, which is determined as in [15].

For calculating the vertical distribution envelope function A(x,y), the expression of $V_F(x)$ is needed. An analytical expression of $V_F(x)$ has been proposed in [15] for bulk MOSFET. We adopted here a quasi-empirical expression inspired from that proposed in [15] and extensively verified by numerical simulation:

$$V_F(x) = \frac{2kT}{q}\frac{m}{n} ln\left[\left(exp\left(\frac{V_D(m/n)^{-1}}{kT/q}\right)-1\right)\left(\frac{x}{L}\right)^{\frac{c}{V_G - V_{FB}}} + 1\right]^{-1} \times (at_{Si})^{\frac{V_D}{3c}} \qquad (7)$$

$m/n = 2 + b\left(V_G - V_{FB}\right)$, $a = 0.2\mathrm{nm}^{-1}$, $b = 7.5\mathrm{V}^{-1}$, $c = 1\mathrm{V}^{-1}$.

The last term to be calculated for obtaining the 2D potential distribution is the surface potential. For obtaining the expression of $\Psi_S(x)$, the Gauss's law is applied to the particular closed surface shown in Figure 1a [11]:

$$-E(x)\frac{t_{Si}}{2} + E(x+dx)\frac{t_{Si}}{2} - E_S(x)dx = -\frac{qN_A t_{Si}}{2\varepsilon_{Si}} - \frac{q_i(x)}{2\varepsilon_{Si}} \qquad (8)$$

In the right hand side, the first term corresponds to the depletion charge (N_A is the channel doping) and the second term is the mobile inversion charge density, given by the integration of the electron charge over the entire Si film:

For very thin films used in this work (<15nm), electric field E(x) can be approximated as $E(x) \approx -\frac{d\psi_S(x)}{dx}$ [11]. After some algebraic manipulations the following differential equation is obtained for Ψ_S:

$$\begin{aligned}\frac{d^2\psi_S}{dx^2} - \frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}\psi_S &= \\ &= \frac{1}{\varepsilon_{Si}t_{Si}}\left[qN_A t_{Si} - 2C_{ox}(V_{GS} - V_{FB} - \phi_F) + q_i\right]\end{aligned} \qquad (9)$$

The analytical solution of equation (9) is given by:

$$\psi_S(x) = C_1\,exp(m_1 x) + C_2\,exp(-m_1 x) - \frac{R(x)}{m_1^2} \qquad (10)$$

with C_1, C_2, m_1 and R(x) calculated for filling the boundary conditions $\Psi_S(x=0)=\phi_S$ and $\Psi_S(x=L)=\phi_S+V_D$:

$$C_{1,2} = \pm\frac{\phi_S\left[1 - exp(\mp m_1 L)\right] + V_D + R(0)\dfrac{1 - exp(\mp m_1 L)}{m_1^{\;2}}}{2\,sinh(m_1 L)} \qquad (11)$$

$$R(x) = \frac{qN_A t_{Si} - 2C_{ox}(V_G - V_{FB} - \phi_F) + q_i(x)}{\varepsilon_{Si}t_{Si}} \qquad (12)$$

$$m_1 = \sqrt{2C_{ox}/(\varepsilon_{Si}t_{Si})}\,,\ \phi_S = (kT/q)ln\left(N_A N_{SD}/n_i^2\right) \qquad (13)$$

In (11), R(0) is calculated considering $q_i(0)$ given by (14) with $\Psi_S(0)=\phi_S$. The inversion charge $q_i(x)$ is quantum-mechanically evaluated using:

$$\begin{aligned}q_i(x) = {}&\frac{qkT}{\pi\hbar^2}\sum_{l,t}\sum_{i} m_{2D}^{t,l} g_{t,l} \\ &\times ln\left[1 + exp\left(-\beta\left(\tilde{E}_{l,t}^{i} + \frac{E_g}{2} - \psi_S(x) + V_F(x)\right)\right)\right]\end{aligned} \qquad (14)$$

where $m_t^*=0.19\times m_0$, $m_l^*=0.98\times m_0$, $g_l=2$, $g_t=4$, β=q/kT, $m_{2D}^{l} = m_t^*$, $m_{2D}^{t} = \sqrt{m_l^* m_t^*}$. In eq. (14) $\tilde{E}^i_{l,t}$ are the energy levels calculated using a standard method for first-order perturbation applied to the energy levels of an infinite rectangular well (as shown in [11]):

$$\tilde{E}_{l,t}^{i} = E_{l,t}^{i} + \Delta E^{i} \qquad (15)$$

where $E^i_{l,t}$ are the energy levels of an infinite rectangular well:

$$E_{l,t}^{i} = \frac{\hbar^2\pi^2 i^2}{2qm_{l,t}^{*}t_{Si}^{2}} \qquad (16)$$

and $\Delta E^i = \left\langle \varphi^i \middle| H \middle| \varphi^i \right\rangle$, where H is the Hamiltonian of the perturbation and ϕ^i are the electron wave functions associated to energy levels $E^i_{l,t}$.

Since $\Psi_S(x)$ given by eq. (10) depends on $q_i(x)$, replacing (10) and (15) in (14) leads to an implicit equation on $q_i(x)$, which is solved numerically for obtaining $q_i(x)$. (10)

The current density (including both the drift and the diffusion components) is expressed as:

$$J = -q\mu n(x,y)\frac{dV_F(x)}{dx} \qquad (17)$$

which is then integrated in y and z directions:

$$I_{ds}(x) = \mu W q_i(x)\frac{dV_F(x)}{dx} \qquad (18)$$

Current continuity requires $I_{ds}(x)$ be independent of x and integrating (18) from 0 to L we obtain:

$$I_{DS} = \mu \frac{W}{L} \int_0^L q_i(x) dV_F(x) \tag{19}$$

In the case of classical calculation of the inversion charge (i.e. without quantum effects)

$$q_i(x) = \int_0^{t_{Si}} q\,ni\, e^{\frac{q}{kT}[(\Psi(x,y) - V_F(x))]} dy \tag{20}$$

the drain current becomes

$$I_{DS} = \mu \frac{W}{L} \frac{kT}{q} \frac{1 - exp\left(-qV_D / kT\right)}{\int_0^L dy \Big/ \left(\int_0^{t_{Si}} n_i e^{q\psi(x,y)/kT} dx \right)} \tag{21}$$

3 MODEL VALIDATION: SHORT-CHANNEL, QUANTUM EFFECTS, VOLUME INVERSION

The model was validated by an extensive comparison with quantum numerical simulation using a full 2-D Poisson-Schrödinger code [10]. In a first step, the potential distribution as given by eq. (1) has been verified. In a second step, the drain current expression has been completely validated by numerical simulation, for channel lengths varying between 30nm and 200nm and film thicknesses from t_{Si}=15nm down to t_{Si}=2nm. A constant mobility is considered in equation (21). Figure 2 shows an example of this validation step on a long channel DG at low and high V_D. Short channel behavior of the quantum drain current is checked in Figure 3: the model reproduces very well the simulation (even in L=30nm), in both weak and strong inversion regimes. The extensive investigation of additional $I_D(V_D)$ curves have shown that the model is completely valid in both linear and saturation regimes. The proposed compact model can easily be used to obtain all main performance indicators of DG MOSFET, such as threshold voltage, subthreshold swing, DIBL, I_{on} and I_{off}.

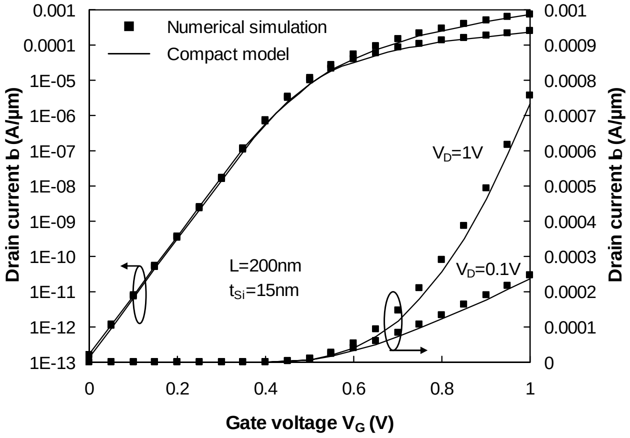

Figure 2. Drain current given by the compact model and comparison with 2D quantum numerical simulation (t_{Si}=15nm, t_{ox}=1nm, L=200nm, midgap gates).

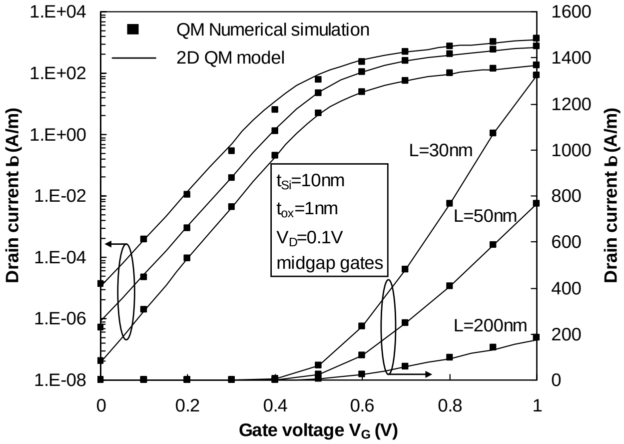

Figure 3. Drain current in short channel devices calculated by 2D QM model and validation by numerical simulation.

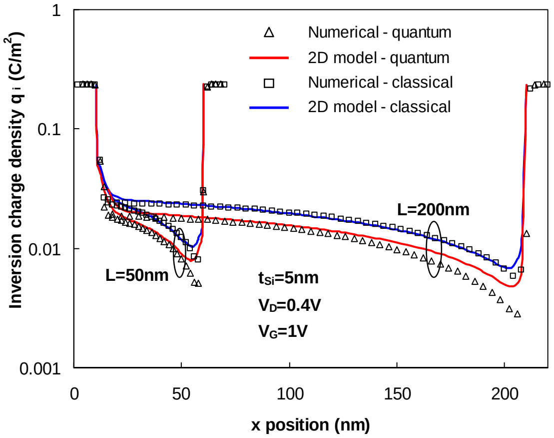

Figure 4. Variation of the inversion charge density $q_i(x)$ in classical and quantum mechanical cases.

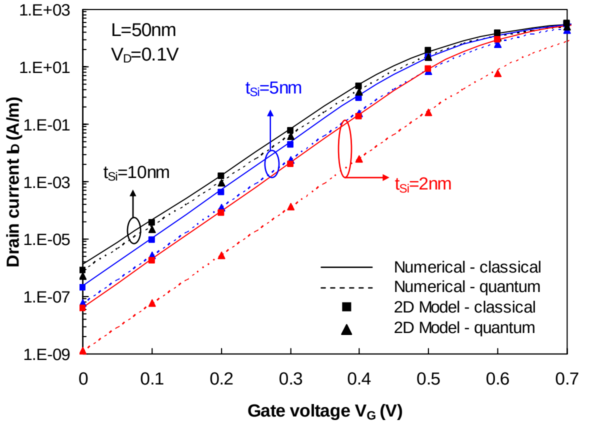

Figure 5. Impact of film thickness on the subthreshold operation: the model perfectly reproduces quantum effects and volume inversion (t_{ox}=1nm, midgap gates).

The validation procedure was continued by an in-depth investigation of the model capability to take into account carrier quantization effects. For this purpose the inversion charge density $q_i(x)$ (in both classical and quantum case, Figure 4) in long and short channels have been compared to numerical results and very good agreement have been found. Further the classical and quantum drain current were calculated as a function of t_{Si} (Figure 5). Note that the 2D QM model perfectly reproduces two essential phenomena: (1) the impact of quantum effects quantum effects, increasingly significant when t_{Si} is scaled down and (2) the drain current dependence on t_{Si} in the subthreshold region (as a manifestation of the volume inversion); above threshold drain current depends much less on t_{Si} [5].

4 COMPACT MODEL VS. EXPERIMENT

Finally, the model was used to fit drain current measured [11-12] on DG devices (Figure 6). The match between experiment and model is very good, especially in the subthreshold regime; above threshold the model slightly overestimates the current due to the use of a constant mobility. For improving the model accuracy the next step will be to consider a realistic mobility model [16].

5 MODEL IMPLEMENTATION IN ELDO^{TM} IC ANALOG SIMULATOR

The drain current model presented previously has been implemented in Eldo IC analog simulator in order to evaluate the performances of simple DG MOSFET-based circuits. For this purpose, the model was firstly supplemented by a charge model including the expressions of charges on the device terminals, using the node charge model (based on the neutrality condition and a classical source-drain charge sharing) presented in [17]. The model has been used further to simulate DC and transient response of a three-stage inverter chain containing DG MOSFETs. Figure 7 shows the time response of the three outputs voltages to a rectangular input voltage, as simulated by Eldo, demonstrating the application of the model to circuit simulation. Other circuits such as 15-stages ring oscillators have also been tested.

6 CONCLUSION

A short channel quantum compact model for drain current in Double-Gate devices has been developed. The model is particularly dedicated to ultra-scaled devices expected at the end-of-roadmap. The development of an analytical expression for the 2D distribution of the potential considering the quantum inversion charge was the starting point of the model. Through an extensive comparison with 2D Poisson-Schrödinger simulation data the model was shown to reproduce with an excellent accuracy the impact on the drain current of short channel effects, volume inversion and carrier quantization. A very good agreement was also obtained with experimental data measured on very integrated devices. Finally, the drain current model supplemented by a node charge model was implemented in Eldo IC analog simulator and the transient simulation of simple DG CMOS-based circuits has been performed.

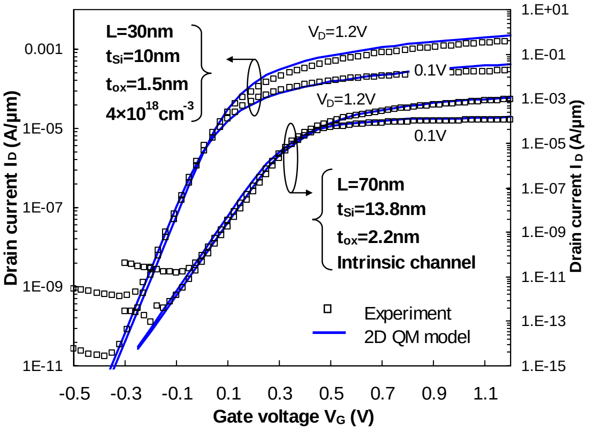

Figure 6. Compact model versus experimental data obtained on GAA/SON devices [11-12].

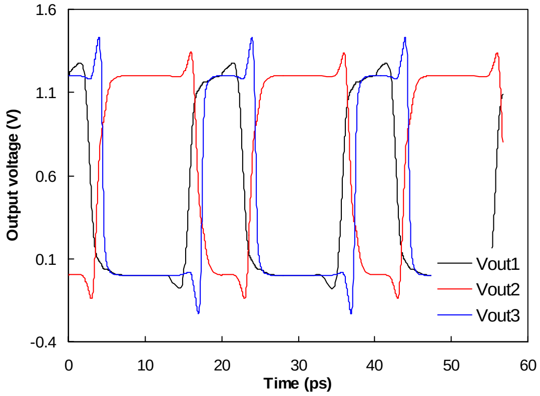

Figure 7. Transient analysis of a three-stages inverter chain containing symmetrical DG MOSFETs.

Acknowledgements

This work was supported by the Network of Excellence SINANO and by the French Ministry of Research (RMNT project "CMOS-DALI").

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