A Defect Model for Metallic Carbon Nanotubes in Cell-based Logic Circuits

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Abstract

This paper presents a model and a corresponding detection technique for nano scaled defects arising from the presence of metallic carbon nanotubes. Using an optimal layout of cells based on Carbon Nanotube Field Effect Transistors (CNTFET) in a circuit netlist, such defects are modeled by traditional *single stuck-at faults* (SSF) and detected by SSF test sets. Simulation results are presented to evaluate the performance of the proposed technique in modeling and detection of metallic CNT defects. It is shown on average 96.77% of metallic CNT defects can be detected for the seven largest ISCAS89 benchmark circuits.

Keywords: Carbon Nanotube, CNTFET, Fault Detection, Defect Modeling, Nanotechnology.

1 Introduction

A carbon nanotube (CNT) is a hollow cylinder composed of one or more layers of carbon atoms which are arranged in a honeycomb lattice form. A nanotube with one layer of carbon atoms is called Single-Wall (SWCNT) while those with multiple layers are called Multi-Wall [1]. Theoretical and experimental research has revealed unique electrical features of SWCNTs such as ability to act as both semiconductor and metal (conductors) [2]. Semiconducting SWCNTs have experimentally been used to construct electron devices similar to conventional Metal Oxide Semiconductor Field Effect Transistors (MOSFET) known as CNTFETs [3][4]. They have shown excellent electrical properties including high transconductance (ability to convert voltage into current) and high on/off current ratio (near optimal switch). CNTFETs are promising nano scaled devices for implementing high performance, highly integrated, and low power circuits [5][6][7]. The main component of a CNTFET is a SWCNT whose conductance is determined by the so-called *chirality* of the tube and is extremely hard to control during manufacturing [8]. Conducting SWCNTs can lead to defective CNTFETs similar to *source-drain short* faults in MOSFETs.

A study on the likelihood of various defects in MOSFET based CMOS has been presented in [9] which has shown more than 40% of defects could not be modeled by SSFs. The first contribution in this work is that, *all m-CNT defects can be modeled by SSFs* given a particular layout style for every cell in the circuit netlist. The second contribution in this work is that, *single m-CNT defects can be detected by the test of the modeled SSF in a logic testing environment.*

The rest of this paper is organized as follows: Section 2 presents preliminaries on the Metallic CNTs and their impact on circuit operation that leads to defects. Section 3 presents how metallic CNT defects can be modeled using SSFs and layout information of the CNT based circuit. Section 4 indicates how the SSF test set of a circuit can be applied for detecting metallic CNT defects and the performance of such test set using benchmark circuits. Section 5 concludes the paper.

2 Metallic CNT Defects

The conductance property of SWCNTs is determined by the diameter and the angle of the atomic arrangement along the tube [10]. The graphene sheet is cut along a *chiral* vector; it is then wrapped around along the cut to form the CNT. The chiral vector $\vec{C}$ is specified in terms of the unit vectors $\vec{V_1}$ and $\vec{V_2}$ by $\vec{C} = n \cdot \vec{V_1} + m \cdot \vec{V_2}$ where n and m are integers. It is known that if $|n - m|$ is divisible by 3, then the tube is metallic (m-CNT), else it is semiconducting (s-CNT)[1]. This suggests that for arbitrary integer values of m and n, the yield of semiconducting CNTs is theoretically at most $\sim 66\%$. The yield of s-CNT is a limiting factor in circuit implementation by CNTs. Consider as an example a chip made of 1000 devices; the chip yield is then 0.66^{1000}, i.e., the probability of all CNTFET devices to be non defective given that the individual CNTs are independently metallic/semiconducting. The resulting chip yield is effectively 0 and rather impractical.

A m-CNT used for a CNTFET device is always conducting, independently of the electric field applied by the device gate. Similar defects are also present in MOSFET based CMOS and they are referred to as stuck-on (SON). SONs are studied within the general category of *bridging faults* (BF) which model defects by shorts (i.e., bridge) between circuit elements such as wires.

[1]When $m = n$, the CNT has a very small bandgap, it is included in the metallic category.

3 Modeling Metallic CNT Defects

In this section, the layout information of a CNTFET based CMOS cell is used for analyzing metallic CNT defects. The layout for a cell can be designed in many ways [11] and several works have addressed the optimal design of cell layouts in terms of area and performance [12]. Optimal cell layouts are often produced in the so-called *line-of-diffusion* style in which two lines of semiconductor are used for implementing the pullup and pulldown transistor networks. Figure 1 (a) shows a generic line-of-diffusion layout with only two semiconducting areas for the CMOS design style of Figure 1 (b). These lines are replaced by CNTs (diffusions) in CNTFET (MOSFET) based CMOS. The top (bottom) line implements the pullup (pulldown) transistor network(s). The output line is conditionally connected to the supply or ground lines (but not both) and the condition is determined by the inputs. The top (bottom) line is always connected to the supply (ground) in at least one point. The output line is always connected to both top and bottom lines in at least one point.

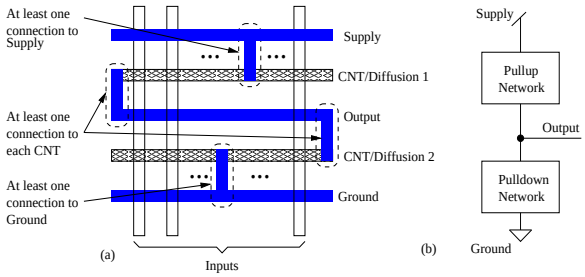

Figure 1: (a) Generic Line-Of-Diffusion layout style (b) CMOS design style

It is easy to see that when the top (bottom) CNT is metallic in a CNTFET based CMOS cell layout, the output will be connected to supply (ground) independent of the inputs. This results in a stuck-at-1 (0) on the output of the CNTFET based cell. Therefore, a single m-CNT in a CNTFET based CMOS cell is modeled by a SSF on the cell output.

Example: Figure 2 shows a NAND2 gate, made of CNTFETs. The layout is a conventional CMOS layout except for the diffusion areas that are replaced by two lines representing the CNTs. When the top CNT is a defective m-CNT, two CNTFETs will be SON. The output will be in contact with the supply. When the bottom CNT is defective, the output will be contacted to the ground. For single intra-gate m-CNTs, the gate output is stuck-at-1/0.

In the line-of-diffusion layout style, transistor networks are represented by a graph in which each transistor is mapped to an edge and its source and drain to two vertices. The graph is undirected as transistors are bidirectional switches. An *Euler* path in either the

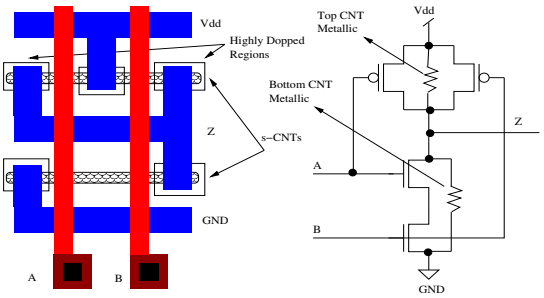

Figure 2: A NAND2 gate using 2 s-CNTs

pulldown or pullup graphs guarantees two lines of semiconducting area[2]. We examine the graph representation of primitive gates (i.e., n-input NAND/NOR) and show that their transistor graphs have an Euler path. This is because *any* logic circuit can be mapped to a netlist of NAND/NOR cells.

Figure 3 and Figure 4 show n-input NAND and NOR transistor lists and the corresponding graph representations. Both graphs have an Euler path (the paths are marked on the graphs). $n = 2k + 1$ (i.e., odd) is assumed in Figure 4; this does not affect the validity and generality of the proposed model. For $n = 2k$, the last edge in the parallel edges will return to the vertex corresponding to the output node (rather than the supply (ground) vertex). Hence, the proposed model is applicable to primitive gates in a CNT based cell library. The layouts are shown in Figure 5. Both layouts show two lines of CNTs. Among them, a m-CNT will connect the output to either supply or ground, thus creating a stuck-at-1/0 fault at the output.

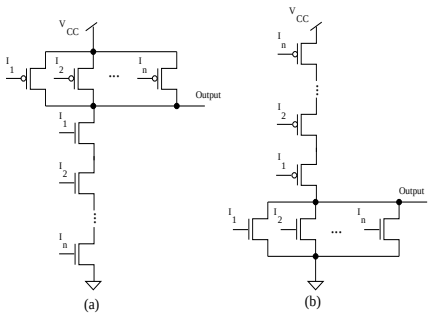

Figure 3: n-input primitive gate transistor list: (a) NAND (b) NOR

4 Detecting Metallic CNT Defects

The detection of SON faults is generally difficult in CNTFET/MOSFET based CMOS due to the intermediate logic values. They imply a supply to ground path,

[2]If both paths have the same edge labeling, the input line order is preserved for pullup and pulldown transistor networks but this is not a necessary condition for two (and only two) lines of semiconducting areas.

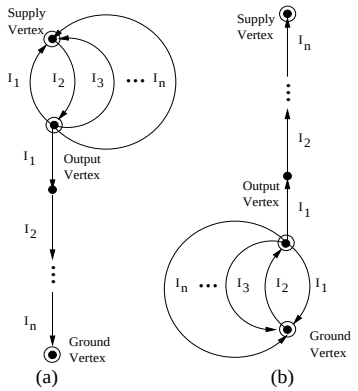

Figure 4: n-input primitive gate graphs: (a) NAND (b) NOR

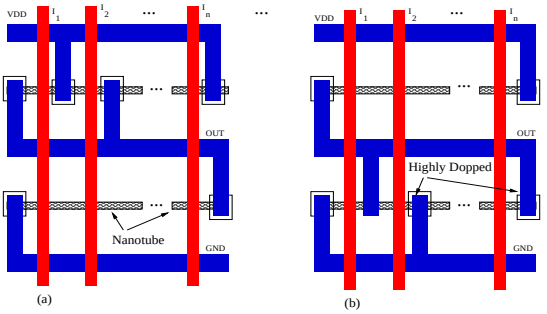

Figure 5: n-input primitive gate layouts in Line-of-Diffusion style: (a) NAND (b) NOR

thus causing an extra current flow; this current can be sensed by a *current supply monitor* (CSM)[3] to detect these faults. CSM is possible in CMOS because the power supply current remains low during steady state (when the inputs/outputs are stable). However for highly integrated circuits, the difference between the steady state current and the excessive current due to a supply-ground path decreases, thus encountering difficulty in the current measurement and assessing the correct outcome as pass/failure. It is more convenient to detect such faults in a a logic testing environment in which a logic discrepancy is activated and propagated to circuit outputs.

Table 1 shows the number of metallic CNT faults and their percentage detected by a SSF test set in the seven largest digital circuits from the ISCAS89 benchmark set. A metallic CNT fault list is compiled for each circuit by selecting one (and only one) CNT and replacing it with a m-CNT. Fault simulation is performed for the fault list using a SSF test set of the circuit. The percentage of detected faults in the metallic CNT fault list is then measured. The SSF test set is the widely used *dynamically compacted test vectors* from MINTEST [13]. The m-CNT defect coverages are not necessarily 100%; this is expected as some of the SSFs are redundant and

[3]Also called IDDQ testing.

	m-CNT Faults		
Benchmark	Count	Detectable	Coverage
s5378	5558	5491	98.7945%
s9234	11194	10569	94.4167%
s13207	15902	15792	99.3083%
s15850	19544	19273	98.6134%
s35932	32130	29282	91.1360%
s38417	44358	44282	99.8287%
s38584	38506	36698	95.3046%
Average	23885	23055	96.77%

Table 1: Performance of SSF Tests for Detection of m-CNT Faults

not detectable. The m-CNTs mapped to these SSFs are therefore not detectable. This is not a problem in practice because these m-CNTs cannot be activated and propagated to the outputs at the same time, i.e., they do not change the normal operation of the circuit.

5 Conclusion

As the electronics of CNT and CNTFETs are being investigated and techniques for reliable synthesis and growth of CNTs with controllable electrical and physical properties are proposed, there is a need for modeling and simulation of CNTFET based circuit behavior when many of these nano-scale devices are integrated. This paper studies a particular defect unique to CNTFET based integrated circuits: when a CNT used for implementing a CNTFET is metallic rather than being semiconducting. It pioneers a technique based on the physical design of layouts for CNTFET based cells. It is shown that single m-CNT defects can be modeled by SSFs and detected by the application of a SSF test set. Experimental results reveal its performance: a high level of m-CNT defect coverage can be achieved for all benchmark circuits examined.

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