Novel Design of Molecular Integrated Circuits and Molecular Nanoarchitectronics

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ABSTRACT

This paper presents an unified synthesis taxonomy to design three-dimensional (3D) molecular integrated circuits (^{M}ICs). The logic design of ^{M}ICs is accomplished by using a novel technology-relevant concept based on the use of neuronal hypercells ($^{\aleph}$hypercell) consisting of molecular gates (^{M}gates). These ^{M}gates are comprised from interconnected multi-terminal molecular electronic devices. Innovative methods in design of ^{M}ICs are documented. Our major motivation is to further develop and apply sound fundamental theory and technology. We expand the basic and applied research towards technology-relevant CAD-supported ^{M}ICs design theory and practice advancing a *molecular architectronics* (*^{M}architectronics*) paradigm.

Keywords: *molecular architectronics*, molecular electronics, molecular integrated circuits, CAD, SLSI

1. INTRODUCTION

Scaled to the nanometer dimensions microelectronic devices and CMOS technology are approaching fundamental and technological limits. Innovative enabling paradigms and technologies have been under developments. Among the most promising revolutionary directions is 3D molecular electronics. Super-high-performance ^{M}ICs can be designed as $^{\aleph}$hypercell aggregates that comprised from ^{M}gates [1]. These ^{M}gates formed by 3D-topology multi-terminal molecular electronic devices with a volumetric dimensionality of interconnected functional device ~1 nm. Up to 1×10^{18} interconnected molecular electronic devices, aggregated within $^{\aleph}$hypercell, can be placed in 1 mm^3.

Enabling molecular nanotechnologies and 3D topologies/organizations/architectures provide enormous advantages as compared with planar CMOS ICs. At the same time, extraordinary fundamental and technological challenges emerge at the device, module and system levels [1]. Significant challenges and unsolved problems exist in synthesis and design of ^{M}ICs, e.g., analysis, optimization, aggregation, evaluation, verification, fabrication, etc.

Nanoelectronics implies the use of: (1) Innovative electronic devices that exhibit novel phenomena which are uniquely utilized guarantying device and system functionality; (2) Enabling 3D topologies, organizations and architectures ensuring superior capabilities; (3) Emerging bottom-up fabrication technologies; (4) Super-large-scale integration (SLSI). To design ^{M}ICs, one must use novel paradigms and pioneering developments which are based on novel methods, enabling organizations/ architectures, sound bottom-up/top-down technology-relevant CAD, etc. We formulate and propose solutions to some fundamental and applied problems establishing a *^{M}architectronics* paradigm. The baseline problems in the design of ^{M}ICs are examined progressing from novel basic fundamentals to CAD-supported design. We foster advanced developments focusing on well-defined current status and future perspectives expanding the near-, medium- and long-term prospects and technologies.

2. SYNTHESIS TAXONOMY IN DESIGN OF ^{M}ICS

We define *^{M}architectronics* as a paradigm in synthesis of preeminent ^{M}ICs and information processing platforms which is based on:

- Discovery, understanding and utilization of novel phenomena, effects and solutions at the system and device levels in 3D topology/organization/architecture molecular electronics;
- Development and implementation of novel high-yield molecular fabrication technology concurrently supported by SLSI design and technology-relevant CAD.

In design of ^{M}ICs, one faces a number of challenging tasks such as analysis, optimization, aggregation, reconfiguration, self-organization, fabrication, evaluation, etc. Technology-relevant synthesis and design at the device and system levels must be addressed, researched and solved. A technology-relevant CAD-supported SLSI design of super-complex ^{M}ICs should be carried out. Molecular ICs utilize novel circuitry hardware within 3D organizations and architectures which guarantee massive parallel distributed computing and large-scale data manipulations. These features ensure super-high-performance computing and information processing. The combinational and memory ^{M}ICs should be designed as aggregated $^{\aleph}$hypercells comprised from ^{M}gates.

Various design tasks for 3D ^{M}ICs are not analogous to the CMOS-centered design, planar layout, placement, routing, interconnect and other tasks that have been successfully solved. Conventional VLSI/ULSI design is based on the developed CMOS fabrication technology, two-dimensional topology and microelectronic gates with FETs and BJTs. For ^{M}ICs, system- and device-level technology-relevant 3D synthesis must be performed using novel methods. Figure 1 illustrates the proposed 3D molecular electronics departing from two-dimensional multi-layer CMOS microelectronics [1, 2]. Some expected performance estimates are documented in Figure 1 where 3D-topology neuron is represented as a biomolecular processing module. Superior performance will be achieved by ^{M}ICs which should be designed. We propose to utilize a unified top-down (system level) and bottom-up (device/gate level) synthesis taxonomy within an *x*-domain flow map as shown in Figure 2 [1, 2]. The core 3D design themes are integrated within four domains: (1) Devising with validation; (2) Modeling–analysis–evaluation; (3) Design–optimization; (4) Molecular nanotechnology–fabrication.

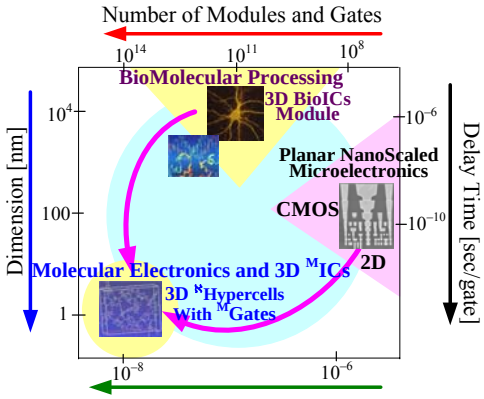

Figure 1. Molecular electronics and ^{M}ICs

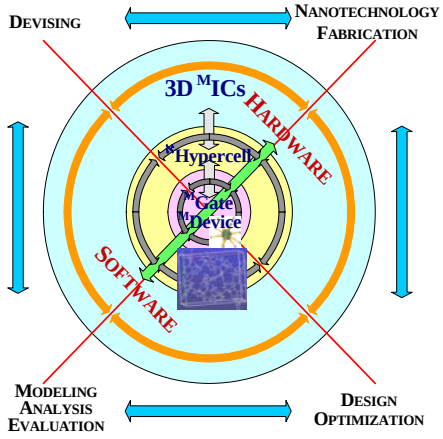

Figure 2. *X*-domain synthesis taxonomy

Novel synthesis, design, analysis and evaluation methods must be developed. The design in 3D space is radically different compared with VLSI/ULSI due to novel 3D topology/organization/architecture, enhanced functionality, enabling capabilities, enormous complexity, technology-dependence, etc. The unified top-down/bottom-up synthesis taxonomy should be coherently supported by developing innovative solutions to carry-out a number of major tasks, for example:

1. Devising and designing of ^{N}hypercells and ^{N}hypercells aggregates forming ^{M}ICs;
2. Development of new methods in design of 3D ^{M}ICs;
3. Analysis and evaluation of baseline performance;
4. Development of technology-relevant SLSI CAD to concurrently support design at the system and device/gate levels.

A novel unified top-down/bottom-up synthesis taxonomy integrates [1]:

1. Top-down Synthesis: Devise super-high-performance 3D ^{M}ICs within 3D organizations and architectures. These 3D ^{M}ICs are implemented as aggregated ^{N}hypercells composed from ^{M}gates that are engineered from multi-terminal molecular electronic devices, see Figure 3 [1, 2];
2. Bottom-up Synthesis: Engineer functional 3D-topology molecular electronic devices arranged in molecular aggregates that comprise ^{M}gates within ^{N}hypercells.

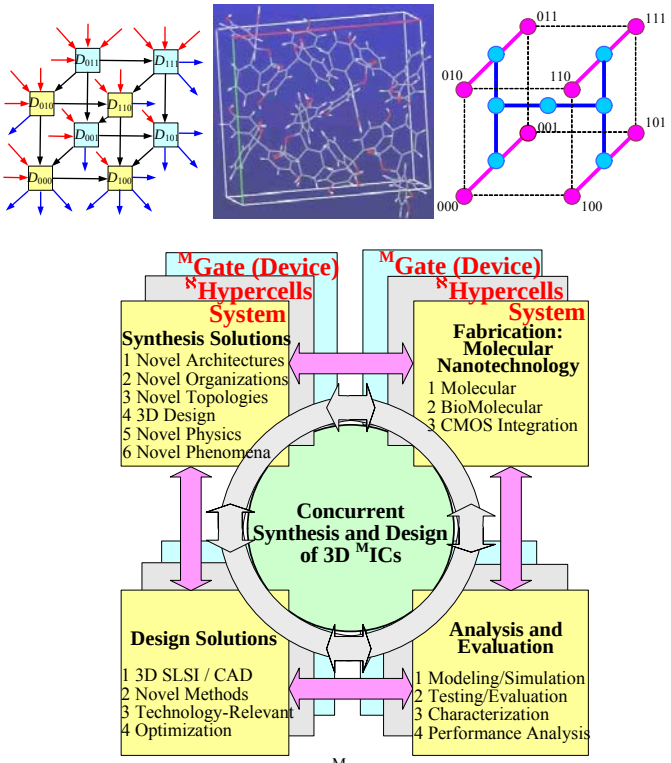

Figure 3. Three-dimensional ^{M}ICs and concurrent synthesis and design at system, module and gate (device) levels.

3. Design of Three-Dimensional ^{M}ICs

Innovative solutions to perform the system-level logic deign for 3D ^{M}ICs is carried out. We depart from 2D logic design (VLSI, ULSI and postULSI) as well as from planar ICs topologies and organizations [1]. We propose SLSI design coherently supported by novel methods which are developed and demonstrated. For 2D CMOS ICs, decision diagram, as a unique canonical structure, is derived as a reduced decision tree by using topological operators. In contrast, for 3D ICs, a new class of decision diagrams and synthesis methods must be developed to handle fundamental design differences the complexity. Design of linear decision diagram, mapped by 3D ^{N}hypercells, was developed and demonstrated in [3, 4]. In general, hypercell (cube, pyramid, hexagonal or other 3D topological aggregates) is a unique canonical structure which is a reduced decision tree. Hypercells are synthesized by using topological operators (deleting and splitting nodes).

We perform and examine optimal and suboptimal technology-specific topology mappings of complex switching functions. The major optimization criteria are: (1) minimization of decision diagram nodes and terminals; (2) simplification of topological structures utilizing linear arithmetic; (3) minimization of pathlength in decision diagrams; (4) simplification of routing and verification tasks. These advantages result in power dissipation reduction, evaluation simplicity, testability enhancement, as well as other important features. In particular, the proposed CAD-supported technology-relevant SLSI, which is concurrently supported by robust software and advanced design methods, performs the following major tasks:

1. Logic design utilizing novel efficient representations of data structures;
2. Synthesis of decision diagrams;
3. Synthesis and aggregation of $^{\aleph}$hypercells from the molecular primitives designing complex 3D ^{M}ICs.

SLSI utilizes a coherent top-down/bottom-up synthesis taxonomy as an important part of a *^{M}architectronics* paradigm. Current CAD-supported postULSI design does not allow one to design ICs with a number of gates more than 1,000,000. For the SLSI, the design complexity significantly increases and novel methods are sought. The binary decision diagrams (BDD), which represent Boolean functions, are the state-of-the-art techniques in high-level logic design [3]. The reduced-order and optimized BDDs ensure large-scale data manipulations and used to perform logic design and circuitry mapping utilizing hardware description languages. The design scheme is

Function (Circuit) ↔ BDD ↔ Optimization ↔
Mapping ↔ Realization.

The dimension of a decision diagram (number of nodes) is a function of the number of variables and the variables ordering. In general, the design complexity is $O(n^3)$. This enormous design complexity significantly limits the designer abilities to synthesize complex ICs for which the design should be performed without partitioning or decomposition. The word-level decision diagrams further increase the complexity. Therefore, novel sound software-supported design approaches are needed. We synthesize 3D ^{M}ICs utilizing the linear word-level decision diagrams (LWDDs) that allow one to perform the compact and effective representation of logic circuits using linear arithmetical polynomials (LP) [3, 4]. The design complexity becomes $O(n)$. The design algorithm

Function (Circuit) ↔ BDD ↔LWDD ↔ Realization

guarantees compact circuit representation and efficient design. The LWDD is embedded in 3D $^{\aleph}$hypercells that represent circuits in a 3D space. The polynomial representation of logical functions ensures the description of multi-output functions in a word-level format. The expression of a Boolean function f of n variables (x_1, x_2, … x_{n-1}, x_n) is $LP = a_0 + a_1x_1 + a_2x_2 + ... + a_{n-1}x_{n-1} + a_nx_n = a_0 + \sum_{j=1}^{n} a_j x_j$.

To perform a design, the mapping LWDD(a_0,a_1,a_2,…,a_{n-1},a_n) ↔ LP is used. The nodes of LP correspond to a Davio expansion. The LWDD is used to represent any m-level circuit with levels L_i, i=1,2,…,m–1,m with elements over the molecular primitive library. The data structures defined in the algebraic form by a set of LPs. In particular, we have

$$L = \begin{cases} L_1 : \text{inputs } x_j ; \text{outputs } y_{1k} \\ L_2 : \text{inputs } y_{1k} ; \text{outputs } y_{2l} \\ \text{.....} \\ L_{m-1} : \text{inputs } y_{m-2,t} ; \text{outputs } y_{m-1,w} \\ L_m : \text{inputs } y_{m-1,w} ; \text{outputs } y_{m,n} \end{cases}$$

that corresponds to

$$LP_1 = a_0^1 + \sum_{j=1}^{n_1} a_j^1 x_j, ..., LP_m = a_0^n + \sum_{j=1}^{n_m} a_j^n y_{m-1,j},$$

or in the graphic form by a set of LWDDs as

$$LWDD_1(a_0^1,...,a_{n_1}^1) \leftrightarrow LP_1, ..., LWDD_m(a_0^n,...,a_{n_m}^n) \leftrightarrow LP_m.$$

The use of LWDD is a significant departure from the existing logic design tools. This concept is compatible with the existing software, algorithms and circuit representation formats. Circuit transformation, format transformation, modular architecture, library functions over primitives, and other features can be performed. Arithmetic expressions underlying the design of LWDD are canonical representations of logic functions. They are alternatives of the sum-of-product, product-of-sum and Reed-Muller forms of representation of Boolean functions. Linear word-level decision diagrams are obtained by mapping LPs, where the nodes correspond to the Davio expansion and functionalizing vertices to the coefficients of the LPs. The design flow is LP Model ↔ LWDD Model ↔ Realization.

Any m-level logic circuits with fixed order of elements are uniquely represented by a system of m LWDDs as

Function (Circuit) ↔ LP ↔ LWDD ↔ Realization.

The proposed concept is verified by designing 3D ^{M}ICs representing Boolean functions by hypercells. CAD tools for logic design should be based on the principles of 3D realization of logic functions with a library of primitives. Linear word-level decision diagrams are extended by embedding the total solution tree into the $^{\aleph}$hypercell structures. For two graphs G=(V,E) and H=(W,F), we embed the graph G into the graph H. The information in the resulting $^{\aleph}$hypercells is subdivided according to the new structural properties of the cell and the type of the embedded tree. The embedding of a guest graph G into a host graph H is a one-to-one mapping M_{GV}:$V(G)\rightarrow V(H)$, along with the mapping M that maps an edge $(u;v)\in E(G)$ to a path between $M_{GV}(u)$ and $M_{GV}(v)$ in H. Thus, the embedding of G into H is a one-to-one mapping of the nodes in G to the nodes in H.

In SLSI design, decision diagrams and decision trees are used. Quantitative information measures and estimates can be evaluated [3]. Decision trees are designed using the Shannon and Davio expansions. There is a need to find the best variable and expansion for any node of the decision tree in terms of information estimates in order to optimize the design and synthesize optimal ^{M}ICs. For the c17 circuit, implemented using 3D molecular NAND gates (^{M}NAND) as reported in Figure 4, the Davio expansions ensure optimal design as compared with the Shannon expansion.

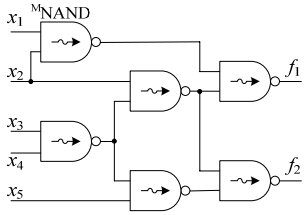

Figure 4. C17 implemented using ^{M}NAND gates

4. $^{\aleph}$HYPERCELL DESIGN

The binary tree is a networked description that carries the information regarding: (i) dual connections of each node; (ii) functionality of the logic circuit and topology.

The nodes of the binary tree are associated with the Shannon and Davio expansions with respect to each variable and coordinate in 3D. A node in the binary decision tree realizes the Shannon decomposition as given by $f = x_i f_0 \oplus x_i f_1$, where $f_0 = f|_{x_i=0}$ and $f_1 = f|_{x_i=1}$ for all variables in *f*. Each node realizes the Shannon expansion, and the nodes are distributed over levels. The classical hypercube contains 2^n nodes, while the ^{N}hypercell has $2^n + \sum_{i=0}^{n} 2^{n-1} C_i^m$ nodes to design technology-relevant ^{M}ICs.

The ^{N}hypercell consists of terminal nodes, intermediate nodes and roots. This ensures a practical ^{N}hypercell implementation, for example, by using the molecular multiplexers as shown in Figure 3. The three-step design procedure is: (*Step* 1) Connect the terminal node with the intermediate nodes; (*Step* 2) Connect the root with two intermediate nodes located symmetrically on the opposite faces; (*Step* 3) Pattern the terminal and intermediate nodes on the opposite faces and connect them via the root.

In general, ^{N}hypercell is a homogeneous aggregated assembly for a massive super-high-performance parallel computing and processing. We apply the enhanced switching theory integrated with a novel logic design concept [3]. The ^{N}hypercell is a topological representation of a switching function by *n*-dimensional graph. In particular, the switching function *f* is given as

$$\underset{f}{\text{Switching Function}} \Rightarrow \underset{\Uparrow}{\overset{2^n-1}{\underset{i=0}{\mathbf{L}}}} \overset{\text{Coefficient}}{\overset{\Downarrow}{\mathbf{K}_i}} \left(x_1^{i_1} \ldots x_n^{i_n}\right) \Rightarrow \underset{f_F}{\text{Form of Switching Function}}$$

The data structure is described in the matrix form using the truth vector ***F*** of a given switching function *f* as well as the vector of coefficients **K**. The logic operations are represented by **L**. Neuronal hypercells and their aggregates compute *f* of any complexity. The logic design in spatial dimensions is based on the advanced methods and enhanced data structures to satisfy the requirements of 3D topology. The appropriate data structure of logic functions and methods of embedding this structure into ^{N}hypercells have been developed in [3]. The design is given as

$$\underset{\text{Step 1}}{\text{Logic Function}} \Leftrightarrow \underset{\text{Step 2}}{\text{Graph}} \Leftrightarrow \underset{\text{Step 3}}{\text{Hypercell Structure}}.$$

5. SLSI Design of ^{M}ICs

The representative CAD tools and software solutions were developed, tested and validated to demonstrate the design of 3D ^{M}ICs ensuring the compatibility with the existing netlist formats. Designs have been performed for distinct ICs, and some results are reported in Table 1 [3]. The topological characteristics are evaluated using the total number of ^{M}gates, terminal (N_T) and intermediate (N_I) nodes, etc. For example, a 3D 9-bit ALU (c5315) with 178 inputs and 123 outputs is implemented using 1413 ^{M}gates. Molecular gates were networked and aggregated in 3D within ^{N}hypercells. The number of incompletely specified ^{N}hypercells was minimized. The design results also reported in Figures 5 displaying the Command Windows data of the representative SLSI Toolbox. In particular, the design of 3D c17 and 9-bit ALU (c5315) are documented.

Table 1. Experimental results for 3D ^{M}ICs

Circuit	I/O	Space Size #G	#X	#Y	#Z	Nodes and Connections $\#N_T$	$\#N_I$	CPU Time
8-bit ALU								
c880	60/26	130	70	72	70	612	482	0.04
c2670	233/140	828	82	80	78	3594	2766	0.15
9-bit ALU								
c5315	178/123	1413	138	132	126	3750	2813	0.34

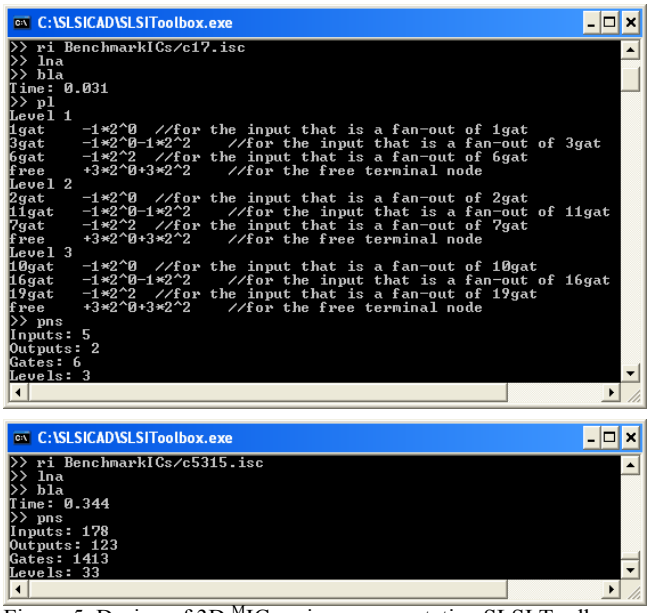

Figure 5. Design of 3D ^{M}ICs using representative SLSI Toolbox

6. Conclusions

The advancements and progress in design of 3D ^{M}ICs were ensured by using new solutions. The results reported further expand the horizon of molecular electronics theory and practice by synthesizing and designing ^{M}ICs.

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