TCAD-based Process-Aware HSPICE Model Parameter Extraction

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ABSTRACT

This paper formulates the problem of global SPICE model parameter extraction in terms of an objective function with process parameter variations. Algorithm to obtain the minimum value of the objective function is also proposed. In order to show the feasibility of the proposed algorithm, global extraction of process-aware SPICE model parameters is performed using electrical data obtained from silicon-calibrated TCAD simulations. An excellent goodness of fit is demonstrated over a known set of process parameters variations as well as the bias conditions. Validation of the extracted models is performed for a 90nm technology node by verifying the predictability of the SPICE model parameters against the TCAD simulations. Model parameters, thus obtained, are used to understand the response of a typical 2-input NAND gate to process variations using HSPICE.

Keywords: TCAD, process-dependant SPICE, extraction

1 INTRODUCTION

A key ingredient for bringing the manufacturing information into the design domain is process models or process related abstractions. Particularly, with the advent of smaller technology nodes like 90nm and beyond, impact of process variations on behavior of circuit design elements has increased significantly [1]. However, current SPICE models which act as the gateway between design and process worlds lack any accurate process related information. Corner case SPICE model extraction do not allow for the simulation of circuits as a function of process variations. Although, elaboration of SPICE model parameters as function of linearly independent vectors (Principal Component Analysis or PCA) aids in representing the entire space of device variations, the identity of process variations is completely lost in a PCA analysis [2]. A methodology to obtain process-dependant SPICE model parameters was proposed in [3] where, individual SPICE model cards were extracted for various process conditions. A compact SPICE model card was then constructed by fitting principal SPICE parameters to a polynomial function of process parameters. Although, the quality of fit might be reasonable, the predictability nature for such a non-physical SPICE model is questionable.

In the current paper, we propose an objective function for global extraction of process-aware SPICE model parameters, which ensures a high degree of predictability and validity over a range of process parameter variations. SPICE model parameters and their process dependencies are simultaneously extracted by minimizing the objective function value. In section 2, we formulate the problem of global optimization required to extract SPICE model parameters as a function of process parameter variations. We also provide the algorithm to solve the above mentioned problem. In section 3, we describe the extraction methodology to derive process-aware SPICE model parameters using TCAD generated device characteristics. In section 4, we show the quality of fit as well as the predictability of the SPICE models at various arbitrary process conditions. Additionally, we demonstrate the impact of process variation on a 2-input NAND gate digital circuit using the process-aware SPICE models.

2 PROBLEM DEFINITION

Let us denote a vector \( \vec{P} = \vec{P}^{(1)}_r = (P_1, P_2, ..., P_N)^T \) - a vector of normalized process parameters (or process conditions). \( N \) is the number of process parameters under consideration. Let \( \vec{P}_0 = \vec{P}^{(1)}_0 \) be a vector of normalized nominal process parameters. Let us define three vectors derived from process parameter vector as follows:

\[
\Delta \vec{P} = \Delta \vec{P}^{(1)} = \vec{P}^{(1)} - \vec{P}^{(1)}_0 \tag{1}
\]

\[
\Delta \vec{P}^{(2)} = (\Delta P_{1}^2, \Delta P_{2}^2, ..., \Delta P_{N}^2)^T \tag{2}
\]

\[
\Delta \vec{P}^{(3)} = (\Delta P_{1}^3, \Delta P_{2}^3, ..., \Delta P_{N}^3)^T \tag{3}
\]

These are vectors of linear, quadratic and cubical values of deviation of normalized process parameters. Let vector of nominal model parameters be defined as follows:

\[
\vec{M}^0 = (M_{ij}^0, |i = 1 \div M, j = 1 \div N) \tag{4}
\]

where \( M \) is the number of model parameters under consideration. Vector \( \vec{M}^0 \) directly corresponds to a vector \( \vec{P}_0 \). Let us denote matrices:

\[
(A^{(1)}_y, A^{(2)}_y, A^{(3)}_y, |i = 1 \div M, j = 1 \div N) \tag{5}
\]

These are matrices of process coefficients, linear, quadratic and cubical respectively. Now, each model parameter as a
function of process deviations can be defined as
\[ M_i = M^0_i + \sum_{j=1}^{N} (A^{(1)} \Delta \tilde{M}^{(1)} + A^{(2)} \Delta \tilde{M}^{(2)} + A^{(3)} \Delta \tilde{M}^{(3)}) | i = 1 : M \] (6)

Let RMS error between measured and simulated data for any device characteristic \( f \) be represented as:
\[ \text{RMS } (f, \tilde{M}) = \sum_{l} \sum_{k} \left( \frac{f_{\text{meas}}(\bar{V}_l) - f_{\text{sim}}(\bar{V}_l, \tilde{M})}{f_{\text{meas}}(\bar{V}_l)} \right)^2 \]
\[ = \sum_{l} \sum_{k} \left( \frac{f_{\text{meas}}(\bar{V}_l) - f_{\text{sim}}(\bar{V}_l, \tilde{M}^0, A^{(1)}, A^{(2)}, A^{(3)}, \Delta \tilde{M})}{f_{\text{meas}}(\bar{V}_l)} \right)^2 \] (7)

where, the first sum is over all samples with different process vector parameters \( \tilde{M} \). The second sum is over terminal voltages covering the whole region of device operation. The total objective function, which we use in our study can then be defined as:
\[ F_{\text{total}}(\tilde{M}) = F_{\text{total}}(\tilde{M}^0, A^{(1)}, A^{(2)}, A^{(3)}) = \text{RMS } (I_d, \tilde{M}) + \text{RMS } (G_m, \tilde{M}) + \text{RMS } (G_{ds}, \tilde{M}) + \text{RMS } (C_g, \tilde{M}) + \text{RMS } (C_d, \tilde{M}) + \Psi(\tilde{M}) \] (8)

where, \( I_d \) is the drain current, \( G_m \) is the transconductance, \( G_{ds} \) is the drain-to-source conductance, \( C_g \) is the gate capacitance, \( C_d \) is the drain capacitance and \( \Psi(\tilde{M}) \) is a penalty function [4]. Let the index set \( S_{NM} \) of integers be:
\[ k = (i-1) \times M + j | i = 1 : M, j = 1 : N \] (9)

where \( N \times M \) is a number of indices in the set \( S_{NM} \).

The objective function for global optimization can be rewritten as:
\[ F_{\text{total}}(\tilde{M}^0, a^{(1)}_k, a^{(2)}_k, a^{(3)}_k) | k \in S_{NM} \] (10)

Practically, this is a hard to solve problem probably without an exact solution. Let the index set \( S_m \) be defined as:
\[ k | a^{(1)}_k \neq 0, a^{(2)}_k \neq 0, a^{(3)}_k \neq 0 \] (11)

where, \( m \) is a number of indexes in the set \( S_m \). Finally we can define the optimization problem as:
\[ \min_{a^{(1)}_k, a^{(2)}_k, a^{(3)}_k} \{ F_{\text{total}}(a^{(1)}_k, a^{(2)}_k, a^{(3)}_k) \} | k \in S_m \] (12)

\( S_m \) should have a minimum number of indices \( k \).

Or in other words, \( m \) value should be as small as possible. Algorithm that will find the minimum value defined by eq.12 is described as follows:

1. Define \( m = 0, S_m = \emptyset \), an empty set, \( a^{(1,2,3)}_k = 0 \) \( \forall k \in S_{NM} \) (13)
2. For each \( k \in S_{NM-m} \) run a 3-dimentional optimization
\[ \min_{a^{(1)}_k, a^{(2)}_k, a^{(3)}_k} F_{\text{total}}(a^{(1)}_k, a^{(2)}_k, a^{(3)}_k) = F \min_k \] (14)
3. Find index \( q | F \min_q \leq F \min_k, \forall k \in S_{NM-m} \)
4. Add index \( q \) to the index set \( S_m \), exclude index \( q \) from the index set \( S_{NM-m} \), set \( m = m + 1 \)
5. Run optimization
\[ \min_{a^{(1)}_k, a^{(2)}_k, a^{(3)}_k} F_{\text{total}}(a^{(1)}_k, a^{(2)}_k, a^{(3)}_k) | \text{for all } k \in S_m \] (15)
6. Check convergence, if not, return to the Step2

3 EXPERIMENT

In order to show the feasibility of the proposed algorithm, we extract the SPICE model parameters as a polynomial function of process parameters. The electrical data required for the SPICE extraction is obtained from the TCAD simulations. Process and device simulations were performed in 2D approximation using state-of-the-art physics models in TSUPREM-4 and Taurus-Device tools, respectively. These simulations were calibrated against silicon based on secondary ion mass spectrometry measurements of the key doping profiles, sheet resistances of the source/drain doping profiles, overlap capacitance, and reverse short-channel effect. Indispensable to the current study is that the calibrated models provide likewise high accuracy for devices with small process and geometry deviations from the nominal values. This is necessary for sensitivity analysis and process optimization and centering.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Allowed Variation</th>
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<tbody>
<tr>
<td>Gate oxidation temperature</td>
<td>±10°C</td>
</tr>
<tr>
<td>Halo implant dose</td>
<td>±1e12 cm²</td>
</tr>
<tr>
<td>Spike temperature</td>
<td>±10°C</td>
</tr>
<tr>
<td>Vt-adjust implant dose</td>
<td>±1e12 cm²</td>
</tr>
<tr>
<td>( \Delta L )</td>
<td>±5nm</td>
</tr>
</tbody>
</table>

Table 1. Process parameters under study and the corresponding allowed variation.
In order to extract the SPICE models as a function of process parameters, process as well as device simulations for NMOS and PMOS devices were performed for each of the 128 process conditions. Process conditions with ranges shown in Table 1 are chosen using a Monte Carlo random number generator for a uniform distribution. The drain current was generated as a function of gate voltage, drain voltage and substrate voltage. The key process parameters chosen for this study are \( \Delta L \) (deviation of gate critical dimension from the nominal value), spike temperature (annealing temperature after all the implantations), halo implantation dose, gate oxidation temperature, and channel implantation dose (implantation used for adjusting threshold voltage, namely Vt-adjust implantation dose).

All the I-V curves generated from random sample points which correspond to more than 120,000 data points are provided to the extraction engine in order to perform global extraction and subsequently, derive process dependant compact SPICE model cards.

<table>
<thead>
<tr>
<th>Process Parameter</th>
<th>Coefficients</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Linear</td>
</tr>
<tr>
<td>Halo Dose</td>
<td>1.20E-02</td>
</tr>
<tr>
<td>Vt-adjust Dose</td>
<td>1.60E-03</td>
</tr>
<tr>
<td>Spike Temperature</td>
<td>2.10E-03</td>
</tr>
<tr>
<td>( \Delta L )</td>
<td>-4.90E-03</td>
</tr>
<tr>
<td>Gate Oxidation Temperature</td>
<td>2.11E-02</td>
</tr>
</tbody>
</table>

Table 2. Extracted spice parameter vth0 as a function of process parameter variations in a quadratic expression

4 RESULTS & DISCUSSION
of Ioff, a discrepancy of -35.7% between TCAD data and high in the case of Ioff. Owing to the logarithmic behavior discrepancy between TCAD and SPICE data is relatively (TCAD and SPICE simulations). The absolute value of discrepancy in Ioff obtained from similar set of I-V curves to possess dominant impact on gate delay variation as compared to that of ∆L, Vt-adjust implant dose and P-halo implant dose.

5 SUMMARY

In this paper, we have shown the formulation of the objective function which, upon minimization, enables global extraction of SPICE model parameters as a function of process parameter variations. We illustrated an excellent goodness of fit between TCAD and SPICE generated electrical characteristics. We have also demonstrated the high degree of predictability of device characteristics over a range of process variations. This study can easily be extended to incorporate real device electrical measurements. Compact SPICE models are used to study circuits like 2-input NAND gate as a function of process parameter variations. For these circuits, delay has been shown to vary in a non-linear but in a monotonic fashion with process parameters variations.

REFERENCES