SOI CMOS Compact Modeling based on TCAD Device Simulations

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ABSTRACT

The aggressive product development schedules demanded by today's marketplace require that early circuit design work overlaps substantially with process development activity. To support this, device models must be available prior to fabrication of the finalized CMOS device design. This work describes a Technology Computer Aided Design (TCAD) –based methodology for generating compact models in advance of hardware availability. The exercise was performed on a 65nm node SOI CMOS technology. TCAD was used in the conventional way to extrapolate interim CMOS devices to target performance by simulating planned process improvements. The resulting TCAD simulations were used to generate I-V and C-V data for compact model extraction. The extracted model is compared with TCAD simulations and the fit is shown to be good.

Keywords: soi, compact model, tcad

1 MODEL DEVELOPMENT FLOW

TCAD calibration has been primarily focused on aiding technology development in achieving next-generation technology targets and correctly predicting the response of these parameters to process changes. Increasingly accurate TCAD representations of SOI devices suggest the possibility of exploiting TCAD's predictive capability to create compact models for early circuit design before final device hardware is available.

The model development paths under discussion are shown conceptually in Figure. 1.

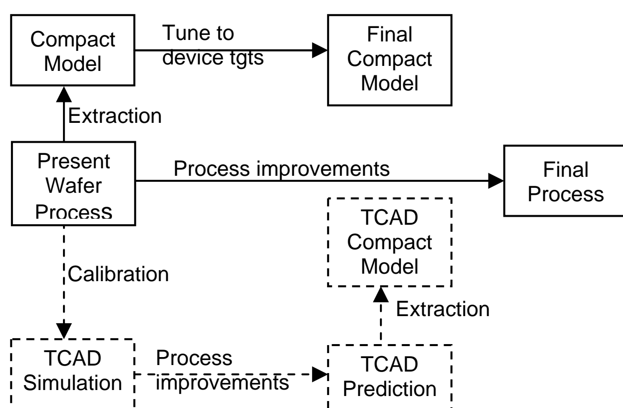

Figure 1: Proposed Role of TCAD.

The conventional path is shown by solid lines. To expedite product development, designers use a compact model that has been extracted from early hardware and tuned to meet ultimate device targets. Model adjustments are performed using compact model parameters describing mobility, saturated drift velocity, source/drain resistance, threshold, and subthreshold slope. The validity of this process is dependent on the proximity of the device used for fitting to the final device targets, that is, the degree of extrapolation, as well as on the experience and skill of the person making the model adjustments.

The proposed TCAD-based compact model development path is shown in the dashed lines. Here, the extrapolation is performed in the TCAD simulation rather than in the compact model. Once the TCAD simulation is satisfactory, the compact model is directly extracted from I-V and C-V data produced by the simulation. Model centering is not necessary since the TCAD produces nominal results.

The first issue with either of these extrapolation techniques is achievability of the ultimate parametric targets, and whether they are physically self-consistent. For example, changes to the process may improve on-current to the target value, but degrade leakage more than anticipated. In practice, experience gathered through prior split lot experiments helps to understand the coupled nature of the results of certain process changes. Also, TCAD may be employed to help assure that final targets are realizable and physically consistent. However, these techniques are imperfect and both the conventional and proposed model development paths are affected by these concerns.

The potential advantage in the TCAD-generated model path arises from the fact that targets are single-point measurements. Because of this, it is possible to adjust model parameters to meet single-point targets while not accurately replicating device behavior over the full range of terminal voltage conditions. Here TCAD should have an advantage since it can generate device behavior under any arbitrary set of conditions once calibrated to replicate target parameters. To be successful, this approach requires highly accurate TCAD calibration that captures both the structural characteristics imparted by semiconductor processes as well as electrical effects of those structures (such as mobility response to crystal stress, for example).

2 TCAD CALIBRATION

The TCAD simulation was calibrated to PFET and NFET devices in an early version of a 65nm node, partially-

depleted SOI CMOS process [1]. Planned process improvements to achieve ultimate parametric targets were implemented in the calibrated TCAD simulation to produce TCAD representations of the production NFET and PFET devices.

3 MODEL EXTRACTION

The compact model must be extracted from TCAD-generated I-V and C-V data using a procedure that emulates conventional model extraction because of the lack of one-to-one correspondence between TCAD physical parameters and compact model fitting parameters. TCAD simulations were used to generate a set of I-V and C-V data for both body-contacted and floating body devices as required by a typical compact model extraction sequence.

Highlights of the extraction sequence for the BSIM-PD 2.23 [2] model are shown in Figure 2.

1a. Junction diode
b. Gate current
c. Parasitic bipolar device
Low Vds {
2. Linear V_T,
3a. Subvt slope
b. Low-field mobility (long channel)
c. Series resistance (short channel)
}
4. Saturated V_T
5a. Long-channel Idsat
b. Short channel Idsat, gds, Impact ionization
6. IdVd (contacted and floating body)
7. Gate, overlap & junction capacitances

Figure 2: Model Parameter Extraction Sequence.

Most parameters are extracted from body-contacted devices. First, parameters for junction diodes, gate current, and bipolar effects are extracted. These parasitic currents must be correctly modeled to predict leakage and floating body voltage. The NFET source/drain-to-body diode model fit is shown in Figure. 3.

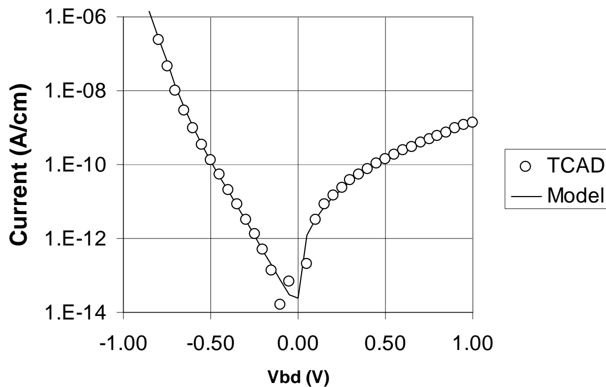

Figure 3: NFET Compact model vs. TCAD simulation for Drain-to-body Junction diode.

Following this, threshold voltage parameters are extracted. The linear Vt fit for the PFET appears in Fig 4.

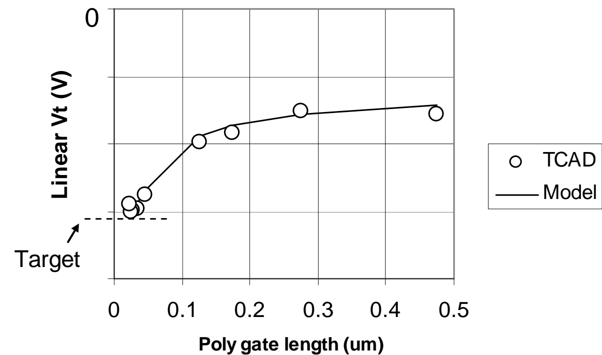

Figure 4: PFET Compact model vs TCAD simulation for linear threshold voltage (Vds = 50 mV) vs. Channel length.

Mobility, sub-threshold, and series resistance parameters are extracted from devices of various channel lengths operating at Vds=50mV as shown in Fig. 5.

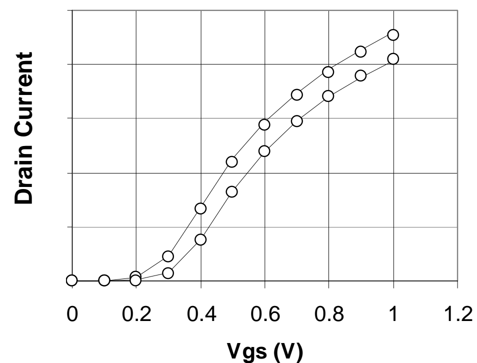

Figure 5: PFET Compact model vs. TCAD simulation for linear drain current (Vds = 50mV), Vbs = 0, 0.6V, Lpoly = 35nm.

Pinch-off and velocity saturation parameters are extracted from high-Vds data. Parameter extraction is performed for the body-contacted case, and checked against floating-body predictions.

One notable difference between hardware- and TCAD-based model extraction is that TCAD can readily isolate various current contributions or provide an ideal body-contacted device for model parameter extraction. The problem of isolating particular current components or interpreting measurement data is transferred from the model parameter extraction arena to the TCAD calibration activity.

4 RESULTS AND DISCUSSION

The resulting model fits are shown in Figs. 6 and 7 along with the ultimate device targets.

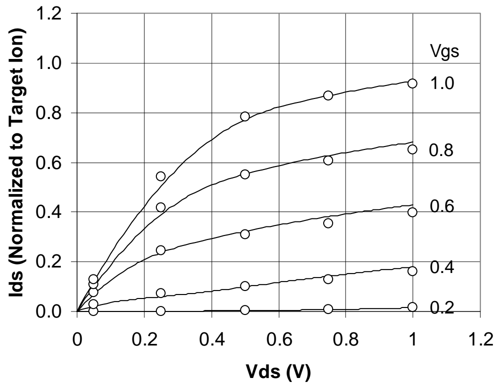

Figure 6: PFET Compact model vs TCAD simulation. Floating body device, Lpoly=40nm. Normalized to target Ion (Vds=Vgs=1.0V).

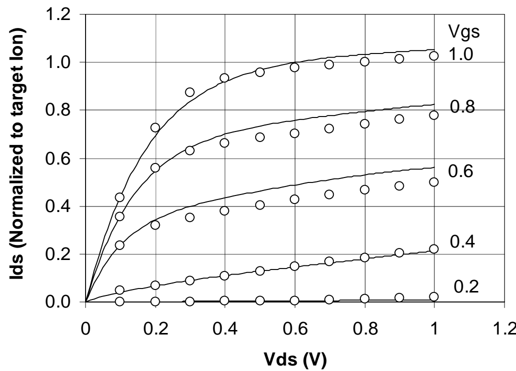

Figure 7: NFET Compact model vs TCAD simulation. Floating body device, Lpoly=35nm. Normalized to target Ion (Vds=Vgs=1.0V).

Both fits are quite good. The NFET model fit shows a small difference in transconductance over the plotted range of Vgs. In this work, the NFET TCAD simulation diverged from measured low-Vds device current data. Low-Vds simulations are used to determine mobility fitting parameters, which then interact with pinch-off and velocity saturation parameters to determine transconductance at high Vds. This demonstrates the importance of achieving high quality TCAD correlation over all operating regimes used to fit the compact model.

The approach of extracting compact models from TCAD simulation shows promise. However, it imposes a stringent standard for TCAD calibration. As described in the preceding paragraph, mobility and parasitic resistance model parameters are extracted from low-Vds I-V curves. If the low field I-V behavior is not simulated with high accuracy in TCAD, the extracted mobility parameters will be affected and lead to inaccuracies in extraction of high-Vds parameters such as saturated drift velocity and bulk charge coefficients for pinch-off. In addition to this concern, device extrapolation using TCAD is problematic without excellent calibration in all operating regimes.

One of the most significant conclusions of this work is the suggestion of an improved calibration procedure for TCAD device simulation. Compact model extraction employs a set of specific bias/geometry conditions to intentionally isolate various physical effects. Since calibration of TCAD has essentially the same goal (though for a different set of parameters) it is suggested that the scheme for calibrating TCAD simulation to hardware results follows a sequence analogous to the model extraction procedure, using essentially the same set of operating conditions.

This work describes the first steps toward generating compact models from TCAD device simulation. Fits were performed on wide devices at room temperature operation. Only the nominal case was considered. To create a compact model with full utility, narrow width effects, temperature, and process variation must be included in both the TCAD simulation and in the compact model extraction.

REFERENCES

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[2] BSIMPD2.2 MOSFET Model User's Manual, University of California, Berkeley, Department of Electrical Engineering and Computer Science.