Analog Compact Modeling for a 20-120V HV CMOS Technology

E. Seebacher, W. Posch, K. Molnar, A. Steinmair,
W. Pflanzl, B. Senapati and Z. Huszka

austriamicrosystems AG
A 8141 Schloss Premstaetten
Austria
ehrenfried.seebacher@austriamicrosystems.com
http://www.austriamicrosystems.com

ABSTRACT

In this paper we present a full characterization of HV CMOS transistors for a 20-120V CMOS technology including DC, AC and mismatch behavior. The model is based on a sub-circuit, which describes the geometry dependent AC and DC behavior of the device as well as the parasitic substrate currents and capacitance. The sub-circuit includes the correct description of the drain current and the parasitic substrate current with forward biased diodes as well. A proper mismatch model for HV CMOS transistors including an efficient parameter extraction strategy is presented.

Keywords: HV CMOS transistor, Sub-circuit modeling, mismatch modeling.

1 INTRODUCTION

HV CMOS transistors (LDMOS) (Figure 1) find an increasing use in the area of automotive applications, switching power supplies and amplifiers [1]. In contrary to the DMOS transistor which operates in vertical direction the LDMOS transistor is lateral orientated and thereby length and width dependent. All existing SPICE model developments for analytical models [2] and sub-circuit modeling concentrates on fixed size devices. In this paper we demonstrate a HV CMOS transistor sub-circuit which is applicable for different channel widths and lengths in case of DC, AC and parasitic modeling. The model includes the channel length dependent quasi-saturation effect, which has been discussed in [3, 4, 5, 6], the channel doping gradient effect and the correct modeling of extrinsic and intrinsic transistor capacitance. An important focus is related to the characterization and modeling of parasitic effects of the extrinsic HV MOS transistors where both, the measurement and modeling is described. For special automotive applications like H-bridges or transmission gates the parasitic bipolar transistors of the HV MOS transistor can be turned on. For a correct simulation of the substrate current of the HV - MOS transistor a full scalable parasitic bipolar transistor model has been developed. For yield prediction during the design phase and improvement of the circuit robustness a proper mismatch model for HV CMOS transistors including an efficient parameter extraction strategy has been introduced. A new algorithm is presented to extract device mismatch parameters for high-voltage transistors.

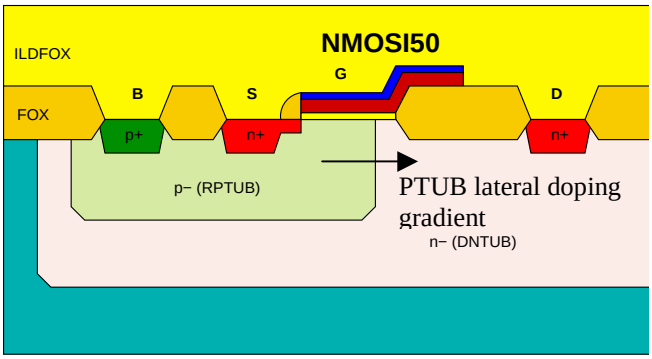

Figure 1: X-Section of a HV CMOS transistor in 0.35um 20-120V CMOS technology, HV NMOS body isolated

2 HV CMOS TRANSISTOR MODELING

The lack of existing analytical compact models for scalable HV CMOS transistors leads to the construction of sub-circuits, which are compatible to all major SPICE simulators. The main physical effects which should be included in a LDMOS transistor model additionally to the standard MOS transistor are the scalable quasi saturation effect [3, 4, 5, 6], the lateral channel doping gradient and the parasitic capacitance and currents. In Figure 2 a sup-circuit is shown which fulfils these requirements. The DC behavior of the LDMOS transistor for low currents is similar to the standard MOS transistor. Transistor M0 in the sub-circuit covers the main transistor effects and is supported with the widely used BSIM3v3 model. The lateral doping gradient in the channel leads to discrepancies in intrinsic capacitance and body factor modeling. To take into account these deviations from the standard transistor M1 is introduced. The main figure of merit for HV transistors is the on-resistance, which has to be modeled with high accuracy. The resistor RDJ is mainly responsible for the on-resistance modeling in the low current regime, which is not achievable with a standard BSIM3 model [7]. The quasi-saturation effect is covered by the JFETs J2 and

J1. The voltage controlled voltage source E is needed to guarantee the scalability of the macro model. The output characteristic is shown in figure 3 where measurement and model of a short channel transistor is demonstrated.

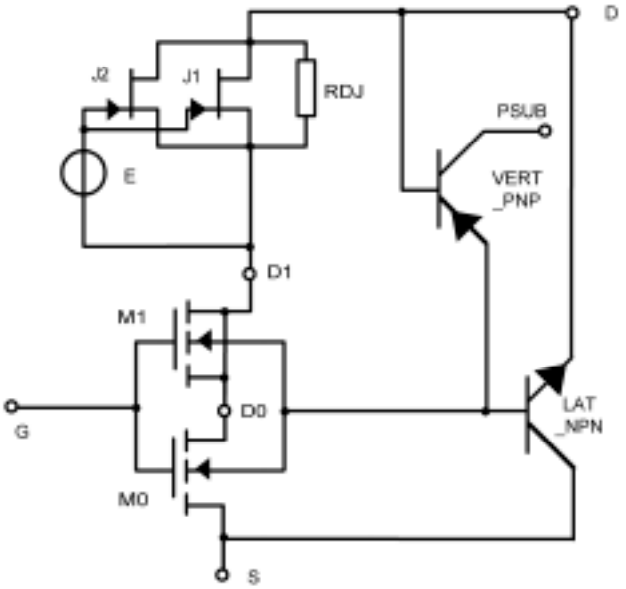

Figure 2: Sub-circuit for advanced HV CMOS transistor modeling for HV/analog applications.

3 MODELING OF THE INTRINSIC AND EXTRINSIC CAPACITANCE

Investigating the structure in Figure 1 there is a lateral-doping gradient in the p-type region under the gate oxide responsible for intrinsic capacitance behavior. The extension of the gate above the less doped body adds a MOS capacitance in parallel, which is modeled by another BSIM3v3 NMOS transistor with shorted source and drain terminals (M1 in Figure 2). Thereby the lateral doping gradient in the channel is taken into account. The length offset fitting parameter DLC of the BSIM3v3 model alone is not sufficient to adjust the intrinsic capacitance. The modification of parameters responsible for doping or threshold voltage would destroy the DC model behavior. The M1 parameters can be adjusted without affecting the DC model. M0 is used for modeling the gate to source and the gate to drain overlap capacitance too. Figure 4 shows the measured and simulated gate to bulk (Cgb) capacitance representing the intrinsic capacitance and the gate to source/drain capacitance (Cgc) demonstrating the extrinsic capacitance behavior. The results are shown for different bulk to source/drain voltages (Vbsd) with and without the second transistor. The modeling of the intrinsic capacitance is significantly improved with the additional transistor M1, especially the Vbs dependence of the threshold voltage can be modeled much better.

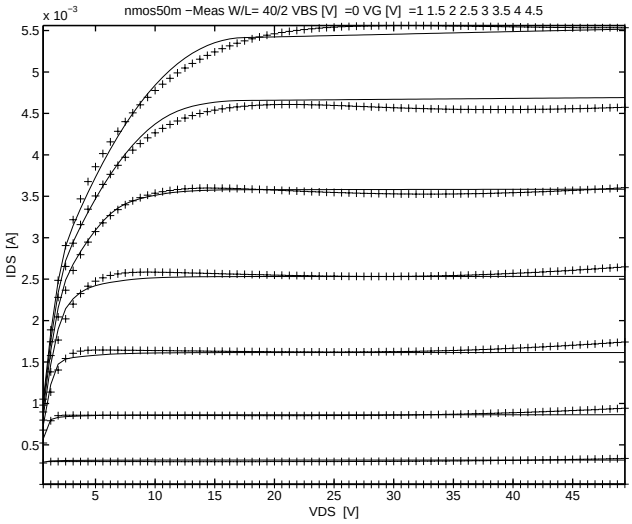

Figure 3: HV NMOS output characteristic W/L=40/2 VGS=1,1.5,2,2.5,3,3.5,4,4.5 V; += measurements, solid lines = sub-circuit (Figure 2).

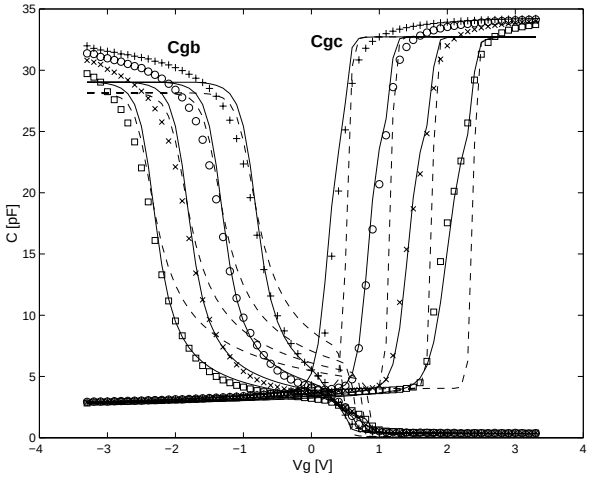

Figure 4*:* Measured and simulated Cgb and Cgc of NMOS50 W/L=4000/0.5. Vbsd=0 (+), -0.5V (o), -1V (x) and -1.5V ( ), dashed lines= with 1 BSIM3v3 transistor, solid lines =with 2 BSIM3v3.1 transistors.

4 MODELING OF HV CMOS PARASITICS

The designer must keep the magnitude of substrate injection under control. As a prerequisite the model of the MOS transistor must include the parasitic bipolar(s).

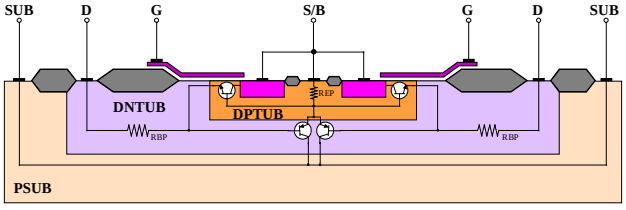

Figure 5: Parasitic bipolars in an isolated *n*-LDMOS

The emitter resistance REP of the vertical PNP keeps the CB junction of the lateral NPN closed while the emitter of the latter connects to the base of the PNP. Clearly, the substrate current is injected by the PNP, the lateral NPN contributes only to the drain current i.e. to the base current of the PNP. The lateral-NPN sub-circuit could be omitted by taking its effect on the base current into account by a special scaling technique.

This simplification was enabled by the observation that the parasitic transistor complex could be appropriately described by a single vertical PNP device as shown on Figure 6

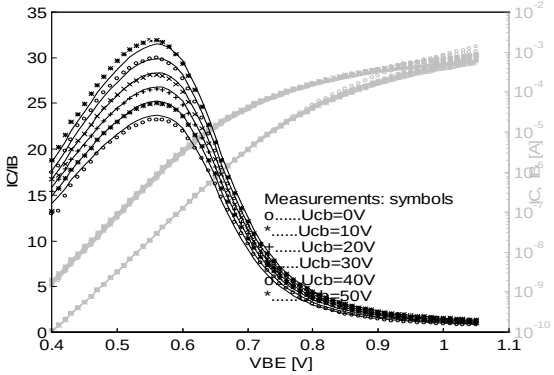

Figure 6: Parasitic bipolar: single *PNP* model

Denoting the scaled parameters by capitals, e.g. the saturation current parameter is expected to vary with the injecting area $A=W*L$ as $IS = IS\_ + ISL\_ \cdot \frac{1}{A}$. (1)

The saturation current IS depends linearly on the inverse area A as sown on Figure 7. The same form of scaling applies to other current parameters like e.g. the knee current IKF as well.

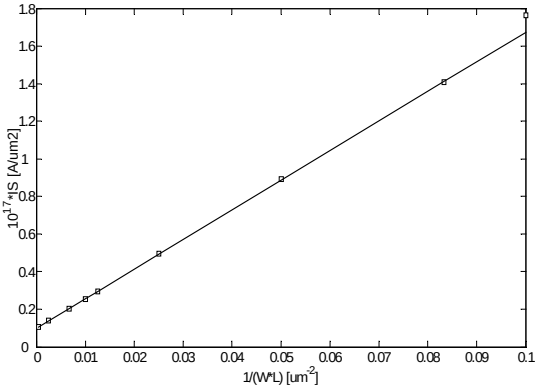

Figure 7: Scaling of *IS* in isolated *n*-LDMOS transistor

The scaling of the current gain parameter BF could be achieved with the ideal base current composed of the currents of the vertical and lateral transistors as

$$BF = \frac{IS\_ + IS\_A \cdot \frac{1}{A}}{ibei\_vl + \frac{1}{L^2} \cdot ibei\_lat0 + \frac{1}{A} \cdot ibei0 - L^2 \cdot ibei\_lat2} \quad (2)$$

Extracted BF values on Figure 8 are shown by open, scaled values by filled symbols.

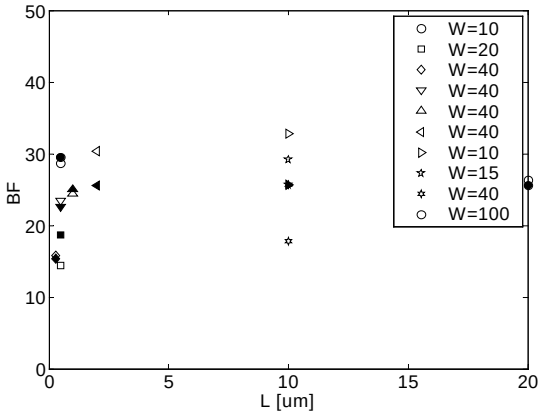

Figure 8: Open: extraction, filled: scaling expression

The currents of a bipolar device vary exponentially with temperature. It was especially important to characterize the parasitic PNPs in the range of -40 C^0 … 200C^0.

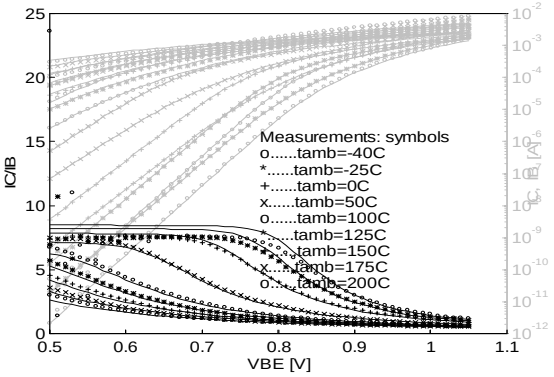

Figure 9: Temperature modeling of parasitic bipolars

5 MISMATCH CONSIDERATIONS FOR HV CMOS TRANSISTORS

The current mismatch of high voltage transistors is related to the mismatch of the device parameters VT (threshold voltage), κ (gain factor), θ (mobility reduction) and RD (drift resistance) by an appropriate variance model (Equation. 3). For high voltage transistors it is important to include the drift resistance RD as a device parameter [8].

Based on the measured transfer characteristic ID = f(VG) of the high voltage MOS transistors, the sensitivities, SV_T, Sκ, Sθ and SRD of the variance model (Equation. 3) are calculated after parameter extraction of V_T, κ, θ and RD. For the drain current appropriate MOS transistor models for the saturation region and the linear region are

assumed. The variances, $\sigma^2(\Delta V_T)$, $\sigma^2(\Delta\kappa)$, $\sigma^2(\Delta\theta)$, $\sigma^2(\Delta RD)$ of the threshold voltage difference, the gain factor difference, the mobility reduction difference and the drift resistance difference are determined by optimization fitting the measured variance curve $\sigma^2(\Delta ID/ID)$ vs. the variance model in equation 2. This procedure is carried out for different device sizes (different width W and length L of the transistor) and the mismatch of the device parameters can be related to the device area using Pelgrom's law.

$$\sigma^2\left(\frac{\Delta ID}{ID}\right)^2 = S_{V_T}{}^2\sigma^2(\Delta V_T) + S_\kappa{}^2\sigma^2(\Delta\kappa) + S_\theta{}^2\sigma^2(\Delta\theta) + S_{RD}{}^2\sigma^2(\Delta RD) + corr \quad (3)$$

Where the sensitivity of a parameter P is derived by

$$S_P{}^2 = \left(\frac{\partial\frac{\Delta ID}{ID}}{\partial\Delta P}\right)^2 .$$

Equation 2 represents a linear approximation of the mismatch variance. In reality, process parameters like VT and κ are correlated and an additional covariance term has to be added to equation. 3. Because the goodness of fit for the current mismatch of high voltage transistors did not improve significantly when adding those terms we decided to stay with the simpler linear model.

The matching parameter extraction [8] for high voltage transistors is carried out in three steps. In the first step the sensitivities for the threshold voltage, the gain factor and the mobility reduction are calculated from measurements in the saturation region and a suitable model for the drain current in the saturation region. In the second step, the sensitivities for the threshold voltage, the gain factor, the mobility reduction and additionally, for the drift resistance are calculated from measurements in the linear region using an appropriate drain current model for the linear region. In the last step, the mismatch parameters $\sigma^2(\Delta V_T)$, $\sigma^2(\Delta\kappa)$, $\sigma^2(\Delta\theta)$ are extracted first for saturation region and then $\sigma^2(\Delta RD)$ is determined for the linear regime taking into account the sensitivities of the variance model derived in the first two steps. The splitting of the parameter extraction is necessary because the optimizer is not able to distinguish between the contributions of $\sigma^2(\Delta\kappa)$ and $\sigma^2(\Delta RD)$ in the linear regime and of course a good fit would not provide reasonable parameters. Since the variation of the drift resistance $\sigma^2(\Delta RD)$ does not influence the mismatch in the saturation region, $\sigma^2(\Delta\kappa)$ can be determined accurately there.

To extract the parameter variances for a complex model like BSIM or EKV, the sensitivities of the variance model can be determined by numerical methods. In this case the compensation of parameters must be considered too. To verify the strategy, the mismatch parameters of an artificial "measurement" data set generated using the Monte-Carlo variation in SPICE simulators are extracted. If these parameters correspond to the variations of the SPICE parameters for data generation then a proper strategy has been used.

In Figure 9 the result of the new developed extraction method for HV MOS devices is shown. The measurements and the simulations of $\sigma(\Delta ID/ID)$ vs. gate voltage VG are compared.

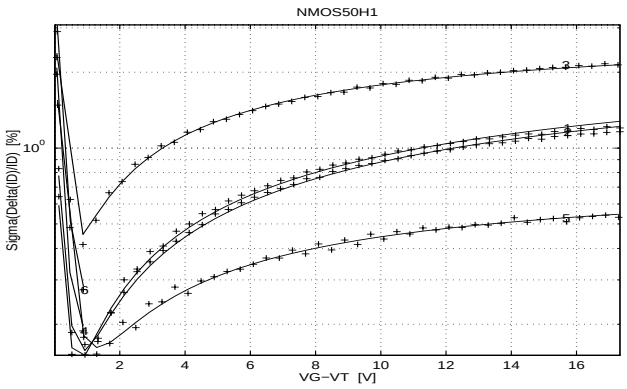

Figure 9: Linear operating regime: drain current mismatch $\sigma(\Delta ID/ID)$ vs. gate voltage VG for different geometries. For high VG, the mismatch is mainly specified by $\sigma(\Delta\kappa)$ and $\sigma(\Delta RD)$

6 CONCLUSION

A simulator independent macro-model for the a lateral HV MOS transistor has been presented which performs well for DC, AC regimes and parasitic substrate currents and capacitance. This sub-circuit has been made for different widths and lengths of the HV transistor. A proper mismatch model has been developed for the presented macro-model with special emphasis on RON matching modeling.

REFERENCES

[1] D.A. Grant and J. Gowa, Power MOSFETs- Theory and Applicatiosn, New York: Wily, 1989

[2] A. Arts, A Surface Potental Based High Voltage Compact LDMOS Transistor Model, IEEE Transactions on Electron Devices, Bol 52, No 5, May 2005.

[3] J. Jang, *et al.*, Proc. SISPAD, pp. 15-18 (1999)

[4] C. Anghel *et al.*, IEEE Semicon. Conf. pp. 417-420 (2001)

[5] C. Liu, *et al.*, IEEE TED, pp. 1117-1123 (1997)

[6] J. Victory, *et al.*, Proc. SISPAD, pp. 271-274 (1998)

[7] www.device.eecs.berkeley.edu/~bsim3/get.html

[8] W. Posch, H. Enichlmair, E.Schirgi and G. Rappitsch, Statistical Modelling of MOS Tranistor Mismatch for High-voltage CMOS Processes, Quality and Reliability Engineering International, 21, pp. 477 – 489, 2005