# BSIM Model for Mosfet Flicker Noise Statistics: Technology Scaling, Area, and Bias Dependence

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## ABSTRACT

We have implemented a statistical extension to the BSIM flicker noise model. The noise variation is attributed to the Poisson nature of the number of traps, and is found to be area and bias dependent. MOSFETs from the 130nm and 180nm technology nodes are compared in terms of their noise statistics. It is found that technology scaling has not had a negative impact on noise variations. Model development methodology is presented along with simulation-to-hardware correlation plots. Two new fitting parameters are introduced for statistical flicker noise modeling. Monte Carlo and Corner simulation capability of the new model is illustrated.

***Keywords:*** 1/f noise, flicker noise, compact-model, MOSFET, statistics.

## 1 INTRODUCTION

The number of traps found in a particular MOSFET device area follows a Poisson distribution [1]. As such, for modern submicron MOSFETs, trap density can not be treated as a fixed process constant. Carrier traps are the main source of MOSFET flicker noise. When modeling flicker noise, trap density must be treated as a random variable for which statistical properties (such as expected value and variance) must be verified experimentally. In fact, more than an order of magnitude of noise power variation can be observed in measurements on submicron FETs. This variation translates to 10dBc/Hz fluctuations in the close-in phase noise of an RF CMOS VCO. Given that many analog and RF circuits have such a sensitivity to flicker noise, it is essential to utilize a quantitative approach to design optimization that accounts for noise statistics. In this paper, we present a methodology for modeling flicker noise statistics, and compare results from 130nm and 180nm MOSFETs. The noise variation increases as transistor area is reduced, and as gate overdrive is decreased. This area and bias dependence is implemented in the new model. We utilize an extensive database where all the relevant data are stored and easily accessed.

## 2 NOMINAL BSIM NOISE MODEL

In the present BSIM implementation, correlated carrier number and mobility fluctuations are assumed to be the source of MOSFET flicker noise. Since the BSIM model is an extension to the number fluctuation theory, an apparent trap density ($N_t$) is defined to give the same level of noise in the absence of mobility fluctuations [2]. Three fitting parameters are used to attain $N_t$:

$$N_t = A + B \cdot N_{inv} + C \cdot N_{inv}^2 \qquad (1)$$

with $N_{inv}$ being the inversion carrier density. The noise level at a given bias condition is modeled to be proportional to $N_t$. To a first-order, it can said that parameter A contributes to noise at all bias conditions, and parameters B and C contribute to noise at higher gate voltages. To model MOSFET flicker noise, one has to determine the values for A, B, and C that gives the best fit to measured data. The bias dependence of the input-referred noise power (Svg) is captured by the relative values of the three fitting parameters. For example, for devices where there is a strong increase in Svg at high gate voltages, the ratio of C/A would be high in comparison to its value for devices where there is a weak increase in Svg at high gate voltages. Parameters B and C are introduced beacause the original number fluctuations theory does not predict any increase in Svg with respect to increased gate bias. The area dependence of the noise level is fixed to be 1/WL.

## 3 STATISTICAL FLICKER NOISE MODEL DEVELOPMENT AND BSIM IMPLEMENTATION

We gather noise data from a large enough sample of devices, such that the addition of new devices to the sample does not alter mean or variance by more than a few percent. In addition to the sample size, it is also important to measure multi-finger and single-finger FETs of different geometries to capture the area dependence of the noise statistics. Measurements are taken at multiple bias points to identify the dependence of noise statistics on Vds and Vgs. A single measurement is defined to be the data for a single device type, size, and bias; such as low-Vt nfet, with W/L of 10μm/0.12μm, Vgs=0.6V, and Vds=1.0V. We generate a database which, for each measurement, contains a matrix of Svg vs. frequency, transconductance, drain current, wafer id, and site id. From the Svg vs. frequency matrix, we extract $\phi$, such that $\phi_i / f^{ef}$ gives the best fit to the $i^{th}$ measurement; ef is treated as a constant and typically has a value close to 1, f is frequency. The final database contains all the relevant information for analyzing various trends in noise statistics. Such analysis yields useful information on the area dependence of noise variance, the bias dependence of noise variance, correlation between noise variation and transconductance variation, wafer-to-wafer and site-to-site variability, etc. Organization of the large volume of data in an easily accessible database allows for efficient data analysis and model development.

Before we can implement the statistical extension to the BSIM noise model, we must start with a nominal model that accurately captures the average noise level as a function of bias for each device type. The nominal model is based on measurements taken on process-centered wafers, with a large selection of bias points. The determination of the nominal values of the noise parameters is achieved by a combination of automated least-squares fitting and educated trial-and-error with the knowledge that the three parameters have different contributions based on gate voltage (through $N_{inv}$) as given in equation (1).

From the flicker noise database, we have observed that the distribution of $\phi$ is asymmetric for all measurements. The origin of the noise variation is the variability between the number of traps found in a particular device versus the expected value of the number of traps for that device area. For straight forward implementation in simulators, the Lognormal distribution can be used to skew the noise parameters with mean and variance extracted from the noise database.

A multiplier, k, is obtained from each measurement, such that:

$$\begin{aligned} \phi_{worst-case} &= k \cdot \phi_{\text{nominal}} \\ \phi_{best-case} &= \frac{1}{k} \cdot \phi_{\text{nominal}} \end{aligned} \tag{2}$$

Note that the value of *k* is dependent on device type, device size, and bias conditions. To make the model scalable with area and bias, we must scale the multiplier accordingly. Since the underlying mechanism of noise variation follows Poisson statistics, the worst-case multiplier scales with the square root of area. Therefore in our implementation, *k* is extracted from a moderate device geometry (W=10μm, L=0.12μm, # of fingers=10). Its scaling with respect to device area is verified through comparisons with the rest of the geometries in the noise database. It is also observed that the value of *k* is reduced for higher gate voltages. This reduction in variability is due to increased contribution of mobility fluctuations that do not have a direct correlation to the number of traps.

In addition to a worst-case model, it is of primary interest for circuit designers to be able to run Monte Carlo simulations, or pick corner-values that are statistically more relevant than the 3-σ point. Therefore the scaling of the noise parameters is tied to a Gaussian distribution which is used as multiplier on the worst-case noise level with proper area scaling:

$$M = \ln(k) - \min(\ln\sqrt{\frac{w \cdot l}{A_0}}, 0) \tag{3}$$

$$A = A_{\text{nominal}} * e^{D \cdot M} \tag{4}$$

$$B = B_{\text{nominal}} * e^{D \cdot \frac{M}{J}} \tag{5}$$

$$C = C_{\text{nominal}} * e^{D \cdot \frac{M}{J^2}} \tag{6}$$

*k* is multiplier extracted from a moderate sized device at low overdrive voltage; $A_0$ is the area of the device from which *k* is extracted; *w* and *l*, are

the width and length of the device being simulated. For $w*l > A_0$, M is pinned at ln($k$); for $w*l < A_0$, M increases according to the square-root of area dependence. The noise multipliers are scaled by a Gaussian random variable, *D,* and a fitting parameter, *J,* which captures the bias dependence of noise variation. The exponent of the Gaussian product gives the Lognormal distribution, with which the nominal values of the noise parameters are scaled (eqs. 4-6). The value of D is fixed in Corner simulations, and follows a Gaussian distribution in Monte Carlo simulations.

With this methodology, we have introduced two new parameters required for the statistical model (k and J), in addition to the three parameters required for the nominal model ($A_{nominal}$, $B_{nominal}$, $C_{nominal}$); k is a measure of noise variability, and J is a measure of the bias dependence of noise statistics.

## 4 RESULTS AND ANALYSIS

We have studied the noise statistics of regular-Vt FET pairs (nfet & pfet) from a 180nm node, and regular-Vt, low-power, low-Vt, thick-oxide, and high-voltage thick-oxide FET pairs, as well as zero-Vt, and thick-oxide zero-Vt nFETs, from a 130nm node. Fig. 1 shows measured noise from 180nm and 130nm regular-Vt nFETs. Note that the variation in noise level is fairly close between the two technology nodes. Technology scaling has not had a negative impact on noise variation, other than that introduced by area reduction. Model to hardware correlation is provided in Figs. 2 and 3, also illustrating the gate bias dependence of noise variation, and its capture by the new statistical model. A Monte Carlo vs. Corner simulation is shown in Fig. 4. This capability allows designers to optimize simulation statistics against other process variations, and pick corner values of interest. Fig 5. shows Corner runs for different areas. The noise is normalized to illustrate the variation with respect to area. Fig. 6 shows nominal and 3-σ simulations for a sweep of gate voltages.

## 5 CONCLUSION

We have presented the methodology and hardware correlation of a statistical flicker noise model with Monte Carlo and Corner simulation capability. BSIM noise parameters are assigned a Lognormal distribution with accurate representation of area and bias dependence. Noise variation is compared between 130nm and 180nm technologies. It is observed that 130nm and 180nm technologies have similar noise statistics, and technology scaling has not lead to increased noise variability. We have introduced two new fitting parameters to model the noise variation and its bias dependence. Strong agreement is shown between simulations and hardware measurements illustrating the quality of the statistical model.

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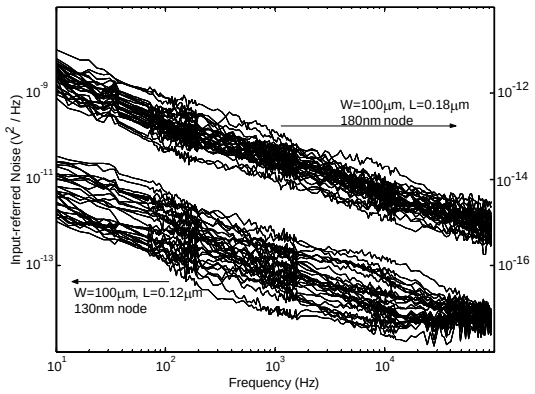


Fig. 1. 130nm and 180nm FETs show similar noise variation. Spread decreases with increased area.

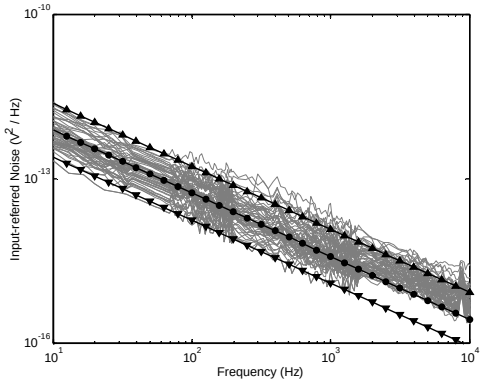


Fig. 2. Nominal, worst-case, and best case; model vs. hardware, pFET W=100μm, L=0.12μm, Vds=1.0V, Vgs=0.41V.

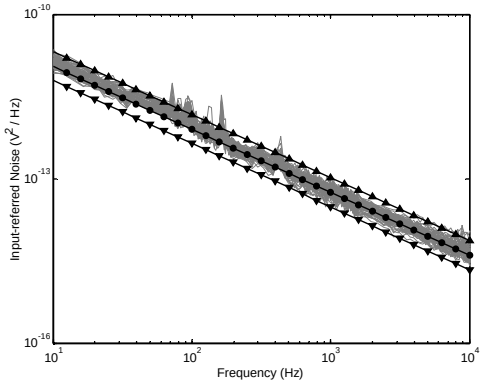


Fig. 3. Nominal, worst-case, and best case; model vs. hardware, pFET W=100μm, L=0.12μm, Vds=1.0V, Vgs=1.17V. Note the reduction in spread at higher gate bias.

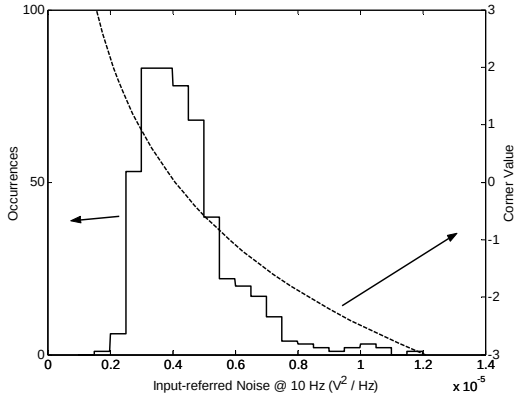


Fig. 4. Monte Carlo and Corner runs, nFET, W=10μm, L=0.12μm, Vds=1.0V, Vgs=0.9V.

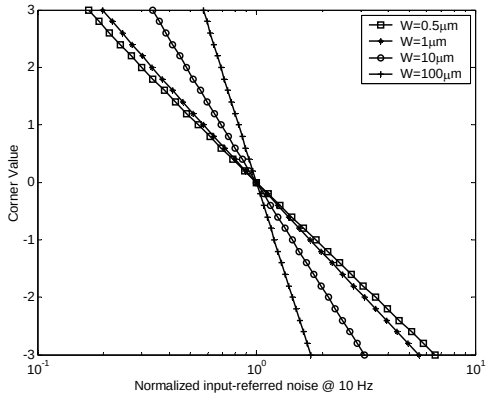


Fig. 5. Corner runs for various gate widths, nFET, L=0.12μm, Vds=1.0V, Vgs=0.7V. Noise is normalized to show relative variation.

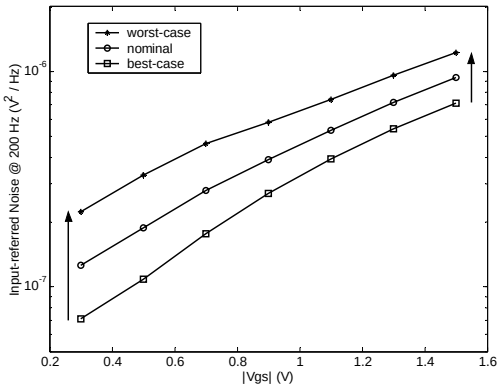


Fig. 6. Relative noise variation is reduced as overdrive is increased. Simulations for pFET, W=100μm, L=0.12μm, Vds=1.0V.