DC to RF Small-Signal Compact DG MOSFET model

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ABSTRACT

We present an analytical and continuous model for a doped double gate SOI MOSFET in which the channel current as well as the small-signal parameters are written as explicit functions of the applied voltages. The model is valid from below to well above threshold, showing a smooth transition between the regimes. The calculated current and capacitance characteristics show a good agreement with 2D numerical device simulations, in all regimes. Using the active transmission line approach the model has been extended to the RF regime. The high-frequency and noise performances of the DG MOSFETs have been analysed.

Keywords: Double-Gate MOSFET, RF modeling, noise.

1 INTRODUCTION

Double-gate transistors are considered to be a very attractive option to improve the performance of CMOS devices and overcome some of the difficulties encountered in further downscaling of MOS field-effect transistors into the sub-50 nanometer gate lengths regime [1,2]. One of the limiting factors in MOSFET downscaling is the static power consumption, due to short channel effects (SCEs) [3]. These effects increase the off-state leakage current. In the DG MOSFETs the control of the channel by the gate is stronger than in single gate MOSFETs, and this lead to a significant reduction of the short-channel effects.

Because of such advantages, these devices will be preferred in nanoscale circuits [4,5], thus making the demand for an accurate and CAD compatible DG SOI MOSFET model really urgent. Some models have been introduced before. Most of these models are for undoped DG MOSFETs, like in [6-10]. However real devices are doped and therefore models for doped devices are urgently needed in order to ease the use of these devices in circuits.

In this paper we present a model for the doped double gate MOSFET, which is analytical, explicit and continuous. It is based on a previous work done in [11], which presented a current model valid for low V_{DS}. Our model works in all operating regimes from weak to strong inversion and from the linear regime to saturation. The current expression is based on a unified charge control model, written in terms of charge densities at the source and drain ends [12] and derived for a doped DG MOSFET. We use an accurate explicit expression of the inversion charge densities in terms of the applied bias. The model is continuous through all operation regimes (linear, saturation, sub threshold). No fitting parameters are used in the charge control model. The model is valid up to well above threshold. Actually these devices are not operated at high values of V_{GS}, and therefore the model is valid for the regimes of practical interest. This model includes expressions of current, charge and capacitances, thus resulting also in a complete small-signal model. The explicit model of the channel current shows a good agreement with the 2D numerical device simulations. A good agreement is observed also for all the capacitances expressions compared to the 2D device numerical simulations. Therefore, our complete small signal model is suitable for use in circuit simulators.

We have extended our DG MOSFET model to RF is done through channel segmentation. The obtained local quasi-static compact models of transconductance, conductance and capacitances are used in each segment. Furthermore, we have developed a physical DG MOSFET noise modelling which includes diffusion and tunnel gate current contributions; this model has been included in our small-signal macro-model. We have considered the extrinsic elements, series source and drain resistances and overlap and fringing capacitances. The high-frequency performances of the DG MOSFETs are analysed through the use of analytical expressions of the cut-off frequency f_T and maximum frequency of oscillation f_{max}. The noise properties of the devices have been discussed. Our simulation results show the importance of gate tunnelling current and parasitic resistance as noise figure limiting factors when the gate length is downscaled.

2 DC MODEL

By using the Gradual Channel Approximation, and neglecting the hole concentration, Poisson's equation in an n-channel DG MOSFET reads as:

$$\frac{d^2\phi(x,y)}{dy^2}=\frac{q}{\varepsilon_{Si}}\left[N_A+\frac{n_i^2}{N_A}e^{\frac{q}{kT}[\phi(x,y)-V(x)]}\right] \qquad (1)$$

The y-axis is perpendicular to the surface and the x-axis starts in source and ends in the drain region. N_A represents the doping density. The potential $\phi(x,y)$ is referred to the neutral region of one equivalent bulk MOS transistor. V(x) is the electron quasi-Fermi potential depending on the voltage applied to the channel between source and drain and is assumed to be independent of x. [11]

The surface electric field can be written in terms of the mobile charge density (in absolute value)per unit area Q, and the depletion charge density per unit area (in absolute value) $Q_{Dep}=qN_At_{Si}$ (t_{Si} being the Si film thickness):

$$E_S(x)=\frac{Q+\frac{Q_{Dep}}{2}}{\varepsilon_{Si}} \qquad (2)$$

where ε_{Si} represents the silicon permittivity.

By integrating (1) between the centre and the surface of the film we get (11):

$$E_S(x)=\sqrt{\frac{2qN_A}{\varepsilon_{Si}}}\sqrt{(\phi_s-\phi_0)+\frac{kT}{q}\frac{n_i^2}{N_A{}^2}e^{\frac{q}{kT}[\phi_S-V(y)]}\left(1-e^{-\frac{q}{kT}(\phi_s-\phi_0)}\right)} \qquad (3)$$

where $\phi_S=\phi(x,-t_{Si}/2)$ is the surface potential and $\phi_o=\phi(x,0)$ is the potential in the middle of the film. Eq(3) cannot be analytically integrated for the potential, but it is observed, from numerical simulations, that the difference $\phi_S-\phi_0$ keeps a constant value from the subthreshold region to well above threshold. In subthreshold Poisson's equation can be reduced to its depletion form:

$$\frac{d^2\phi(x)}{dy^2}=\frac{qN_A}{\varepsilon_{Si}} \qquad (4)$$

Therefore, the following expression is obtained for the difference $\phi_S-\phi_0$.

$$\phi_S-\phi_0=\frac{qN_At_{Si}^2}{8\varepsilon_{Si}}=\frac{Q_{Dep}}{8C_{Si}} \qquad (5)$$

$C_{Si}=\varepsilon_{Si}/t_{Si}$ represents the silicon film capacitance. This approximation is valid from subthreshold to well above threshold, which is demonstrated by the correct agreement with simulations, for low and moderate V_{GS}(~2V) [11] For high V_{GS} the surface potential increases much more rapidly than the mid-film potential, making the approximation less correct.

Equating (2) and (3) we obtain the following charge control model:

$$V_{GS}-V_{FB}-V-\left(\frac{Q_{Dep}}{2C_{ox}}+\frac{kT}{q}\log\left[\frac{q^2}{kT}\frac{N_A{}^3}{n_i{}^2}\frac{t_{Si}{}^2}{2\varepsilon_{Si}}\right]\right)=\frac{Q}{C_{ox}}+\frac{kT}{q}\log\left[\frac{Q}{Q_{Dep}}\right]+\frac{kT}{q}\log\left[\frac{Q+Q_{Dep}}{Q_{Dep}}\right] \qquad (6)$$

Note that V varies from source to drain, being V=0 at the source and $V=V_{DS}$ at the drain. [12]. V_{FB} is the flat-band voltage, C_{ox} represents the capacitance of the oxide and Q is the mobile charge sheet density per unit area (in absolute value). n_i is the intrinsic carrier concentration.

The drain current is calculated from:

$$I_{DS}=\frac{2w\mu}{L}\int_0^{V_{DS}}Q(V)dV \qquad (7)$$

w represents the width of the device, μ the mobility of the electrons and L the channel length. The factor 2 appears because we have 2 gates.

From (6) we get:

$$dV=-\frac{dQ}{C_{ox}}-\frac{kT}{q}\left(\frac{dQ}{Q}+\frac{dQ}{Q+Q_{Dep}}\right) \qquad (8)$$

Therefore the expression of I_{DS} can be written in terms of carrier charge densities. Integrating (7) using (8), between Q_s and Q_d ($Q=Q_s$ at source end and $Q=Q_d$ at the drain end), we have:

$$I_{DS}=\frac{2w\mu}{L}\left[2\frac{kT}{q}(Q_s-Q_d)+\frac{Q_s^2-Q_d^2}{2C_{ox}}+\frac{kT}{q}Q_{Dep}\log\left[\frac{Q_d+Q_{Dep}}{Q_s+Q_{Dep}}\right]\right] \qquad (9)$$

In order to calculate the charge densities from an explicit expression of the applied bias, we use the following equation:

$$Q=C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_{Dep}}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_{Dep}}\right)^2+4\beta^2\log^2\left[1+e^{\frac{V_{GS}-V_{th}+\Delta V_{th}-V}{2\beta}}\right]}\right) \qquad (10)$$

This expression (10) is similar to the expression used in surrounding gate MOSFETs [12], where the charge control model has the same form as (6). This expression tends to the desired limits below and above threshold (see [12] for details).

In (10) $\beta=\frac{kT}{q}$ and V_{th} is defined as:

$$V_{th}=V_0+2\beta\log\left(1+\frac{Q'}{Q_{Dep}}\right) \qquad (11)$$

Q' is actually a first iteration for Q:

$$Q' = C_{ox}\left(-\frac{2C_{ox}\mathbf{b}^2}{Q_{Dep}} + \sqrt{\left(\frac{2C_{ox}\mathbf{b}^2}{Q_{Dep}}\right)^2 + 4\mathbf{b}^2 \log^2\left[1 + e^{\frac{V_{GS}-V_0-V}{2\mathbf{b}}}\right]}\right)$$
(12)

and

$$V_0 = V_{FB} + \left(\frac{Q_{Dep}}{2C_{ox}} + \frac{kT}{q}\log\left[\frac{q^2}{kT}\frac{N_A{}^3}{n_i^2}\frac{t_{Si}{}^2}{2\mathbf{e}_{Si}}\right]\right) \quad (13)$$

The term ? V_{th} ensures the correct behaviour of Q above threshold:

$$\Delta V_{th} = \frac{\left(\frac{2C_{ox}\mathbf{b}^2}{Q_{Dep}}\right)Q'}{Q_{Dep} + Q'} \quad (14)$$

Therefore Q_s and Q_d from the I_{DS} expression (9) can be computed by applying V=0 and V=V_{DS} in (10)-(12) .
The threshold voltage, V_t is extracted using the maximum transconductance change (TC) method [11,13], where V_t is defined as the gate voltage at which $\partial g_m / \partial V_{GS}$ is maximum or $\frac{d^3 I_{DS}}{dV^3{}_{GS}} = 0 = \frac{d^3 E_S}{dV^3{}_{GS}}$

From this extracted value of V_t, using (17-19) we obtain the corresponding value of V_{FB}, which is actually one of the parameters used in our model to calculate the expressions of the mobilie charge sheet densities through the V_0 parameter defined in (13). We have observed that the extracted value of V_{FB} corresponds to the calculated value (the difference between the work functions of the gate material and the semiconductor) in the case of the device simulated with ATLAS (where no interface states have been introduced) .

In order to compare our model with ATLAS numerical simulations, we have considered a DG MOSFET with the following parameters: the doping level was N_A=6.10^{17} cm^{-3}; the silicon thickness t_{Si}=31nm; the oxide thickness t_{ox}=2nm; the channel length L=1µm; the width of the device w=1µm. We have compared the modeled and simulated I_{DS}-V_{GS} characteristics for two values of V_{DS} (0.05V and 1V). These characteristics are plotted in the linear and logarithmic scale (Fig. 1-2). Agreement is good, provided V_{GS} is not very high. In the subthreshold regime there is a perfect match between our model and the simulations (Fig.2). The I_{DS} - V_{DS} characteristics, for different values of V_{GS}, show a good agreement with the numerical simulations. (Fig.3).

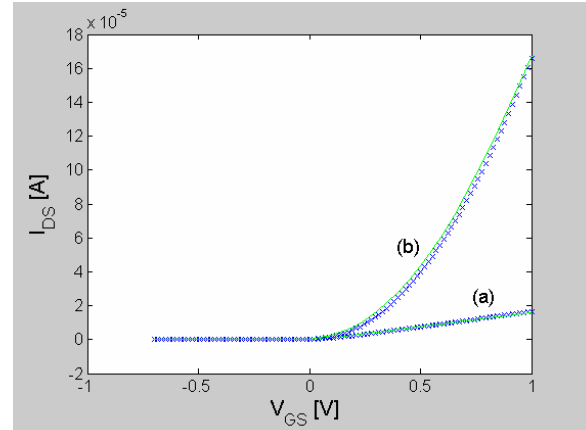


Fig.1. Transfer characteristics for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in linear scale. Solid line: ATLAS simulation; Symbol line: our model using (9)

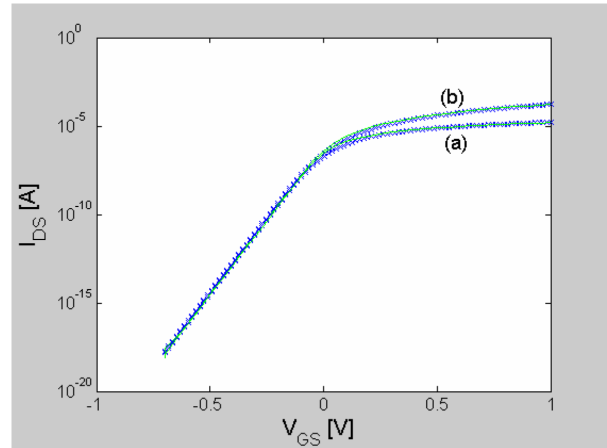


Fig.2. Transfer characteristics for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in logarithmic scale. Solid line: Atlas simulation; Symbol line: our model using (9)

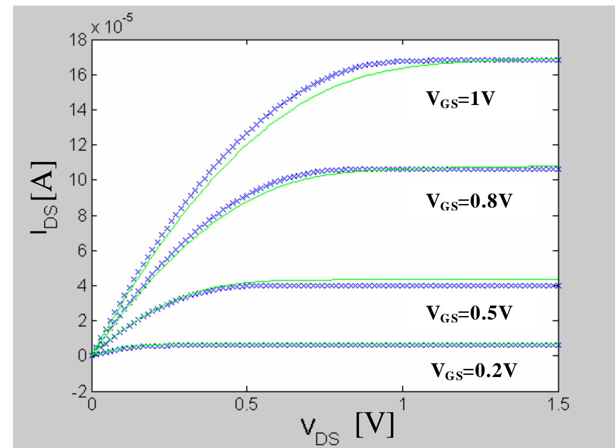


Fig. 3 Output characteristics of a DG MOSFET. Solid line: Atlas simulation; Symbol line: our model using (9)

3 CHARGE MODEL

The total inversion charge is calculated as [14]:

$$Q_{Tot} = -2w\int_0^L Q dx = -(2w)^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV \qquad (15)$$

Using (8) we can obtain an analytical expression by integrating:

$$Q_{Tot} = (2w)^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q + Q_{Dep}} \right) dQ \qquad (16)$$

The total gate charge is Q_G=-Q_{Tot}+Q_{ox}+Q_{Dep}, where Q_{ox} is the total fixed charge in the oxide and at the oxide/semiconductor interface.

The capacitances, C_{gd} and C_{gs}, are obtained as [14]:

$$C_{gi} = -\frac{dQ_G}{dVi} \qquad (17)$$

where i=d,s

We obtain these capacitances, by differentiating Q_{Tot} according to (8) and using (10) for the charge densities at source and drain.

Following the Ward's channel charge partitioning scheme [14] we obtain analytical expressions for the total drain (Q_D) and source (Q_S) charges:

$$Q_D = -2w\int_0^L \frac{x}{L} Q dx = \frac{(2w)^3 \mu^2}{L I^2_{DS}} \cdot \int_{Q_s}^{Q_d} Q^2 \left(\left(\frac{Q^2 - Q_s^2}{2C_{ox}} \right) + \frac{kT}{q} \left(2(Q - Q_s) - Q_{Dep} \log \left[\frac{Q + Q_{Dep}}{Q_s + Q_{Dep}} \right] \right) \right) \cdot \left(\frac{1}{C_{ox}} + \frac{kT}{q} \left(\frac{1}{Q} + \frac{1}{Q + Q_{Dep}} \right) \right) dQ \qquad (18)$$

$$Q_S = Q_{Tot} - Q_D \qquad (19)$$

The capacitances C_{dg} and C_{sg} are obtained as [14]:

$$C_{ig} = -\frac{dQ_i}{dV_G} \qquad (20)$$

All the resulting expressions of charges and capacitances are analytical and explicit.

In order to have a complete model for the drain and source capacitances, we have to account for the parasitic capacitances: overlap and fringing capacitances. In our model we added these parasitic capacitances to the intrinsic capacitances. We have adapted a model that considers the bias dependence of the overlap and fringing capacitances to DG MOSFETs. The fringing capacitance between gate and source is defined as:

$$C_f = C_{f,\max} \exp\left[-\left(\frac{V_{GS} - V_{FB} - \frac{\phi_F}{2}}{\frac{3\phi_F}{2}} \right)^2 \right] \qquad (21)$$

where $C_{f,max}$ is an adjustable parameter. By increasing V_{GS} the fringing capacitance tends to zero because of the inversion channel formed.

The gate-source overlap capacitance has the following expression:

$$C_{ov} = wC_{ox} \frac{L_d}{1 - \lambda V_{GS}^*} \qquad (22)$$

where L_d is the gate overlap region. A smoothing function, in order to make the overlap capacitance to tend to the desired values above and below threshold, is used:

$$V_{GS}^* = V_{GS} - \frac{1}{2} V_{GS} + \sqrt{V_{GS}^{\ 2} + 0.05} \qquad (23)$$

In (22) ? is an adjustable parameter depending on the channel doping, acting on the technological parameter L_d. [15]. From (22)-(23), well above threshold, C_{ov}~wC_{ox} L_d, as it should. As V_{gs} decreases C_{ov} decreases and from (22)-(23) it tends to 0 below threshold , as it should.

Therefore, the complete model for the parasitic gate-source capacitance which will be added to our intrinsic capacitance model, is given by:

$$C_{GS,par} = 2w\left(C_{ox} \frac{L_d}{1 - \lambda V_{GS}^*} + C_f \right) \qquad (24)$$

Following the same reasoning, the parasitic gate-drain capacitance, $C_{GD,par}$ can be calculated by replacing V_{GS} with V_{GD} from (21) to (24). These expressions of $C_{GS,par}$ and $C_{GD,par}$ should be added to the expressions of the intrinsic capacitances C_{SG}, C_{GS} and C_{DG}, C_{GD}.

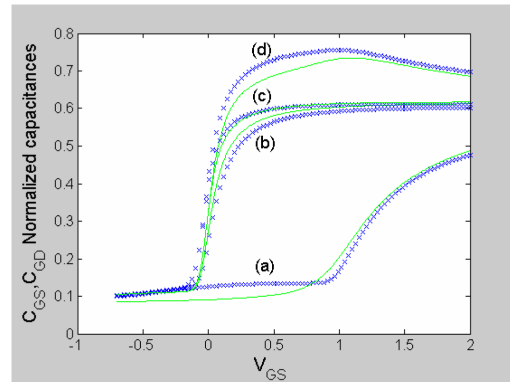


Fig. 4. Normalized C_{GD} for V_{DS}=0.05V (b) and for V_{DS}=1V (a) and C_{GD} for V_{DS}=0.05V (c) and for V_{DS}=1V (d). Solid line: ATLAS simulations; Symbol line: model. DG MOSFET with doping: N_A=6.10^{17} cm^{-3}; silicon thickness t_{Si}=31nm; oxide thickness t_{ox}=2nm

Using ATLAS we simulated the device capacitances of the

same DG MOSFET studied in the previous section for two values of V_{DS}: 0.05V and 1V. We have compared these simulations with our model. The capacitances have been normalized to the oxide capacitance. (Fig.4). Good agreement is observed in all operating regimes.

4 RF AND NOISE ANALYSIS

To extend our DG MOSFET model to RF, and be able to account for effects such as the non-quasi static effects (including the correlation between the gate and the drain noise sources and the tunneling gate current noise) we use the active transmission line method.

The active transmission line method is based on splitting the channel into several sections or slides [16,17]. The small-signal and noise sources for each channel section can be derived from semiconductor equations. The local equivalent circuit (Fig. 5) is composed by the gate to channel capacitance, the transconductance, and the channel resistance (or conductance), which are determined by our model. Diffusion noise and gate shot noise (due to the direct tunneling through the gate [18]) are incorporated into the model.

We have analysed the high frequency performances of the DG MOSFET through the use of analytical expressions of the transition frequency f_T and maximum frequency of oscillation f_{max}, and also, the noise properties of the devices.

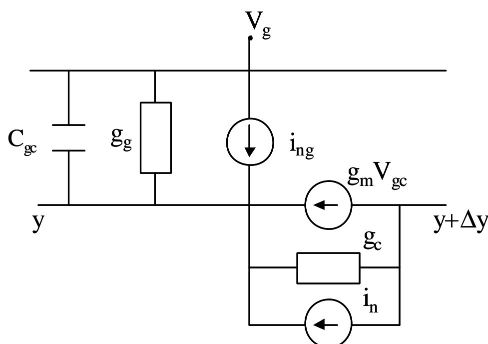


Fig. 5: Small equivalent circuit of a channel slide.

Figure 6 shows the frequency behavior of a DG MOSFET (N_a=6·10^{17} cm^{-3}, t_{ox}=1.5 nm, t_{si}=40 nm, L=100 nm, total width W=50 µm, 4 fingers, V_{GS}-V_{TH}=1.5V, V_{DS}=1.5V) for two gate bias voltages (V_{GS}-V_{TH}=0.5V and V_{GS}-V_{TH}=2.5V). This figure shows an important increase of minimum noise figure at the low frequency range (about f<5 GHz) due to the gate shot noise for high gate voltages where tunneling gate current is significative. The gate shot noise current generated in each segment of the device flows along the channel and subsequently creates drain shot noise current as well, because it is uncorrelated with the origins of the drain and gate current noise. Since the direct tunneling current can be substantial, the drain shot noise becomes comparable to the drain current noise in devices with oxides below 2 nm.

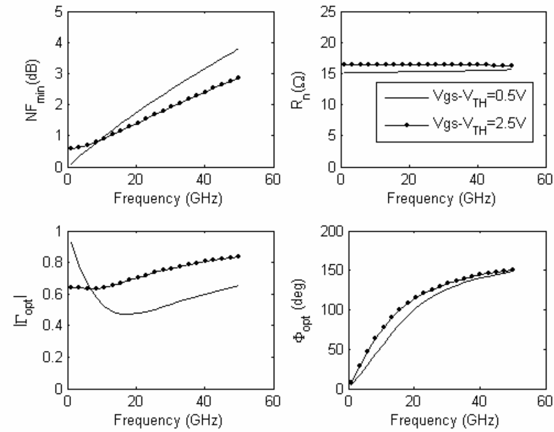


Fig.6: Noise parameters as function of frequency for a DG (N_a=6·10^{17} cm^{-3}, t_{ox}=1.5 nm, t_{si}=40 nm, L=100 nm, total width W=50 µm, 4 fingers, V_{DS}=1.5V).

As the gate length is reduced, all other parameters have been scaled in accordance with the ITRS roadmap (ITRS 2003). In particular we have considered the relevant scaling of the effective oxide thickness. For a gate length smaller than 65 nm the oxide thickness is smaller 1.5nm. In the following simulations, we consider that values of silicon body thickness (to minimize SCE) are $t_{si}=0.4L$ for DG MOSFETs.

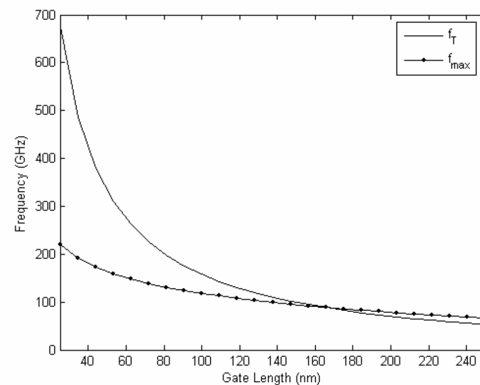


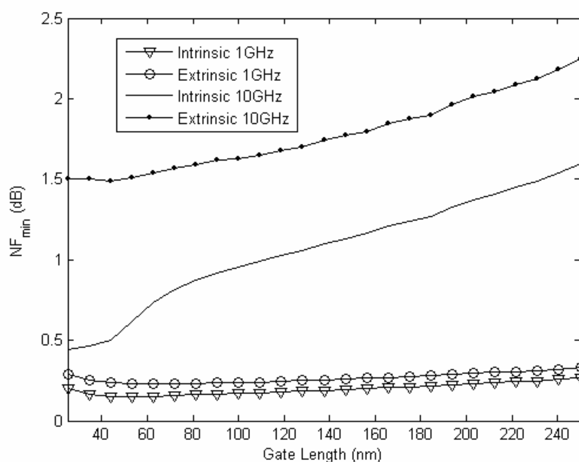
Fig.7: Transition frequency f_T and f_{max} frequency as function of gate length for Double-Gate (DG) (N_a=6·10^{17} cm^{-3}, t_{ox}=1.5 nm, $t_{si}=0.4\cdot L$, total width W=50 µm, 10 fingers, V_{GS}-V_{TH}=1.5V,V_{DS}=1.5V).

Figure 7 shows the transition frequency f_T and maximum frequency of oscillation f_{max} with the gate length (N_a=6·10^{17} cm^{-3}, t_{ox}=1.5 nm, $t_{si}=0.4\cdot L$, total width W=50 µm, 10 fingers, V_{DS}=1.5V). f_T depends on the ratio between the

transconductance, g_m, and total gate capacitance, while f_{max} also depends on the source/drain and gate parasitic resistances, the equivalent nonquasi-static resistance R_i, the drain-to source conductance g_{ds}, and the Miller capacitance to gate ratio, C_{gd}/C_{gs}. Overlap and fringing capacitances increase intrinsic capacitances reducing the transition frequency f_T and the maximum frequency of oscillation f_{max}. Other important limiting factors in f_{max} are the parasitic resistances, especially the gate resistance, R_g, which increases with downscaling and must be reduced using silicate gates with parallel gate fingers and gate contacts [19].

Figure 8 shows the extrinsic and intrinsic minimum noise figure as a function of gate length for the same conditions as in Fig.3 at 1 GHz and 10 GHz. At 10 GHz, the diffusion noise predominates over shot gate noise, and the intrinsic noise figure reduces with downscaling. But at 1 GHz, the shot noise contribution is predominant and the noise figure increases with gate length downscaling. Also, the effect of parasitic resistances is more important at 10 GHz, and its noise contribution increases with the downscaling.

Fig.8: Intrinsic and Extrinsic Minimum Noise Figure NF_{min} (dB) as function of gate length at1 GHz and 10 GHz (N_a=$6\cdot10^{17}$ cm^{-3},



t_{ox}=1.5 nm, $t_{si}=0.4\cdot L$, total width W=50 μm, 10 fingers, V_{GS}-V_{TH}=1.5V, V_{DS}=1.5V).

5 CONCLUSION

We have developed an analytical and compact dc charge model for doped DG MOSFETs from a unified charge control model derived from Poisson's equation. The effect of volume inversion is inherent to the model. The drain current expression shows a good agreement compared to 2D numerical simulations from subthreshold to well above threshold. The charge model, consistent with the dc model, is also analytical. The small signal model is obtained from the current and the charge model. The modeled capacitances show good agreement with the 2D numerical simulations, in all operating regimes. Using channel segmentation, the model has been used to study and discuss the RF and noise performances of these devices.

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