Static Analog Design Methodology

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ABSTRACT

This paper presents a static design methodology dedicated to ultra low power ($Vdd < 1V$, $i_{branch} < 100nA$) analog circuits. This methodology based on the EKV 2.0 MOS model, tuned with non uniform substrate doping correction and rigorous derivation of the EKV 3.0 MOS model, provides continuous over inversion levels equations in conduction as in saturation modes. Fundamental parasitic effects such as mobility reduction due to vertical field are therefore integrated with highlights of newer EKV versions.
Furthermore, this methodology provides a tool, the technological char for easily integrating this improvement during conception phase. It results in a good accuracy over all regions of MOS operation, including moderate inversion where neither weak-inversion nor traditional strong inversion MOS hand analysis are applicable.

Keywords: Analog design methodology, EKV MOS model, Ultra low power, Moderate Inversion, MOS sizing

1 INTRODUCTION

When strong constraints of supply voltage ($< 1V$) and bias current ($< 100nA$) are required, the only way to meet design's specifications without using huge silicon area consists on decreasing transistor inversion level and therefore going in moderate inversion. Gm/Id methodology [1], [2] is a good solution for dynamic target, but unusable for static circuits. In this case, analog designers need a design methodology which provides continuous over inversion level hand calculation usable equations.

EKV 2.0 MOS model proposes drain current formula which in addition to being continuous from weak to strong inversion is invertible. This equation usable for hand calculation, is thus a good starting point for making ultra low power analog designs without inversion level constraint.

Nevertheless, if the 2.0 version of the EKV MOS model is the only one which proposes invertible expressions, it is also the oldest. As a consequence, accuracy must be taken into account by considering newer versions highlights, and particulary mobility reduction due to vertical field.

The main objective of the Static Design Methodology (SDM) presented here, is to provide analog designers a tool as simple as possible for creating low power circuits with all regions of MOS operation. As a consequence EKV 2.0 formulas are used in addition to technological charts which allows an easy to use integration of fundamental advanced effects affecting strongly the accuracy. Others specific effects are beyond the scope of this paper but they could be integrated later if necessary.

2 EKV MOS MODEL

2.1 EKV 2.0 version

2.1.1 Introduction

EKV 2.0 is a fully analytical MOS model [3] dedicated to design of low-power analog circuits. This model provides continuous over inversion levels equations, in conduction as in saturation modes.
The same approach is used to derive all the equations of the model : weak and strong asymptotes are first derived, then variables of interest are normalized and linked using an appropriate interpolation function.

2.1.2 Reverse and forward current

As already introduced, EKV MOS model describes continuously drain current comportment from weak to strong inversion.
First of all, this modeling is based on the assumption that drain current can be split into the forward (i_F) and reverse (i_R) currents which describe respectively influence of source and drain voltages on the drain current :

$$I_D = I_S(i_f - i_r) = F(V_p - V_s) - F(V_p - V_d) \qquad (1)$$

where I_S is the normalization (specific) current, i_f and i_r are the forward and reverse normalized currents which depend on the pinch-off V_p, and respectively on source V_S and drain V_D voltages. These three voltages are referenced to the bulk voltage. The normalization current is defined by :

$$I_S = 2n\mu_n C'_{ox} U_t^2 \frac{W}{L} = 2n\beta U_t^2 \qquad (2)$$

where n is the slope factor, μ_n the mobility, C'_{ox} the surfacic gate oxide capacitance, U_T the thermal voltage

and $W/L = S$ the transistor aspect ratio.
Furthermore, EKV MOS model introduces the inversion level coefficient IC as being the forward normalized current i_f : under 0.1 the transistor is assumed to be in weak inversion (WI), and above 10 it reaches strong inversion (SI). Between these two limits the MOSFET is biased in moderate inversion.

2.1.3 Currents and tensions

The EKV 2.0 reverse and forward currents introduced in Eq. 1, are given by :

$$\begin{cases} i_f = ln^2(1 + e^{\frac{V_P - V_S}{2U_T}}) \\ i_r = ln^2(1 + e^{\frac{V_P - V_D}{2U_T}}) \end{cases} \quad (3)$$

with :

$$V_P \approx \frac{V_G - V_T}{n} \quad (4)$$

where V_T is the threshold voltage. These functions can be inverted to express tensions in terms of currents. More details about (1)-(4) can be found in [3].

2.2 EKV 2.6 & 3.0 versions

2.2.1 Introduction

EKV 2.6 MOS model [4] which appears in 1997, is based on inversion charge linearization versus surface potential. It is thus a more physical model than the 2.0 version, but its better accuracy results in non invertible equations.
The latest EKV 3.0 model [5]–[7] has the same physical basis as EKV 2.6 version. Consequently statics equations are the same, but major improvement come from inclusion of all major physical effects affecting static and dynamic operation of the device.

2.2.2 Reverse and forward current

As in 2.0 modeling, the drain current can be split into the forward (i_F) and reverse (i_R) currents (Eq. 1), but the normalization current I_S is now defined by:

$$I_S = 2n_q\mu_n C'_{ox} U_t^2 \frac{W}{L} = 2n_q \beta U_t^2 \quad (5)$$

where n_q is the inversion charge linearization factor, given by :

$$n_q = 1 + \frac{\gamma_s}{2\sqrt{\psi_0 + \frac{V_P}{2}}} \quad (6)$$

γ_s and ψ_0 are respectively the body factor and the surface potential.

2.2.3 Currents and tensions

As already introduced, the EKV 2.6/3.0 drain current is not invertible. In this modeling, voltages are expressed in terms of currents :

$$\begin{cases} v_p - v_s = ln(\sqrt{\frac{1}{4} + i_f} - \frac{1}{2}) + 2\sqrt{\frac{1}{4} + i_f} - 1 \\ v_p - v_d = ln(\sqrt{\frac{1}{4} + i_r} - \frac{1}{2}) + 2\sqrt{\frac{1}{4} + i_r} - 1 \end{cases} \quad (7)$$

with v_p expressed as a function of V_G, V_T and n_v :

$$v_p = \frac{V_P}{U_T} \approx \frac{V_G - V_T}{n_v} \quad (8)$$

n_v, the slope factor is given by :

$$n_v = 1 + \frac{\gamma_s}{2\sqrt{\psi_0 + V_P}} \quad (9)$$

More details about (5)-(9) can be found in [4]–[7].

3 ACCURACY AND OPTIMIZATION

As already introduced, a static design methodology dedicated to low power circuits needs continuous over inversion level equations, invertible in conduction as in saturation. The 2.0 version is the only one that meets these specifications. But this version is the oldest too, and accuracy must be taken in consideration. The solution proposed in this paper is to use the EKV 2.0 version with highlights of newer versions.

The first improvement made in EKV 3.0, was to use the slope factor n or n_v (Eq. 9) only in pinch-off voltage expression. It was remplaced in the specific current expression by the inversion charge linearization factor n_q (Eq. 6). Thus, this improvement will be included in EKV2.0 expressions (Eq. 3).

But, the main effect which affects strongly accuracy is the mobility reduction due to vertical field, and it is precisely one of EKV 2.0 modeling lacks. Indeed, the 2.0 effective mobility is defined by :

$$\mu_{eff} = \frac{\mu_n}{1 + \theta V_P} \quad (10)$$

This equation suitable for olders technologies which were slightly doped and has relatively thick oxyde is today a non realistic formulation. As shown on Fig. 1, the 3.0 version predicts a huge mobility reduction for low effective field and not a horizontal asymptote as Eq. (10) involves. This modeling takes into account effects of coulomb scattering (μ_c), phonon scattering (μ_{PH}) and surface roughness (μ_{SR}).

By taking into account the non-uniform substrate doping [8], and using a rigorous derivation of the EKV 2.6/3.0 model [9], it is possible to extract a valid mobility (Fig. 2) with EKV 2.0 formulas. By dividing the

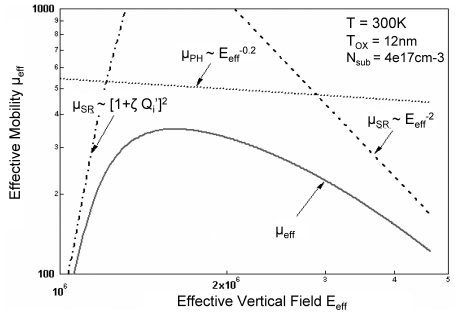

Figure 1: EKV 3.0 charge-based mobility model.

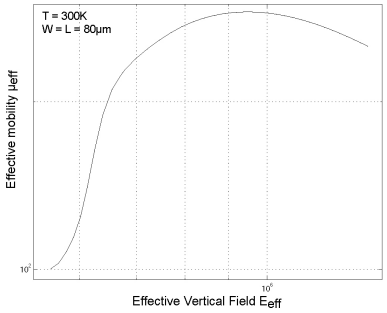

Figure 2: Mobility extracted from $0.18\mu m$ technology experimental data, with EKV 2.0 tuned formulas.

experimental drain current by the modified EKV 2.0 current without mobility, it comes :

$$\mu_{eff} = \frac{Id_{exp}}{2n_q^* C'_{ox} U_T^2 \frac{W}{L}(i_f - i_r)} \tag{11}$$

where n_q^* is the inversion charge linearization factor, modified with non-uniform substrate doping considerations [9].

4 STATIC DESIGN METHODOLOGY

4.1 First approach

The methodology proposed hereafter, takes into account the same parasitical effects as Binkley's methodology [10], but the main difference comes from integration of mobility reduction due to vertical field which has a strong influence on drain current modeling accuracy.

As shown on Fig. 3 and Fig. 4, for a given transistor, the mobility depends largely on the gate voltage V_g, and to a lesser degree, on the drain and source voltages (V_d and V_s respectively).

This weak drain voltage dependence can be ignored as soon as the drain voltage is sufficiently hight ($V_d > 200mV$). Consequently, by extracting the saturation ($V_d = V_g$) mobility for a given source voltage, the EKV 2.0 tuned saturated drain current modeling accuracy is good enough to made analog design (Fig. 5).

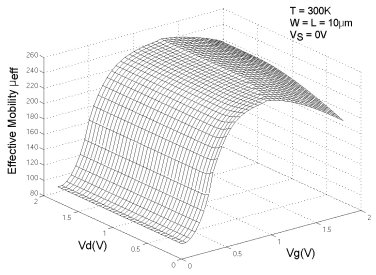

Figure 3: Effective mobility extrapolated from $0.18\mu m$ technology experimental data.

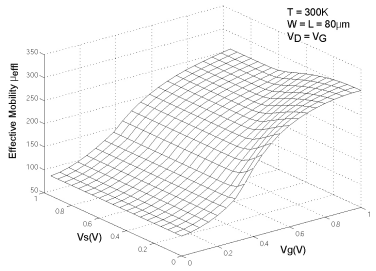

Figure 4: Effective mobility extrapolated from $0.18\mu m$ technological experimental data.

By making the same thing in conduction, it is possible to cover all regions of MOS operation with a good accuracy.

4.2 Mobility integration in SDM

As already introduced, the main objective of the SDM is to provide analog designers a tool as simple as possible for creating low power circuits without inversion level constraint. This simplicity requirement leads us to the creation of technological charts linking EKV parameters, the specific current I_S, and pinch off voltage V_P, to electrical quantities, the drain current and gate voltage.

A technological chart is associated to a transistor of a given size. But the creation of a "square" chart associated to a square transistor, linking V_g, V_P, $I_{S\square}$, and $I_{d\square}$ is possible. As $I_S = I_{S\square}\frac{W}{L}$ (and thus $I_d = I_{d\square}\frac{W}{L}$), a good knowledge of dimensional parasitic effects allows to extend the validity of this square chart to all transistors of a given technology.

4.3 Design flow

Static design methodology consists on using standard and proposed equations in addition to help of a math software (Fig. 6).

On one hand, proposed drain current [11] and standard asymptotes (when strong constraints of weak/strong

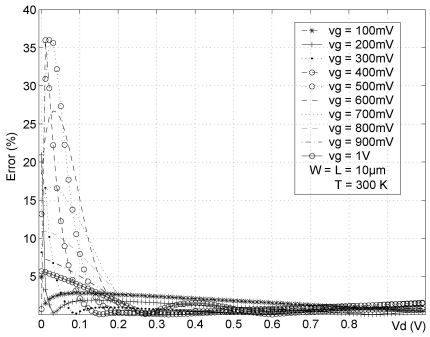

Figure 5: Error between experimental id(vd) at different vg, and SDM modeling.

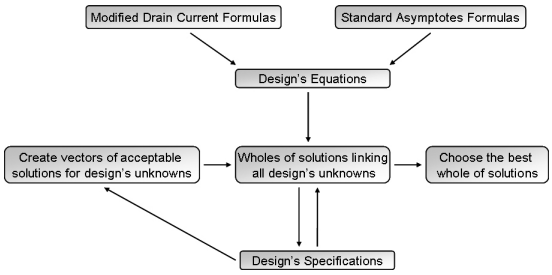

Figure 6: SDM design flow.

inversion are required) formulas lead to design's equations. On other hand, designs specifications allow the creation of wholes of acceptable solutions for each designs unknown (transistors sizes for exemple).

From this two points and the use of appropriate charts, it is possible to obtain wholes of solutions linking all design unknowns. The circuit is therefore completely described, and the best solution according to the design specifications can be chosen.

5 CONCLUSION

The Static Design Methodology presented in this paper allows analog designers to made circuits with all regions of MOS operation.

This methodology is based on the hand calculation usable EKV 2.0 formulas, but the use of technological charts, leads to a transparent integration of major parasitical effects, such as reduction mobility due to vertical field : in addition to meet the easy to use requirement of a good design methodology, it allows a very good accuracy.

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