A Simple Yet Accurate Mismatch Model
For Circuit Simulation

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ABSTRACT

As technology scales, mismatch between a pair of transistors becomes a more and more critical issue for technology development and circuit designs. Scaling also increases the complexity of compact device modeling. Sophisticated models are usually required to capture various device aspects and behaviors associated with scaling, however, they often slow down simulations. Therefore, efficient device models are highly desired, and this efficiency lies in the balance between circuit simulation accuracy and model complexity. In this work, we proposed a simple yet accurate mismatch model based on sensitivity analysis. We compared the circuit simulation results using the proposed model and our previous model in [2], and found that the proposed model is accurate enough to predict the circuit performance while it maintains simple enough for fast circuit simulations.

Keywords: mismatch, CMOS, compact model, dopant fluctuation, BSIM, op-amp, SRAM.

1 Introduction

As technology scales, mismatch between a pair of transistors becomes a more and more critical issue for technology development and circuit designs [1]. Mismatch is mainly due to random local dopant fluctuations, and other random process variation. The smaller the gate area, the larger the mismatch between devices. The resulting threshold voltage difference between a pair of devices can be as much as a few 10s of millivolts. As the threshold voltage of transistors continues to decrease as technology scales, a few 10s of mV difference in threshold voltage is extremely challenging for circuit designs sensitive to mismatch. Scaling also increases the complexity of compact device modeling. Sophisticated models are usually required to capture various device aspects and behaviors associated with scaling, however, they often slow down simulations. Therefore, efficient device models are highly desired, and this efficiency lies in the balance between circuit simulation accuracy and model complexity. In this work, we proposed a simple yet accurate mismatch model based on sensitivity analysis. We compared the circuit simulation results using the proposed model and our previous model in [2], and found that the proposed model is accurate enough to predict the circuit performance while it maintains simple enough for fast circuit simulations.

2 A simple mismatch Model

Threshold voltage and drain current sensitivity can be derived from BSIM4 model equations using the method in [3]. Data shows that the threshold voltage variation depends on drain and body biases, hence threshold voltage variation can be expressed as follows, if vth0, k2, and eta0 are treated as independent random model parameters.

\[
\delta V_{th} = \frac{\delta V_{th}}{\delta v_{th0}} \delta v_{th0} + \frac{\delta V_{th}}{\delta k_2} \delta k_2 + \frac{\delta V_{th}}{\delta \eta_0} \delta \eta_0 + E(V_{th}) \tag{1}
\]

where \(E(V_{th})\) is the error term. The abstract form of a simplified drain current in BSIM4 model can be expressed as

\[
I_{DS} = au0f(V_{th}) \tag{2}
\]

Assuming all the threshold voltage related variation is in the function term, we can treat \(u0\) as another independent random parameter to model additional current variation that \(\delta V_{th}\) cannot cover, as suggested by measured data. By analogy to Eq. (1), drain current variation can be expressed as

\[
\frac{\delta I_D}{I_D} = \frac{\delta u_0}{u_0} + \frac{\delta f(V_{th})}{f(V_{th})} + E(I_D) \tag{3}
\]

where \(E(I_D)\) is the error term. It is generally accepted that a random mismatch parameter can be modeled as having \(1/\sqrt{WL}\) dependence. Therefore, \(\delta v_{th0}, \delta k_2, \delta \eta_0,\) and \(\delta u_0\) can be expressed in a similar fashion as

\[
\delta v_{th0}, k_2, \eta_0, u_0 = \frac{m_{v_{th0}, k_2, \eta_0, u_0}}{\sqrt{WL}} \tag{4}
\]

where \(m\) is a coefficient extracted from measurement data. Eqs. (1)-(4) can be used as a simple mismatch model if the error terms are simply ignored. Our previously proposed model [2] can nicely capture the co-variance between electrical parameters and fractional power scaling of gate geometry dependence, but it introduces great complexity and slows down simulation significantly. Figs. 1 & 2 compare results from the proposed model and our previous model [2], and show that the proposed model can reasonably predict \(V_{th}\) and \(I_{DS}\) variations.

3 Model Evaluation

To further evaluate the proposed model, simulated circuit performance were compared. SRAM cell and Op-amp are chosen because these circuits are very sensitive to mismatch.
3.1 SRAM

SRAM cell has a symmetrical topology as shown in Fig. 3. Vmargin is the voltage difference between the two opposite nodes LO and C_LO during read process. Positive Vmargin ensures the latch returns from metastable state to the initial state, while negative Vmargin can flip the state of the SRAM cell. Mismatch between a pair of FETs can result in negative Vmargin, and hence cause failure of the cell during read/write process. As shown in Fig. 4, Monte Carlo result using the simple model is similar to that using the model in [2].

3.2 Operational Amplifier

Op-amp is a very fundamental block in analog circuits, and is very sensitive to mismatch due to the differential topology. If mismatch presents between the pair of differential legs, a non-zero input offset is needed to produce zero output in an Op-amp, as illustrated in Fig. 5. Mismatch in differential amplifiers can be quantified using this dc input offset voltage. Mismatch in Op-amp can degrade common-mode rejection ratio, decrease signal to noise ratio, and produce distortion at the output. As shown in Fig. 6, Monte Carlo simulation results of an Op-amp from IBM 90nm CMOS ASIC library show that proposed model has similar accuracy as the model in [2]. The proposed model, however, significantly reduced the run time.

4 Summary

A simple mismatch model is proposed based on the sensitivity analysis of the BSIM model. The model is accurate enough to predict the circuit performance, while it can significantly reduce the model extraction time, and most importantly circuit simulation time particularly for large-scale circuits.

REFERENCES

Figure 3: Schematic of a 6-Transistor SRAM cell. The SRAM cell used in the simulation is from IBM 90nm CMOS ASIC library.

Figure 4: Histogram of 5000 Monte Carlo runs using (a) model in this work (b) model in [2]. One sigma Vmargin is 24.3mV for the model in this work, and 23.1mV for the model in [2]. Vmargin is the voltage difference between the two opposite nodes LO and C_LO during read process. Positive Vmargin ensures the latch returns from metastable state to the initial state, while negative Vmargin can flip the state of the SRAM cell.

Figure 5: If mismatch presents between the pair of differential legs, a non-zero input offset is needed to produce zero output in an Op-amp. Op-amp used in this work is from IBM 90nm CMOS ASIC library.

Figure 6: Histogram of 500 Monte Carlo runs using (a) model in this work (b) model in [2]. One sigma input offset voltage is 2.30mV for the model in this work, and 2.32mV for the model in [2].