High-Voltage LDMOS Compact Modelling

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ABSTRACT

In compact modelling of high-voltage LDMOS devices often a sub-circuit approach is used. While for the channel region a standard compact MOS model (for example BSIM4, MM11 or PSP) is used, the drift region is described by a compact JFET model. We will show that using this conventional approach the effects of the widening of the depletion region in the lateral direction cannot be taken into account properly. As a consequence the voltage at the internal node between channel and drift region becomes unphysical and accurate physics-based capacitance modelling becomes unfeasible.

In this paper we will introduce a new approach for compact LDMOS modelling to remedy these shortcomings. Next this new approach is compared with device simulations and measurements for both currents and capacitances. Finally we describe the method to implement this approach in a circuit simulator.

Keywords: high-voltage, LDMOS, compact modelling

1 INTRODUCTION

High-voltage LDMOS devices are extensively used in all kinds of integrated power circuits, e.g., switch-mode power supplies. RF application areas of these devices include power amplifiers, wireless communication, automotive applications, and base stations. In Figure 1 a cross-section of a RF-LDMOS device is shown. The p^+-well is diffused from the source-side under the gate (G) and forms a graded inversion channel region. To withstand the high voltages applied between source (S) and drain (D), a lightly doped n^--drift region is located between the channel region and the heavily doped n^{++}-drain contact region. For some applications the gate extends over the drift region. Consequently in the linear operating regime an accumulation layer forms under the thin gate oxide in the drift region and the on-resistance is lowered. For RF applications, however, the gate does not extend over the drift region in order to minimize the feedforward and feedback or Miller capacitances.

Versatile design of RF applications of LDMOS transistors requires compact models for circuit simulation, which accurately describe the electrical characteristics, i.e., currents and capacitances, over a wide range of bias conditions. The specific high-voltage aspects of an LDMOS device are not incorporated in standard compact MOS models like BSIM4 and PSP. Therefore a dedicated LDMOS modelling approach is necessary.

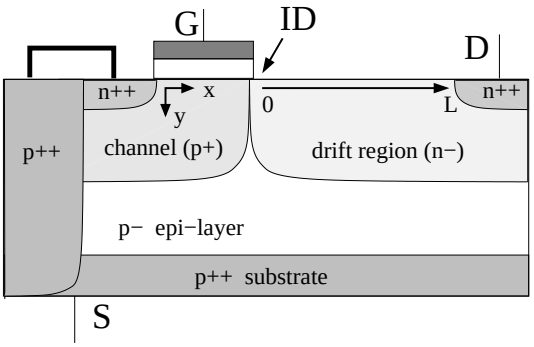

Figure 1: Cross-section of an n-type high-voltage RF-LDMOS transistor. The p^+-well is diffused from the source-side and forms a graded channel region. The internal drain (ID) is the boundary between the channel region (0.4 μm) and drift region (3.5 μm). Note that the gate (G) does not extend over the lightly doped n^--drift region.

Part of this work has been published elsewhere [1].

2 EVALUATION OF EXISTING COMPACT MODELS

Recently we introduced a new single compact model for LDMOS transistors, MOS Model 20 [2]-[4]. This model gives an accurate description of the LDMOS characteristics, including the capacitance behaviour, as can be seen from Figures 2 and 3. It should be noted, however, that MOS Model 20 has been developed to describe device structures with a gate extending over the lightly-doped drift region. In these devices at high gate-source voltages an accumulation layer is formed in the drift region, resulting in a non-zero feedforward capacitance (see Figure 2). In Figure 4 the feedforward capacitance of the RF-LDMOS device from Figure 1 is shown. At high gate-source voltages this capacitance drops to zero. In Figure 5 the input capacitance of the RF-LDMOS device from Figure 1 is shown. In inversion at a gate-

source voltage of about 5 V a peak is observed, which is much more pronounced than for devices with the gate extending over the drift region (see Figure 3) and which exceeds the oxide capacitance.

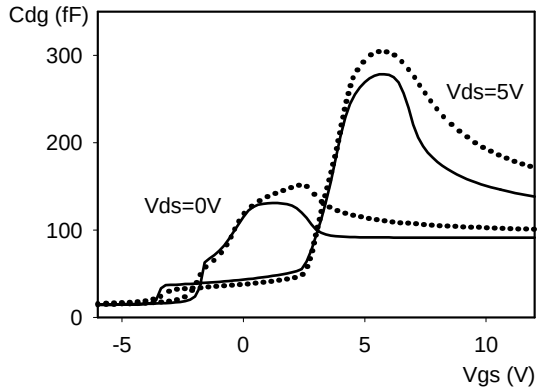

Figure 2: Measured (symbols) and simulated (solid lines) feedforward capacitance C_{DG} of a device with the gate extending over the drift region as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS} of 0 and 5 V, respectively. MOS Model 20 was used for the simulations.

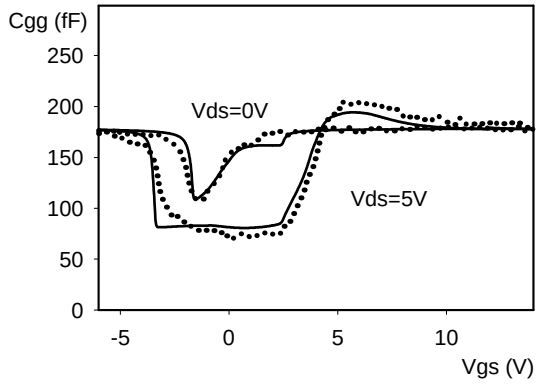

Figure 3: Measured (symbols) and simulated (solid lines) input-capacitance C_{GG} of a device with the gate extending over the drift region as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS} of 0 and 5 V, respectively. MOS Model 20 was used for the simulations.

For the input capacitance of the LDMOS device the following equation holds

$$C_{\mathrm{GG}}^{\mathrm{LDMOS}} = C_{\mathrm{GG}}^{\mathrm{channel}} - C_{\mathrm{GID}}^{\mathrm{channel}} \cdot \frac{\partial V_{\mathrm{ID}}}{\partial V_{\mathrm{G}}} \qquad (1)$$

From this equation it can be seen that the gate-drain capacitance of the channel region contributes to the input capacitance. Moreover this gate-drain capacitance is amplified by the gate-induced variation of the internal drain bias. Consequently the correct description of the

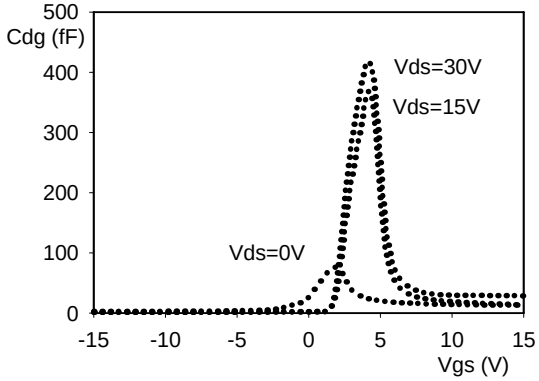

Figure 4: Measured feedforward capacitance C_{DG} of an RF-LDMOS transistor as a function of gate-source voltage V_{GS} for drain-source voltages V_{DS} of 0, 15 and 30 V.

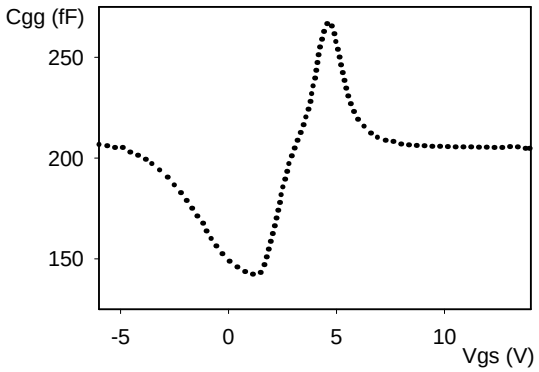

Figure 5: Measured input-capacitance C_{GG} of an RF-LDMOS transistor as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS} of 26 V.

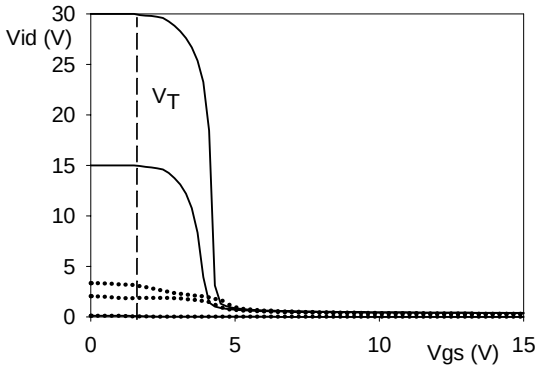

Figure 6: Voltage at the internal drain V_{ID} as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS} of 0.1, 15 and 30 V. Symbols represent device simulation (Medici) and solid lines represent simulations using a subcircuit approach with MOS Model 11 and MiOS Model 31.

voltage at the internal drain is of crucial importance for the modelling of LDMOS capacitances.

As MOS Model 20 is not suited for the modelling of the RF-LDMOS device of Figure 1, the conventional subcircuit approach has been tried. The channel region was modelled with MOS Model 11, while the drift region was modelled with MOS Model 31, a JFET-type model including velocity saturation [4]. In Figure 6 the voltage at the internal drain (ID) resulting from this subcircuit approach is compared with device simulations. The subcircuit model yields values for the voltage at the internal drain which are about one order of magnitude too high. Consequently, also the multiplication factor $-\partial V_{\mathrm{ID}}/\partial V_{\mathrm{G}}$ for the gate-drain capacitance is much too high. This observation explains the overestimation of the input capacitance when the subcircuit model is used (see Figure 7).

3 MISSING PHENOMENA IN EXISTING DRIFT REGION MODEL

From device simulations it was found that for the RF-device structure of Figure 1 the depletion starts from the junction of p^+-doped channel region and the n^--doped drift region, while the remaining part of the drift region stays neutral. We will call this situation partial lateral depletion (PLD), because with increasing external drain bias the depletion region moves laterally towards the drain contact [see (A) in Figure 8]. Once the drain contact has been reached, the current is limited by the space charge and the electrical field peaks at the drain contact [see (B) in Figure 8]. These situations can occur at almost all current levels as is illustrated in Figure 9.

The current MOS Model 31 only contains vertical depletion from the top surface and from the bottom junction between the n^--doped drift region and p^--doped epi-layer (see Figure 1). Consequently, the subcircuit consisting of MOS Model 11 for the channel region and and MOS Model 31 for the drift region fails to correctly describe the voltage at the internal drain (see Figure 6) and the input capacitance (see Figure 7).

4 IMPROVED DRIFT REGION MODEL

The one-dimensional Poisson equation for the drift region reads

$$\frac{dE}{dx} = \frac{qN_{\mathrm{d}}}{\varepsilon_{\mathrm{Si}}}\left(1 - \frac{I}{qN_{\mathrm{d}}Av_{\mathrm{dr}}}\right) \qquad (2)$$

where E is the lateral electrical field, N_{d} is the doping concentration, I is the current, A is the area (depth times width) of the drift region, and v_{dr} is the drift

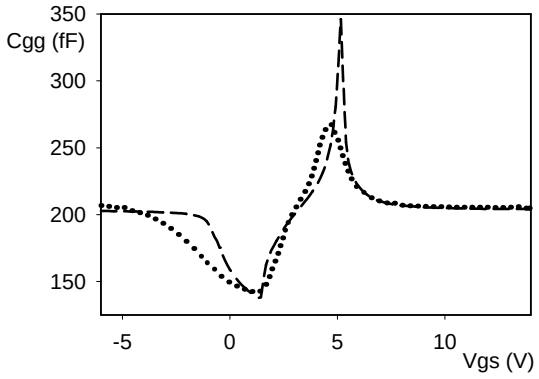

Figure 7: Measured (symbols) and simulated (dashed line) input capacitance C_{GG} of an RF-LDMOS transistor as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS} of 26 V. For the simulations a subcircuit approach with MOS Model 11 and MOS Model 31 was used.

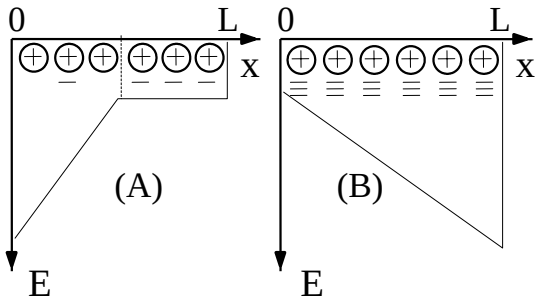

Figure 8: Charge distribution and lateral electric field inside the drift region for partial lateral depletion (A) and space-charge limited current flow (B): $\oplus$ indicate ionized donors, and $-$ indicate mobile electrons.

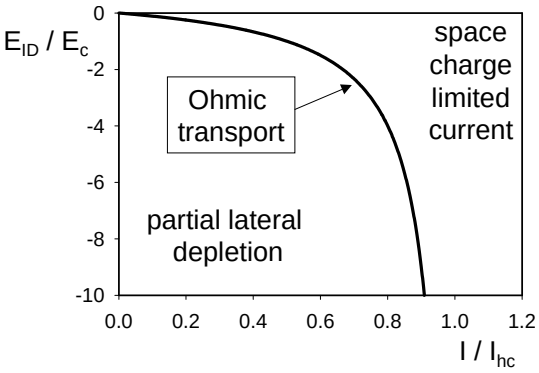

Figure 9: Diagram showing the operational modes of the drift region as a function of the normalized current and the normalized electrical field at the internal drain (or beginning of the drift region). See Eq. 3 for the definition of the critical field E_{c} and Eq. 5 for the definition of the hot-carrier current I_{hc}.

velocity given by

$$v_{\rm dr} = \frac{\mu_0 E}{1 + |E|/E_{\rm c}} \tag{3}$$

where μ_0 is the zero-field mobility, and $E_{\rm c}$ is the critical field given by $E_{\rm c} = v_{\rm sat}/\mu_0$, where $v_{\rm sat}$ is the saturated drift velocity. Integration of Eq. 2 yields

$$\left(1 - \frac{I}{I_{\rm hc}}\right)^2 = \frac{\varepsilon_{\rm Si} E_{\rm c}}{q N_{\rm d} L} \left\{ \left(1 - \frac{I}{I_{\rm hc}}\right) \left(\frac{E_{\rm L} - E_0}{E_{\rm c}}\right) - \frac{I}{I_{\rm hc}} \ln\left[\frac{(E_{\rm c} - E_{\rm L})I + E_{\rm L} I_{\rm hc}}{(E_{\rm c} - E_0)I + E_0 I_{\rm hc}}\right] \right\} \tag{4}$$

where L is the length of the drift region (see Figure 1), E_0 is the electrical field at the beginning of the drift region, $E_{\rm L}$ is the electrical field at the end of the drift region and $I_{\rm hc}$ is the hot-carrier current given by

$$I_{\rm hc} = q N_{\rm d} A\, v_{\rm sat} \tag{5}$$

Integrating once more yields the following expression for $V_{\rm dr}$, the voltage over the drift region,

$$V_{\rm dr} = E_{\rm c} L \left(\frac{I}{I_{\rm hc} - I}\right) - \frac{\varepsilon_{\rm Si}\left(E_{\rm L}^2 - E_0^2\right)}{2 q N_{\rm d}\left(1 - I/I_{\rm hc}\right)} \tag{6}$$

In order to solve the current from Eqs. 4 and 6 one needs to know E_0 or $E_{\rm L}$. As the lateral electrical field at the beginning of the drift region, E_0, is non-zero, we use the continuity of this lateral electrical field —going from channel to drift region— as an additional boundary condition. Expressions for the lateral electrical field at the end of the channel region can be obtained from the compact MOS model, MOS Model 11, used to describe the channel region. For the linear operation region one has

$$E_{\rm lat}^{\rm lin} = \frac{I}{Q_{\rm inv} \beta L_{\rm ch}} \tag{7}$$

where $Q_{\rm inv}$ is the inversion charge density in the channel, $L_{\rm ch}$ is the effective channel length and β is the gain factor of the channel. For the saturation region one finds

$$E_{\rm lat}^{\rm sat} = E_{\rm c} \cosh\left(\frac{\Delta L_{\rm ch}}{l_{\rm CLM}}\right) \tag{8}$$

where $\Delta L_{\rm ch}$ is the amount of channel length modulation (CLM) and $l_{\rm CLM}$ is the channel length modulation parameter [5].

Using the improved model formalism described above the voltage at the internal drain is evaluated (see Figure 10). Comparing Figures 6 and 10 one can see that the description of the voltage at the internal drain is drastically improved.

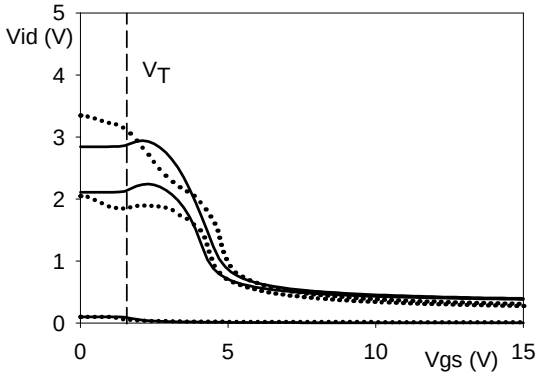

Figure 10: Voltage at the internal drain $V_{\rm ID}$ as a function of gate-source voltage $V_{\rm GS}$ for a drain-source voltage $V_{\rm DS}$ of 0.1, 15 and 30 V. Symbols represent device simulation (Medici) and solid lines represent simulations using our new modelling approach.

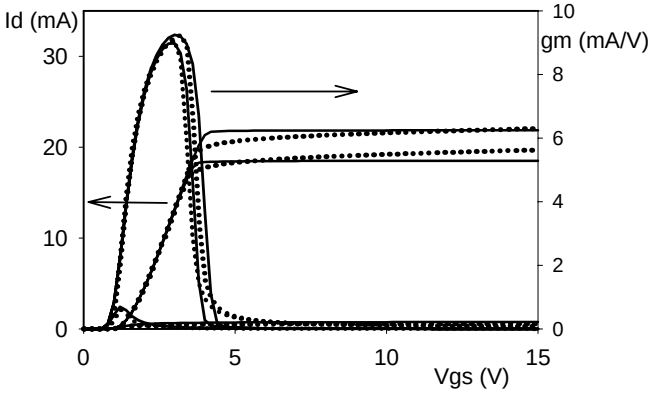

Figure 11: Drain current and transconductance as a function of gate-source voltage at drain-source voltages of 0.1, 15 and 30V. Symbols represent device simulations (Medici) and solid lines represent our new modelling approach.

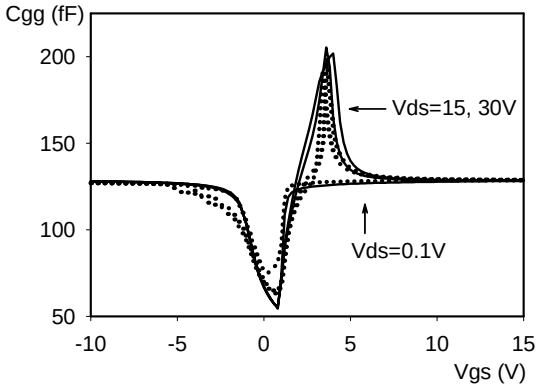

Figure 12: Input capacitance $C_{\rm GG}$ as a function of gate-source voltage at drain-source voltages of 0.1, 15 and 30V. Symbols represent device simulations (Medici) and solid lines represent our new modelling approach.

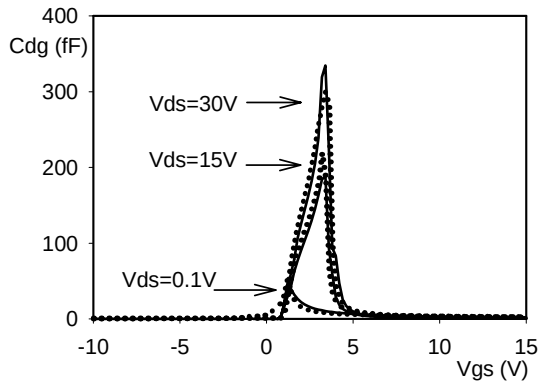

Figure 13: Feedforward capacitance C_{DG} as a function of gate-source voltage at drain-source voltages of 0.1, 15 and 30V. Symbols represent device simulations (Medici) and solid lines represent our new modelling approach.

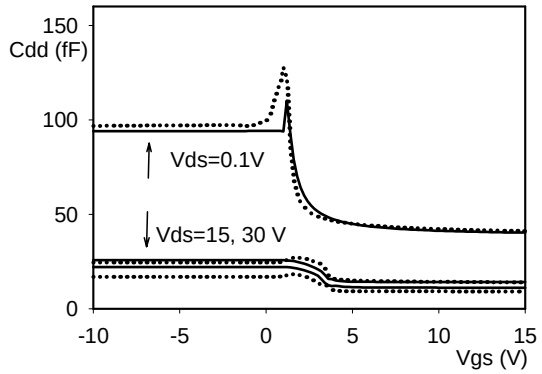

Figure 14: Output capacitance C_{DD} as a function of gate-source voltage at drain-source voltages of 0.1, 15 and 30V. Symbols represent device simulations (Medici) and solid lines represent our new modelling approach.

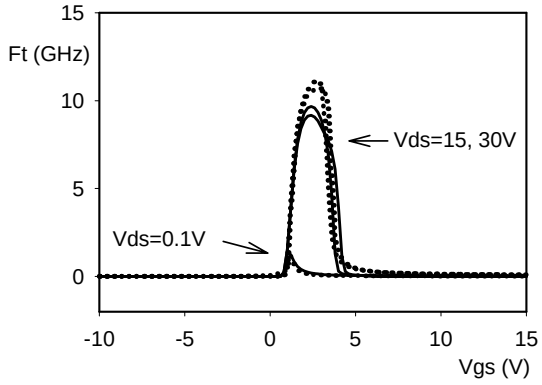

Figure 15: Cut-off frequency f_{T} as a function of gate-source voltage at drain-source voltages of 0.1, 15 and 30V. Symbols represent device simulations (Medici) and solid lines represent our new modelling approach.

5 COMPARISON WITH DEVICE SIMULATIONS

Device simulations using Medici have been performed for the RF-LDMOS transistor of Figure 1. A comparison between the results from these device simulations and our new RF-LDMOS modelling approach is presented in the following figures:

- drain current and transcapacitance in Figure 11;
- input capacitance C_{GG} in Figure 12;
- feedforward capacitance C_{DG} in Figure 13;
- output capacitance C_{DD} in Figure 14;
- cut-off frequency f_{T} in Figure 15.

From these figures it can be seen that all these characteristics are accurately described by our new modelling approach.

6 COMPARISON WITH MEASUREMENTS

Both dc and ac measurements have been performed on the RF-LDMOS transistor of Figure 1. Small-signal Y-parameters have been measured at a frequency of 1 GHz. Capacitances were obtained from the small-signal Y-parameters after open-short de-embedding. A comparison between these experimental results and our new RF-LDMOS modelling approach is presented in the following figures:

- drain current in Figure 16;
- input capacitance C_{GG} in Figure 17;
- cut-off frequency f_{T} in Figure 18.

From these figures it can be seen that all the measured characteristics are accurately described by our new modelling approach.

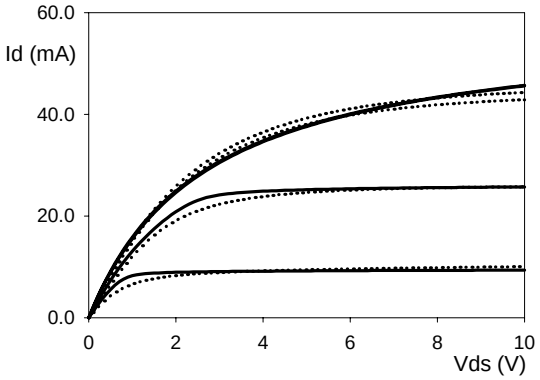

Figure 16: Drain current as a function of drain-source voltage at gate-source voltages of 3, 4, 10 and 15V. Symbols represent measurements and solid lines represent our new modelling approach.

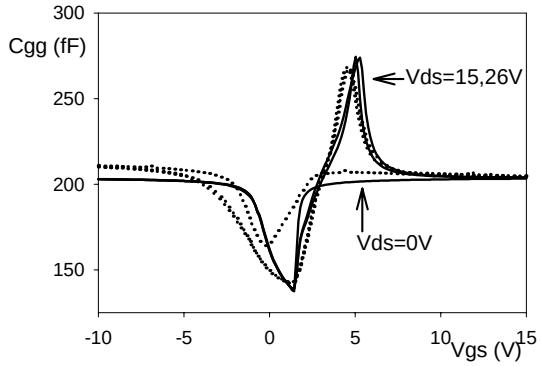

Figure 17: Input capacitance C_{GG} as a function of gate-source voltage at drain-source voltages of 0, 15 and 26V. Symbols represent measurements and solid lines represent our new modelling approach.

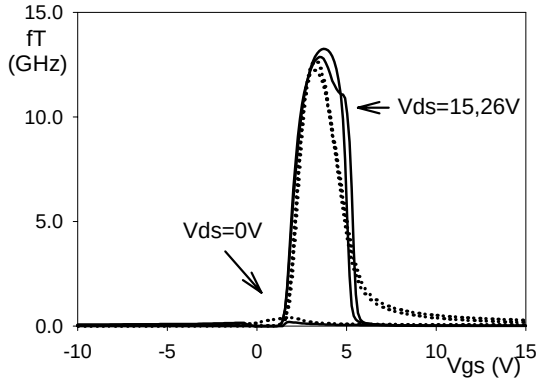

Figure 18: Cut-off frequency f_{T} as a function of gate-source voltage at drain-source voltages of 0, 15 and 26V. Symbols represent measurements and solid lines represent our new modelling approach.

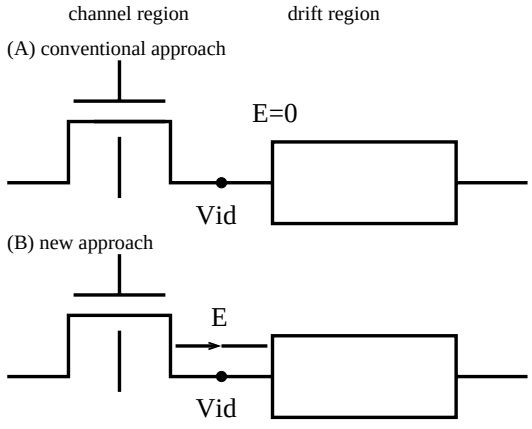

Figure 19: Conventional subcircuit for an LDMOS (top; A) and subcircuit for an LDMOS using our new modelling approach (bottom; B).

7 IMPLEMENTATION IN CIRCUIT SIMULATORS

In a circuit simulator at each node the sum of all currents is made equal to zero (based on Kirchoff's law). Consequently, if an LDMOS transistor is modelled using a subcircuit with separate models for channel region and drift region, only the currents and voltages at the internal drain are made equal [see (A) in Figure 19]. In our new modelling approach also the condition has to be imposed that at the internal drain the lateral electrical field in the channel region is equal to the lateral electrical field in the drift region [see (B) in Figure 19]. Consequently, both the model for the channel region and the model for the drift region have to be extended with an additional terminal, representing the lateral electrical field at the and of the channel and beginning of the drift region, respectively.

8 SUMMARY

In high-voltage RF-LDMOS transistors with gates that do not extend over the drift region, lateral depletion of the drift region occurs. This has to be incorporated in the model for this drift region in order to accurately describe the peaking of the input capacitance which can amount up to about 1.4 times the oxide capacitance.

We have presented a model for the drift region including this lateral depletion effect. Part of this new model is an additional boundary condition at the internal drain, which is the point where channel region and drift region meet. At this internal drain continuity of the lateral electrical field is imposed. Consequently, both the model for the channel region and the model for the drift region need to have an additional terminal, representing this lateral electrical field.

Using this new modelling approach excellent agreement with both TCAD simulations and measurements has been obtain for dc characteristics, capacitances and high-frequency characteristics, e.g., cut-off frequency f_{T}.

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