Capacitance Model for Four-Terminal DG MOSFETs

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ABSTRACT

We present an intrinsic capacitance model for undoped-channel full-deplete DG MOSFETs with two independent gates of different gate-oxide thickness. The basis of the model is double charge-sheet four-terminal compact model of DG MOSFET with carrier velocity saturation. We considered five intrinsic capacitances C_{G1S}, C_{G1D}, C_{G2S}, C_{G2D}, and C_{G1G2}. Since total charge in the channel can be calculated analytically, these capacitances are obtained by differentiating it. Anomaly of C_{G1G2} was found in the sub-threshold region when the transistor is in the double charge-sheet mode. This can be explained by the redistribution of the carriers between two charge-sheets when the gate voltages is changed, resulting in the screening current against the perpendicular electric field. To remedy this effect, it was found that the charge-sheets should be placed at the mean position of the carriers, instead at the silicon-insulator interface.

Keywords: double-gate, MOSFET, compact model, capacitance.

1 INTRODUCTION

Double-gate field effect transistors (DG MOSFETs) have recently gained much attention, and they are now considered, in ITRS 2005 roadmap, as the future principal device structure. We proposed a compact model of the DG MOSFETs based on the double charge-sheet model. The model can handle different gate-oxide thickness and independent gate voltage for two gates[(1)]. It was modified to include carrier-velocity saturation, and mobility change by the surface electric-field[(2)]. To complete the model suitable to a SPICE module, it is necessary to add the capacitance model based on an equivalent circuit for the transistor. As the first step, we present in this report an intrinsic capacitance model, which is derived from the derivatives of the channel charge.

2 MODELING

The model is for undoped-channel full-deplete DG MOSFETs with two independent gates of different gate-oxide thickness. The model uses gradual channel approximation and double charge-sheet assumption with no current mixing between the two sheets in the entire channel. In the drift-diffusion transport, carrier-velocity saturation is explicitly described:

$$-q\mu\left(\frac{q}{C}\frac{dn}{dy}n+\frac{kT}{q}\frac{dn}{dy}\right)=I_{\mathrm{D}}\left(1+\left|\frac{E}{E_{\mathrm{c}}}\right|^{2}\right)^{1/2} \tag{1}$$

where μ is the low-field mobility, n is the carrier density, C is the effective capacitance[(1)], E (=(q/C)dn/dy) is the electric field along the channel, E_{c} is the critical electric field that characterizes the velocity saturation, and I_{D} is the drain current for the respective charge-sheet. Introduction of the carrier-velocity saturation is accurate enough when the drift current dominates the total current. It can be rewritten as,

$$\sqrt{n_{\mathrm{a}}^{2}-n_{\mathrm{b}}^{2}}\,\frac{dn_{\mathrm{a}}}{dy}=-\beta E_{\mathrm{c}}n_{\mathrm{b}} \tag{2}$$

$$n_{\mathrm{a}}=n/\left(CkT/q^{2}\right)+1$$

$$n_{\mathrm{b}}=\left(I_{\mathrm{D}}/q\mu E_{\mathrm{c}}\right)/\left(CkT/q^{2}\right).$$

Source carrier density is obtained by solving the one-dimensional Poisson equation. Since saturated carrier-velocity requires limited lowest value of drain-end carrier density, the transition point, beyond which carriers are driven by the drain electric field, is introduced.

2.1 Equivalent circuit

The DG MOSFET equivalent circuit that we supposed is shown in Figure 1. We considered five intrinsic capacitances C_{G1S}, C_{G2S}, C_{G1D}, C_{G2D}, C_{G1G2}, neglecting C_{SD}. Compared to the equivalent circuit of bulk MOSFETs, body-related capacitances are absent, while gate-related capacitances for the second gate are added. Other circuit element in the model is only the current source that represents the channel current. The source and drain resistance is shown in the figure but it is considered to be

the outside of the intrinsic model. Therefore, source and drain voltage cited in the model are the voltages at the cross-points just inside the channel.

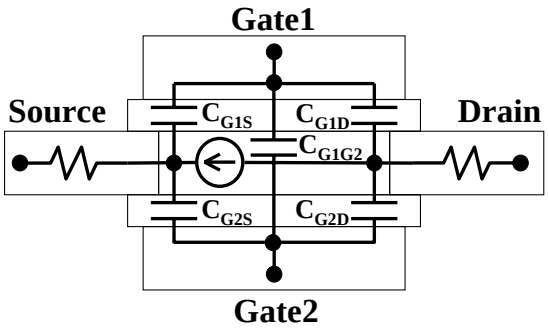

Figure 1: DC equivalent circuit of DG MOSFET.

2.2 Capacitance formulation

Charge Q_i (i=1, 2) in charge-sheet i can be obtained by using eq. (2).

$$\begin{aligned} Q_i &= -\frac{CkT}{q}\int_0^{L_{\text{eff}}}(n_{\text{a}}-1)dy \\ &= -\frac{CkT}{q}\left(\int_{n_{\text{a}0}}^{n_{\text{aL}}} n_{\text{a}}\left(\frac{dn_{\text{a}}}{dy}\right)^{-1} dn_{\text{a}} + L_{\text{eff}}\right) \\ &= \frac{CkT}{q}\left(\frac{1}{\beta E_{\text{c}} n_{\text{b}}}\int_{n_{\text{a}0}}^{n_{\text{aL}}} n_{\text{a}}\sqrt{n_{\text{a}}^2-n_{\text{b}}^2}\,dn_{\text{a}} + L_{\text{eff}}\right) \end{aligned} \tag{3}$$

where $n_{\text{a}0}$ is n_{a} at the source-end, and n_{aL} is that at the effective drain-end which is equivalent to the drain-end when the current is not saturated. When the current is saturated, L_{eff} is the transition point, and the above charge is only for the part of the total charge from the source to the transition point. Charge density beyond the transition point is assumed to be the average of the charge density at the transition point and that at the drain-end.

Gate charge is linear combination of the charge in the charge-sheets.

$$Q_{\text{G1}} = C_{\text{tot}}(V_{\text{G1}}-V_{\text{G2}}) - \frac{C_{\text{OX1}}}{C_{11}}Q_1 - \left(1-\frac{C_{\text{OX2}}}{C_{22}}\right)Q_2$$

$$Q_{\text{G2}} = C_{\text{tot}}(V_{\text{G2}}-V_{\text{G1}}) - \left(1-\frac{C_{\text{OX1}}}{C_{11}}\right)Q_1 - \frac{C_{\text{OX2}}}{C_{22}}Q_2$$

$$C_{\text{tot}} = \left(C_{\text{OX1}}{}^{-1} + C_{\text{Si}}{}^{-1} + C_{\text{OX2}}{}^{-1}\right)^{-1}$$

$$C_{11} = C_{\text{OX1}} + \left(C_{\text{Si}}{}^{-1} + C_{\text{OX2}}{}^{-1}\right)^{-1}$$

$$C_{22} = \left(C_{\text{OX1}}{}^{-1} + C_{\text{Si}}{}^{-1}\right)^{-1} + C_{\text{OX2}}$$

where Q_{G1} (Q_{G2}) is charge of the gate 1 (2) metal, and Q_1 (Q_2) is charge in the charge-sheet 1 (2).

There are 8 derivatives of the gate charges, which are derivatives of Q_{G1} and Q_{G2} with respect to the V_{S}, V_{D}, V_{G1} and V_{G2} (source, drain, gate1 and gate2 voltages). Among them, two derivatives are dependent to other derivatives, i.e.

$$\frac{dQ_i}{dV_{\text{S}}} = -\left(\frac{d}{dV_{\text{D}}} + \frac{d}{dV_{\text{G1}}} + \frac{d}{dV_{\text{G2}}}\right)Q_i \quad (i = \text{G1, G2}),$$

leaving 6 derivatives independent. On the other hand, number of capacitances in the circuit is 5. Therefore, there is one constriction more than needed. Relations among them are as follows.

$$\frac{\partial Q_{\text{G1}}}{\partial V_{\text{G1}}} = C_{\text{G1S}} + C_{\text{G1G2}} + C_{\text{G1D}}$$

$$\frac{\partial Q_{\text{G2}}}{\partial V_{\text{G2}}} = C_{\text{G2S}} + C_{\text{G2G1}} + C_{\text{G2D}}$$

$$\frac{\partial Q_{\text{G1}}}{\partial V_{\text{D}}} = -C_{\text{G1D}}, \qquad \frac{\partial Q_{\text{G2}}}{\partial V_{\text{D}}} = -C_{\text{G2D}}$$

$$\frac{\partial Q_{\text{G1}}}{\partial V_{\text{G2}}} = -C_{\text{G1G2}}, \qquad \frac{\partial Q_{\text{G2}}}{\partial V_{\text{G1}}} = -C_{\text{G2G1}}$$

Note that the capacitance between gate1 and gate2 is defined in two ways.

2.3 Charge-sheet position

Figure 2 shows calculated C_{G1G2} and C_{G2G1}, by changing the gate voltages of the two gates in anti-phase fashion. In the figure, lines labeled as 'fixed charge-sheet position' are the calculation assuming the charge-sheets are at the Si-SiO_2 interfaces. Beside the fact that these two lines do not match each other, there is step-like increase in the capacitance, where the device condition changes from single charge-sheet mode to double-charge-sheet mode. It was found such an anomaly is commonly observed under the sub-threshold condition. Even when the device is in deep sub-threshold condition, the terrace height does not diminish while the terrace width narrows.

Since the carrier density in the sub-threshold region is thin, the double charge-sheet mode occurs only when two gates gives almost equal surface potentials. Under this condition a small change in the gate voltage causes redistribution of the carriers between two charge-sheets, while total carrier is almost unchanged. This redistribution is model artifact caused by the assumption that the charge-sheets reside at the silicon-SiO_2 interfaces irrespective to the real charge distribution. This redistribution results in the screening current against the perpendicular electric

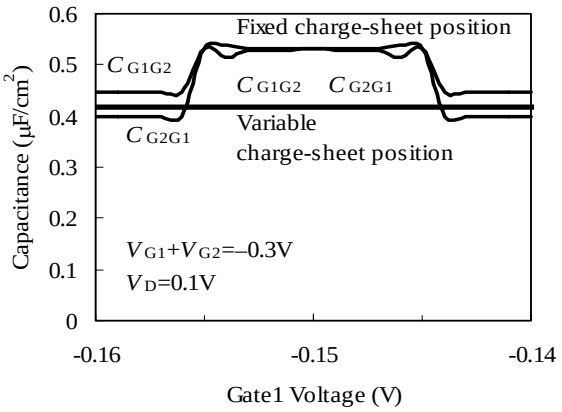

Figure 2: calculated C_{G1G2} and C_{G2G1}, for a device with 10nm thick silicon channel, and 2nm thick gate oxides. Two method of calculation, fixed and variable charge-sheet position is compared.

field. Calculation assuming thin carrier density indicates that C_{G1G2} should approach

$$C_{tot}\left(1+\frac{C_{tot}}{C_{Si}}\right)$$

instead of C_{tot}.

To remedy this effect, it was found that the charge-sheets should be placed at the mean position of the carriers at the source-end, instead these are placed at the silicon-insulator interface.

The mean position x_{ch} of the charge sheet is

$$x_{ch1,ch2}=\frac{\psi_{S1,S2}-\psi_M}{E_{\perp S1,S2}}$$

in the case of double charge-sheet, and is

$$x_{ch1}=\frac{(\psi_{S1}-\psi_{S2})-t_{Si}E_{\perp S2}}{E_{\perp S1}-E_{\perp S2}}$$

in the case of single charge-sheet. In these formulae, ψ_{S1} (ψ_{S2}) is the surface potential, ψ_M is the potential minimum, $E_{\perp S1}$ ($E_{\perp S2}$) is the surface electric field.

Two lines, in figure 2, labeled as 'variable charge-sheet position' show the result of the renewed method. Anomaly is now eliminated.

Modification in the charge-sheet position changes drain current, but the effect was found rather small.

3 RESULT

Figure 3 shows the calculated capacitances for three-terminal operation of the DG MOSFET where the identical voltage is applied to two gates. The device assumed is with 50nm channel length, 10nm channel thickness, and with 2nm thick gate oxides. Gate conductor is assumed to be polysilicon.

Although C_{G1G2} does not have any meaning when the two gates are physically tied, we leave it shown for reference. Capacitances are normalized by unit area, where the gate area is doubled in the case of three-terminal operation. When the drain voltage is high (the upper figure) C_{GD} is almost zero indicating that the drain terminal does not have controllability on the gate charge. On the other hand, C_{GD} approaches to C_{GS} when the drain voltage is small (lower figure). The value, however, does not coincide even if V_{DS}=0. This is not observed in the real device. This is caused by the asymmetrical modeling with respect to the source and the drain.

Figure 4 shows the capacitances for four-terminal operation of the DG MOSFET where gate 2 is fixed to –0.4V. The device is in single charge-sheet mode over the entire range. Again C_{G1D} and C_{G1S}, and C_{G2D} and C_{G2S} do not coincide even the drain voltage is very small.

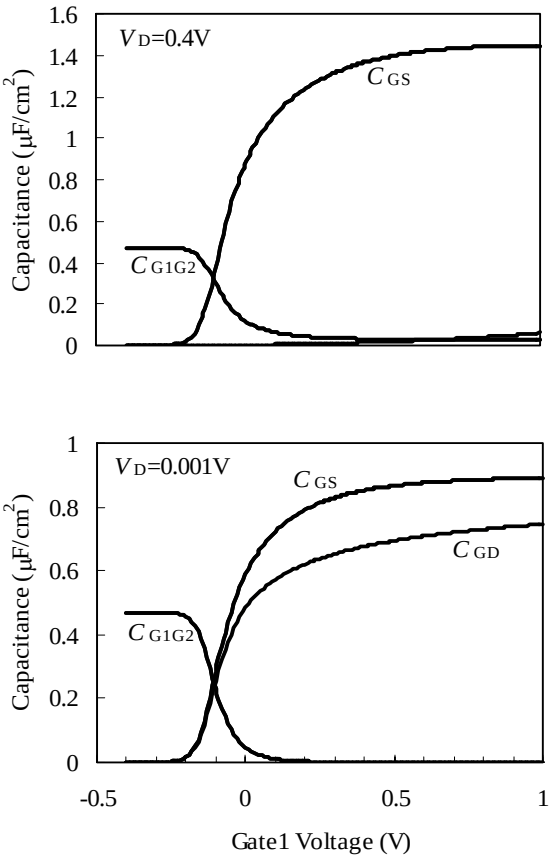

Figure 3: Capacitances for three terminal DG MOSFET.

In the figure, C_{G1G2} and C_{G2G1} seems almost coincide. But these two change drastically each other especially when channel charge screens the electric field across the channel. Such a situation is shown in Figure 5. In the figure, the device is operating in double charge-sheet mode. Since channel carrier density is high, both C_{G1G2} and C_{G2G1} are small compared to C_{tot}. But the values, in itself, are quite different each other.

This phenomenon is also observed in the result of ATLAS device simulator with the device configuration of an extraordinary short drain region to mimic the intrinsic part of the compact model, where capacitances are calculated by exactly the same procedure defined in this report. In real devices, C_{G1G2} and C_{G2G1} can be different. One possible cause is the presence of drain resistance. Change in the gate voltage changes channel current which, in turn, changes the drain voltage at the intrinsic drain node. This results in the contribution of capacitive current through C_{G1D} and C_{G2D} for the measurement of dQ_{G1}/dV_{G2} and dQ_{G2}/dV_{G1}. Because C_{G1D} and C_{G2D} are different each other at asymmetric gate voltages, contribution to the derivative differs.

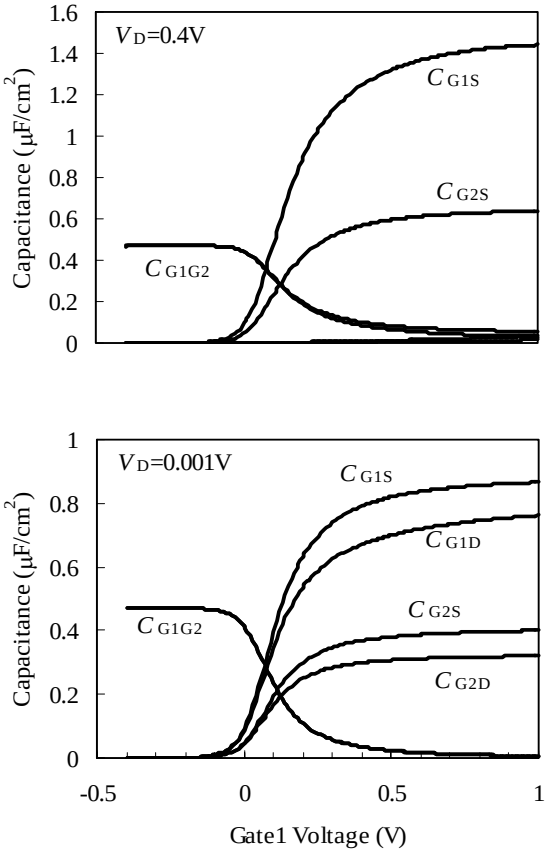

Figure 4: Capacitances for four terminal DG MOSFET, with gate 2 voltage fixed to -0.4V.

This fact implies that, even in the case of the intrinsic model, we should introduce an unorthodox capacitance element between G1 and G2, or we should introduce resistive element at the drain end.

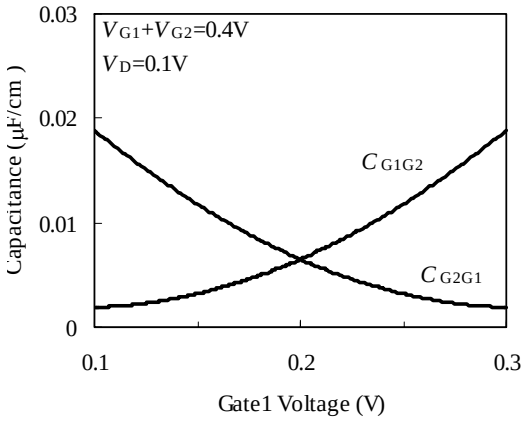

Figure 5: C_{G1G2} and C_{G2G1} in four terminal DG MOSFET.

4 SUMMARY

An intrinsic capacitance model which is derived from the derivatives of the gate charges, was presented. Based model is for undoped-channel full-deplete DG MOSFETs with two independent gates of different gate-oxide thickness. Capacitance anomaly, which occurs when the channel is in the sub-threshold region with the almost identical gate voltages to form two charge-sheets, is discussed. Modification of the model by changing the position of charge-sheets at the mean position of the carrier is proposed to remedy the anomaly, and it is confirmed by the calculation.

REFERENCES

[1] T. Nakagawa, T. Sekigawa, T. Tsutsumi, E. Suzuki, and H. Koike; "Primary Consideration on Compact Modeling of DG MOSFETs with Four-terminal Operation Mode," Tech. Digest Nanotech 2003, Vol. 2, (2003)330.

[2] T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki and H. Koike; "Compact Model for Ultra-Short Channel Four-Terminal DG MOSFETs for Exploring Circuit Characteristics," Tech. Proc., WCM 2005, (2005)183.