Design and Fabrication of Flexible OTFT Array by using Nanocontact Printing

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ABSTRACT

The high-resolution and large-area flexible OTFT array to use as a driving device for an OLED was designed and fabricated in the nanocontact printing process and organic thin films could be deposited even in a room temperature process. The gate, source, and drain electrode patterns of OTFT were fabricated through the nanocontact printing process using as a mask PDMS stamp on which an SAM used as an etching mask was inked selectively. To fabricate an OTFT array, an E-beam deposition device with a low-temperature inside a chamber was used to deposit Cr as an adhesion layer, to deposit a thin film of Au as an etching layer, and to create a conductive gate electrode through the nanocontact printing on a PEN plastic substrate. High-permittivity parylene-C was deposited at the room temperature using an exclusive deposition device to create an organic dielectric on the fabricated gate electrode and the patterned organic dielectric was etched selectively by O_2 plasma. Channel length of 1um was left on the parylene-C organic dielectric so that source and drain metal electrodes could be patterned and fabricated using the nanocontact printing process. On a contact electrode, an organic active semiconductor layer of pentacene was deposited through e-beam deposition device. The nanocontact printing process using SAM and PDMS stamp made it possible to fabricate OTFT arrays with channel lengths minimize to even sub-micron size, and reduced and optimized the procedure by 10 steps compared with photolithography. Since the process was done in room temperature, there was no pattern transformation, retraction, and shrinking problem appeared. Also, it was possible to improve electric field mobility, to decrease contact resistance, and to reduce threshold voltage by using a big dielectric and fabricate nanopatterns.

Keywords: nanocontact printing(nCP), OTFT array, PDMS stamp, SAM, organic semiconductor

1 INTRODUCTION

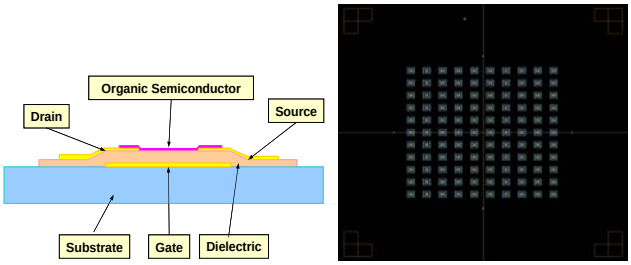
The organic thin film transistors(OTFTs) can be fabricated using a number of different device structures. In general, OTFTs are comprised of four components: gate electrode, gate dielectric, organic active semiconductor layer, and source and drain contacts. OTFTs can be fabricated either with a horizontal device structure, where the electric current flow is perpendicular to the substrate and in which the channel length is defined by lithographic resolution, or with a vertical device structure, where the current flow is perpendicular to the substrate and in which the channel length is determined by film thickness[1]. As an OTFT is expected to be applied frequently to a driving device of active organic EL, a plastic chip for inventory tags and smart cards, it is currently under investigation in the world's most prominent companies, research institutes, universities, and so on [2]. While an OTFT is characterized by low charge mobility as an organic semiconductor and thus cannot be applied to a device which needs high speed, it can be useful when it is necessary to fabrication a device on a large area, when low process temperature is necessary, when bendability is necessary, or particularly when a low-cost process is necessary [3, 4]. When fabricating OTFT arrays on flexible substrate, substrates warpage, surface roughness, and layer-by-layer registration methods should be considered, and the several problems such as optical characteristics deterioration caused by exceeding the maximum process temperature, incoherent pattern arrangement by shrinkage and transformation, and loosening of the adhesion between organic and inorganic materials should be solved to improve the performance [5]. New technologies including inkjet printing, screen printing, and nanocontact printing are being used to fabrication an OTFT [6].

This study is design and fabrication an OTFT array which can be fabricated through a nanocontact printing and a low-temperature process and will be used as a switching device of an organic light emitting diode(OLED). The gate, source, and drain electrode patterns of OTFT were fabricated by nanocontact printing process which is high-resolution lithography technology using polydimethylsiloxane (PDMS) stamp. The OTFT array with dielectric layer and organic active semiconductor layers formed at room temperature or at a temperature lower than 40℃. During the OTFT fabricating process, in order to keep the flatness, we used dry film photoresist(DFR) as adhesion layer and glass substrate as rigid layer adhered to PEN layer [7, 8].

For a design in pursuit of efficiency improvement and commercialization of an OTFT, it is necessary to investigate high heat resistance, high coplanarity and high optical transmittance technology, and large-area substrate design and to develop new materials on source/drain, gate electrodes, insulators, organic semiconductor layer, plastic substrates, and so on; also necessary is a manufacturing method considering On/Off ratio, mobility, etc. It can be applied as key technology for plastic electronics plastic-based thin film display which is next-generation display-based technology with plastic as a substrate, for ultra-thin film information storage, and for high-volume thin film batteries, and will be the motive power in developing flexible information display in other forms, such as E-paper, wearable computer, and foldable PC.

2 DESIGN AND FABRICATION PROCESS

The gate, source, and drain electrode patterns of OTFT were fabricated through the nanocontact printing process using as a mask PDMS stamp on which an SAM used as an etching mask was applied selectively. As high-resolution and large-area OTFT arrays could be fabricated by using the nanocontact printing process. Since the fabrication process was done in low temperature, there was no pattern transformation, retraction, and shrinking problem appeared. The mask size is 5 x 5 x 0.9 inch, and the channel length is 10um where the line width and the pattern space are different. Figure 1 shows the mask for conducting a patterning experiment on 110 pattern zones on a 4 inch silicon wafer, and a device structures were designed and manufactured only on the 2.5 x 2.5mm zone located respectively.



(a) (b)

Figure 1: (a) cross-section of OTFT on flexible substrate, and (b) geometry of OTFT array designed pattern mask(5" size)

As to the plastic substrates for fabricating OTFT arrays, we used polyethylenenaphthalate(PEN, Teijin Dupont Films) which thickness was 200um, and surface roughness was 0.6nm, coefficient of thermal expansion(CTE) was 20ppm/℃ at 200℃, thermal shrinkage was 0.02%(150℃X30min.), and so they had excellent thermal safety characteristics, H_2O permeability was low and O_2 permeability was also low, the chemically resistant characteristics against acid and alkaline was excellent, and Young's Modulus was high, and so they had high strength characteristics. On the PEN substrate, we deposited 10nm of Cr as adhesion layer and 100nm of Au as etching layer using e-beam deposition device maintained below 50℃ inside the chamber, and inked hexadecanethiols(HDT) SAM solution up to PDMS stamp, transferred into PEN substrates through registration contact printing, and formed single layers. Also selectively etched Au using TFA/GE-8148 solution and formed conductive gate electrode. Parylene-C was used as organic insulation film. Parylene-C is a primary dielectric, exhibiting a very low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency. Parylene-C of which dielectric strength is 5600(DC volts/mil short time), sheet resistance is 1014 (Ω, 23℃, 50%), and dielectric constant is 3.15(60Hz), has the excellent conductive characteristics.

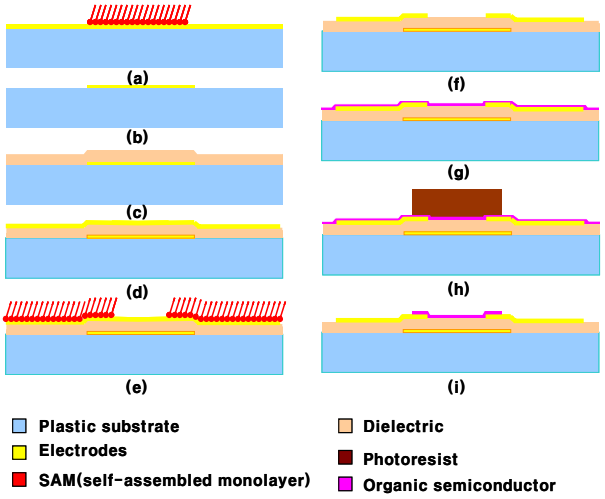


Figure 2: Fabrication process of OTFT using nCP (a) Inked SAM solution on Au deposited plastic substrate, (b) fabricated gate electrode, (c) deposited and patterned dielectric, (d) Au deposition, (e) Inked SAM solution for contact electrodes, (f) fabricated source and drain electrode, (g) deposited organic semiconductor, (h) patterned organic semiconductor, and (i) fabricated organic semiconductor

On the fabricated gate electrode, we deposited parylene-C with high permittivity at room temperature using deposition device and formed organic dielectric, and then coated with positive photoresist in 1um thickness under the condition of maintaining OFPR at 3000RPM for 20 seconds and prebaked at 90℃ for 30minutes. Then carried out lithography process using gate mask and developed with NMD solution for 80 seconds. Selectively etched patterned organic insulation film using O_2 plasma at 130W of RF power for 10 minutes. And photoresist removed in MS2001 solution at 70℃ for 8minutes. On the Parylene-C organic insulation film, we made 1um of channel length and carried

out patterning of source and drain metal electrodes through nanocontact printing process, inked HDT SAM solution up to PDMS stamp transferred into PEN substrates through registration contact printing, and formed electrodes. On the source and drain metal electrodes, we deposited 10nm of Cr as adhesion layer and 100nm of Au as etching layer. And on the contact electrodes, we deposited 100nm of pentacene as organic active semiconductor layer using e-beam deposition method. On the pentacene organic semiconductor, we formed passivation layer by depositing 1um of Parylene. Then coated with positive photoresist in 3um thickness under the condition of maintaining AZ5214 at 3000RPM for 20 seconds and prebaked at 90℃ for 30minutes. And carried out patterning through lithography process using pentacene mask and fabricated organic semiconductor by means of eliminating unnecessary parts using O_2 plasma. Figure 2 show fabrication process of OTFT by using nanocontact printing.

3 EXPERIMENT AND RESULTS

To fabricate OTFT, Au/Cr thin films were deposited on a PEN plastic substrate at a temperature lower than 50℃ inside a chamber and a conductive gate electrode was created through the nanocontact printing process. The parylene-C was deposited on the fabricated gate electrode to create an organic dielectric and the patterned organic dielectric was etched by oxygen plasma. The Source and drain metal electrodes were patterned and fabricated on a parylene organic dielectric using nanocontact printing process. The pentacene which is an organic active semiconductor layer was deposited on a contact electrode through a room temperature. Figure 3 show deposition process of Parylene-C dielectric at room temperature. During the OTFT fabricating process, in order to keep the flatness, we used dry film photoresist(DFR) as adhesion layer and glass substrate as rigid layer adhered to PEN layer. Then put the glass substrate on the hot plate maintained at 60℃, cut the DFR film in proper size, and adhered closely flattening out using roller and then, adhered PEN film to the glass substrate without passivation layer on the hot plate. When fabricating OTFT through nanocontact printing process, since there was no need for photolithography device, photoresist and photo process, we could reduce the procedure by 10 steps or more.

The SAM-treated OTFT was more efficient than non-SAM-treated one in terms of drain current. Such higher efficiency was due to the increase in the molecular structure of the pentacene films and strong coherence among SAM molecules, resulting from the change from hydrophilic surface to hydrophobic one and the increased interactions with hydrophobic pentacene molecules. An exclusive device was used to enable room temperature process of conductive electrode, insulator, and organic semiconductor layers, so that it was possible to minimize CTE caused by shrinkage and extension due to temperature of a plastic substrate and to provide better alignment in the patterning process. Besides, since there was no substrate deformation, it was possible to prevent optical property degradation. Parylene-C was used as a gate insulator to reduce threshold voltage. An OTFT array was fabricated through the nanocontact printing process using SAM and PDMS stamp to prevent a leakage current from lowering the efficiency of a device and reduce degradation and to enable micropattern fabrication of OTFT. Figure 4 shows the results of the OTFT fabrication using nanocontact printing process and low-temperature process.

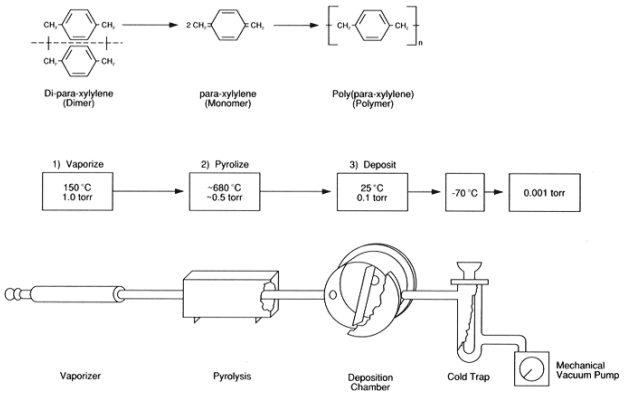


Figure 3: Deposition concept and process of Parylene-C dielectric at room temperature

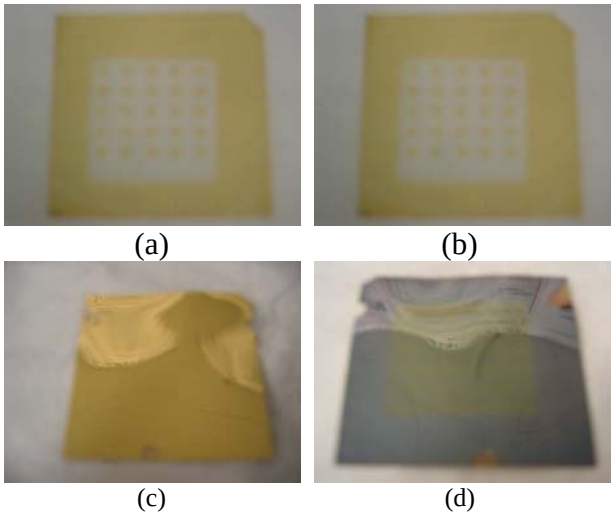


Figure 4: Results of OTFT fabrication: (a) patterned dielectric and gate electrode on PEN substrate, (b) patterned source/drain electrode as the dielectric, (c) Au/Cr deposited on PEN substrate, and (d) deposited organic semiconductor.

4 CONCLUSIONS

This study fabricated an OTFT array with insulator, electrode, and organic active semiconductor layer formed at room temperature or at a temperature lower than 50℃. The high resolution and large-area OTFT array could be fabricated and an OTFT whose substrate and pattern size was never deformed could be fabricated using a room temperature process. Also, the nanocontact printing process made it possible to fabricate OTFT arrays with channel length down to even sub-micron size, and reduced the procedure by 10 steps compared with photolithography. The flexible OTFT array was fabricated through the nanocontact printing and room temperature processes, so that it was possible to increase close packing of molecules by SAM, to improve electric field mobility, to decrease contact resistance, and to reduce threshold voltage by using a big dielectric.

ACKNOWLEDGMENT

This Research was supported by a grant(M102KN01001) from Center for Nanoscale Mechatronics & Manufacturing, one of the 21st Century Frontier Research Programs, which are supported by Ministry of Science and Technology, Korea.

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