Recent Upgrades and Applications of UFDG

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ABSTRACT

Recent upgrades and applications of UFDG, a process/physics-based compact model for nonclassical MOSFETs having ultra-thin silicon bodies (UTBs), are overviewed. The overviews are focused on use of UFDG to aid the optimal design of nanoscale double-gate (DG) CMOS.

Keywords: Compact model, predictive device/circuit simulation, FinFET, MIGFET, nonclassical CMOS.

1. INTRODUCTION

Interest in nonclassical DG CMOS, especially with nanoscale FinFETs [1], is growing as classical CMOS is approaching its scaling limit. Optimal design of nanoscale DG CMOS, at the device as well as the circuit levels, requires a reliable, physical compact model for the DG MOSFET, and we have been developing one (UFDG [2]-[4]) for the past few years. In this paper, we overview recent UFDG upgrades by describing nonclassical device applications for which they are needed.

2. UFDG

The UFDG model [2]-[4] is process/physics-based for the generic DG device structure shown in Fig. 1, which covers the single-gate (SG) FD/SOI MOSFET as well as the DG FinFET. For the latter application, consider Fig. 1 a cross-sectional view of the FinFET from the top, with UTB thickness $t_{Si} = w_{Si}$, the fin width, and $\Phi_{Gf} = \Phi_{Gb} = \Phi_G$, the gate work function. The FinFET width is the fin height h_{Si}.

The UFDG model is physically based on the electric potential and the inversion charge in the UTB/channel. To allow truly physical modeling of the intrinsic MOSFET, the formalisms for weak ($V_{GS} < V_{TW}$) and strong ($V_{GS} > V_{TS}$) inversion are separated, with moderate-inversion channel current and terminal charges, and their voltage-derivatives, being continuously defined by spline polynomial functions of gate voltage. The short-channel effects (SCEs) are accounted for mainly in the weak-inversion modeling, in which the 2-D Poisson equation in the rectangular UTB/channel region (L_{eff} x t_{Si} in Fig. 1) is solved. The current, assumed to be predominantly diffusion, is characterized by integrating the inversion-carrier charge density over (in x) the UTB/channel and defining the effective channel length for diffusion ($<L_{eff}$) based on the derived potential. The modeling effectively accounts for source/drain (depletion and inversion) charge sharing and DIBL (over the entire UTB) in the subthreshold region, including moderate inversion via the mentioned spline functions. For strong inversion, the 2-D effects are less severe but the quantization (QM) effects are quite significant, and dependent on t_{Si} (structural confinement) as well as the transverse electric field $\mathcal{E}_x$ (electrical confinement). Thus, an iterative, self-consistent solution, dependent on arbitrary front- (V_{GfS}) and back-gate (V_{GbS}) biases, of the 1-D (in x) Schrödinger and Poisson equations in the UTB/channel (with distributed inversion-carrier charge, i.e., bulk inversion [5]) of the generic DG MOSFET is derived [2]. The iteration loop is closed by the characterization of the integrated (over t_{Si}) inversion charge density (Q_i), which defines the predominant drift (and diffusion) current, in all the significant (we assume the first four) quantized-energy subbands using the 2-D (energy-independent) density of states and Fermi-Dirac statistics. In part then, UFDG is a compact Poisson-Schrödinger solver for generic DG MOSFETs.

UFDG is charge-based (for transient and AC simulations), with the five (V_{iS}-dependent, i = Gf, Gb, D, B) terminal charges (the body, which typically floats, is the fifth terminal) defined by properly integrating charge components, physically linked to the channel-current modeling, over the intrinsic device, and appropriately adding parasitic components. Thus, all transcapacitances are properly modeled, as reflected in the network representation of UFDG shown in Fig. 2.

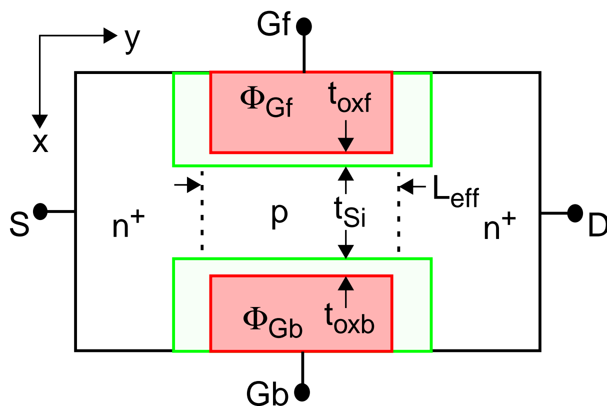


Fig. 1. Generic DG (n)MOSFET structure. The effective channel length L_{eff}, and its relation to the gate length L_g, depend on the lateral doping-density profile $N_{SD}(y)$ in the source/drain extension.

3. INDEPENDENT-GATE FINFETs

Recently, fabrication of independent-gate FinFETs, e.g., the MIGFET [6], with desirable characteristics such as dynamic threshold-voltage (V_t) control, have been reported. Such novel devices could relax requirements for Φ_G

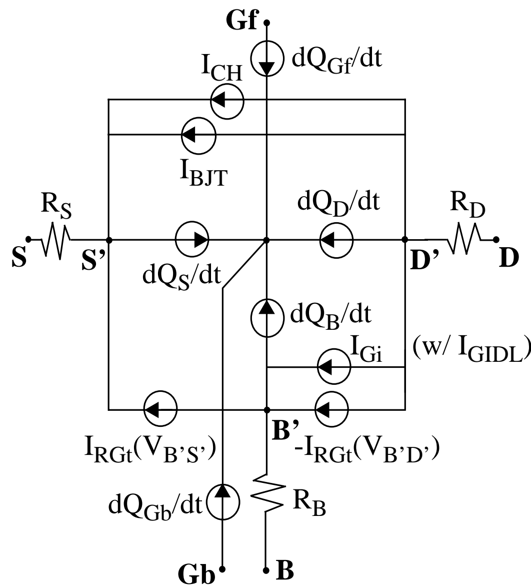


Fig. 2. Network representation of the UFDG model.

engineering for V_t control, and enable nonclassical CMOS integrated circuits to be optimally designed with variable-V_t devices. For simulation of such devices, general modeling of the Gf-Gb charge coupling is needed, and UFDG does that via the noted iterative Poisson-Schrödinger solver for the UTB/channel. Further, we have upgraded UFDG with a new "2-D" spline formalism in terms of both V_{GfS} and V_{GbS} [7]. The formalism, illustrated in Fig. 3, utilizes V_{GfS}-V_{GbS} contours that physically define the moderate-inversion region in terms of the integrated inversion-carrier density ($N_{invW} < N_{inv} \equiv |Q_i|/q < N_{invS}$). When a V_{GfS}-V_{GbS} bias point passed into the model routine lies in the moderate-inversion region, the channel-current and terminal-charge solutions are characterized by 2-D cubic-polynomial spline functions, of V_{GfS} and V_{GbS}, along a 45° line in the moderate-inversion region as shown in the figure, with

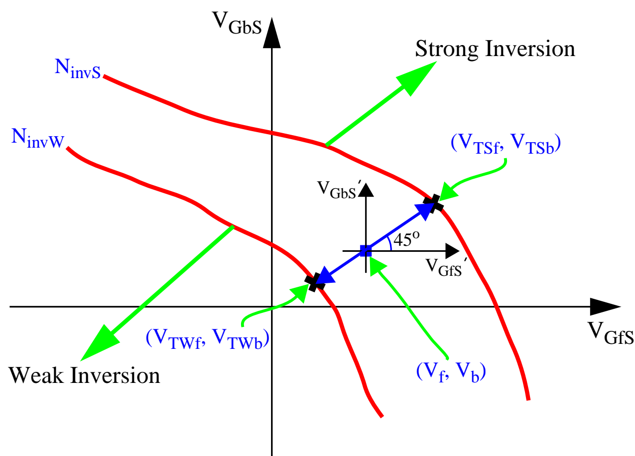


Fig. 3. Mechanics of the 2-D spline. For a specific moderate-inversion bias point (V_f, V_b), the V_{GfS}-V_{GbS} origin is first shifted to (V_f, V_b) as shown, and then VTW and VTS are determined as the intercepts of the 45° line from the new origin on the N_{invW} and N_{invS} contours, respectively.

coefficients defined by the solutions at the intercepted weak- and strong-inversion boundaries, (V_{TWf}, V_{TWb}) and (V_{TSf}, V_{TSb}), respectively. The result is a model that is numerically stable irrespective of device asymmetry and arbitrary V_{GfS} and V_{GbS} (which was not generally the case with our former 1-D spline function of V_{GfS}).

The UFDG-predicted current-voltage (I_{DS}-V_{GfS}) characteristics of an L_g = 80nm n-channel MIGFET [8] in Fig. 4, which are in good accord with measured characteristics, exemplify the utility of the 2-D spline. The Gf-Gb charge coupling, which, with the SCEs and QM effects, defines the subthreshold slope as well as the V_t dependences on V_{GbS}, is predicted well with good numerical stability. The predicted characteristics of the device in the DG mode (V_{GbS} = V_{GfS}) are included in the figure for comparison.

Further demonstration of the 2-D spline utility, and of that of the MIGFET, is provided by the application to a compact low-power single-transistor RF mixer illustrated in Fig. 5. Transient and Fourier simulations of the mixer were done with UFDG/Spice3 [8], with f_{RF} = 1.8GHz and f_{LO} = 1.6GHz. Interestingly, these predicted mixer characteristics, which followed from physics/process-based UFDG model parameters defined with limited knowledge of the MIGFET processing, are in very good agreement with characteristics of the fabricated MIGFET mixer.

Another possibly useful application of the MIGFET is in the 6T-SRAM cell, the scalability of which is highly dubious in classical CMOS technology. FinFET CMOS will enable scalability, but since the DG-FinFET effective width is "digital," defined by h_{Si} and the number of paralleled fins, the SRAM performance-versus-layout area tradeoff, defined by the relative strengths of the constituent transistors, tends to be undermined. Replacing the access FinFETs by SG

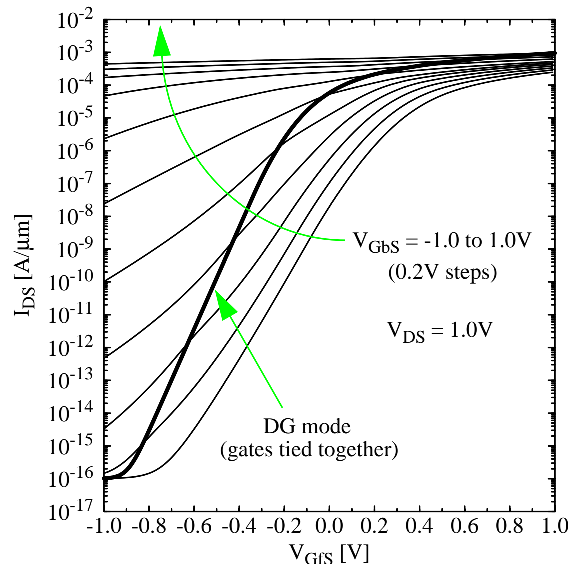


Fig. 4. UFDG-predicted current-voltage characteristics (per h_{Si}) of an L_g=80nm n-channel MIGFET for varying back-gate bias; w_{Si}=25nm, t_{oxf}=t_{oxb}=2.0nm. The predicted DG-mode characteristic is included.

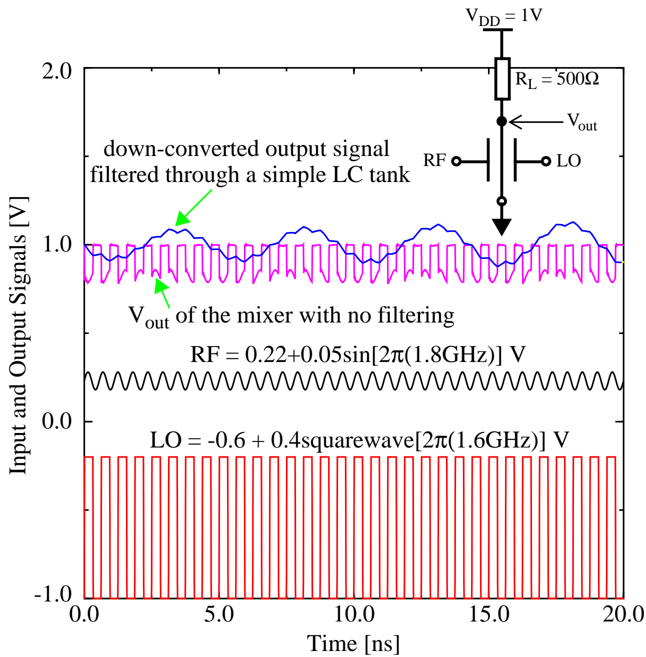


Fig. 5. UFDG/Spice3-predicted frequency-modulated transient output signal of the simple, single-MIGFET mixer depicted in the inset. The down-converted output signal (with IF = f_{RF} - f_{LO}) filtered through a simple LC tank is also shown, as well as the RF and LO input signals.

MIGFETs [9], with, for example, V_t controlled by optimal Gb bias, can possibly improve the tradeoff and yield good nanoscale SRAM performance, as reflected by the UFDG/ Spice3-predicted butterfly curves and read-static noise margins (SNMs) in Fig. 6. Additional simulations show how

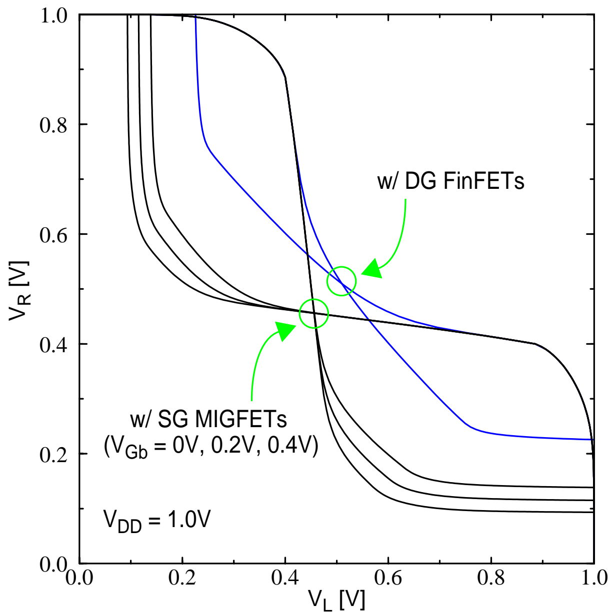


Fig. 6. UFDG/Spice3-predicted SRAM butterfly curves for an L_g =28nm FinFET-based SRAM cell with MIGFETs used as the access transistors, compared with that for the cell with all FinFETs. For the latter, SNM=140mV; with the MIGFETs, SNM =281mV, 261mV, and 237mV for V_{Gb} increasing from 0 to 0.4V.

the write-0 margin decreases with decreasing V_{Gb}, and hence must be traded off with SNM via optimization of the MIGFET back-gate bias.

4. GATE-SOURCE/DRAIN UNDERLAP

For nanoscale nonclassical MOSFETs, which must use undoped UTBs [7], gate-source/drain (G-S/D) underlap, in contrast to the common overlap in classical devices, is essential [10]. The underlap, which is defined by the lateral doping-density profile $N_{SD}(y)$ in the thin S/D extension, necessitates more UFDG upgrades. First, it defines a V_{GS}-dependent effective channel length L_{eff} that is longer than L_g, especially for weak inversion; it approaches L_g for strong inversion [10]. The $L_{eff}(V_{GS})$ modeling in UFDG is facilitated by the noted use of splines for moderate inversion. For weak inversion, $L_{eff} = L_g + L_{eS} + L_{eD}$, where (for V_{DS} = 0) $L_{eS/D}$ is defined by $N_{SD}(y)$ as indicated in Fig. 7. For strong inversion, we can assume $L_{eff} \cong L_g$. Second, the longer L_{eff} in weak inversion modifies the noted 2-D Poisson-equation solution, since part of the $L_{eff} \times t_{Si}$ region is ungated, which in fact ameliorates the SCEs as shown in Fig. 8(a). This modification is accounted for in UFDG by reducing the effective S/D-junction potential barrier defined by $N_{SD}(y)$ [11], modeling that is verified by Medici [12] simulations as exemplified in Fig. 8(a). Third, the underlap redefines, i.e., reduces, the G-S/D parasitic capacitance $C_{GS/D}$. This capacitance, which comprises inner and outer components due to electric-field fringing, is quite important in nanoscale nonclassical devices (having negligible effective body capacitance), as indicated in Fig. 8(b), since it does not scale with the intrinsic gate capacitance. It is modeled [13] in UFDG, with important V_{GS} dependences of $L_{eS/D}$, by using classical solutions of Laplace's equation in the vicinity of two conducting plates at a device structure-defined angle. Medici-based verification of the modeling is exemplified in Fig. 8(b). (High-V_{DS} dependences of $L_{eS/D}$, which affect $C_{GS/D}$, as well as S/D series resistance $R_{S/D}$ as

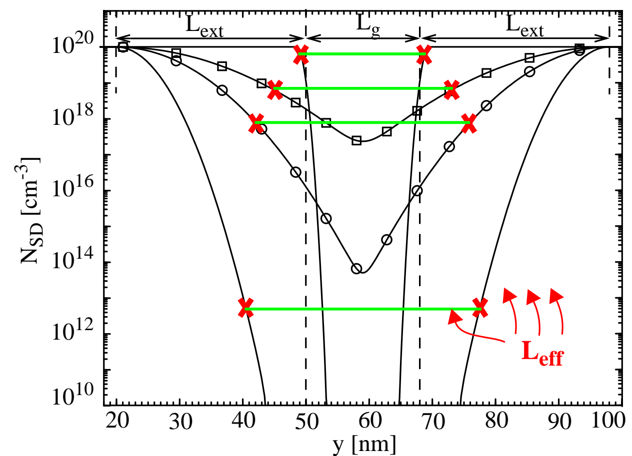
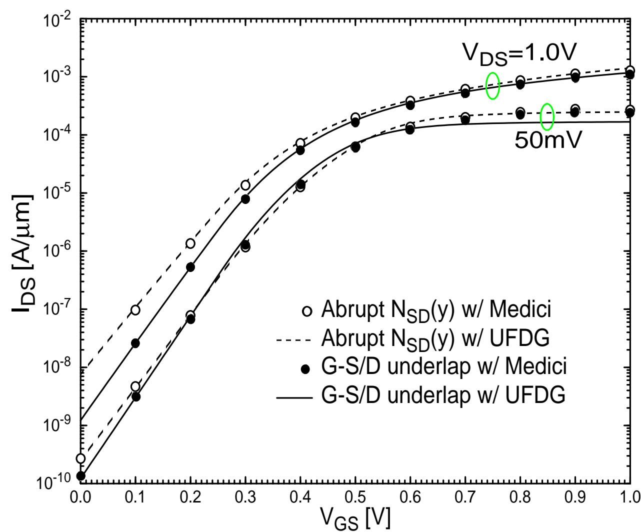
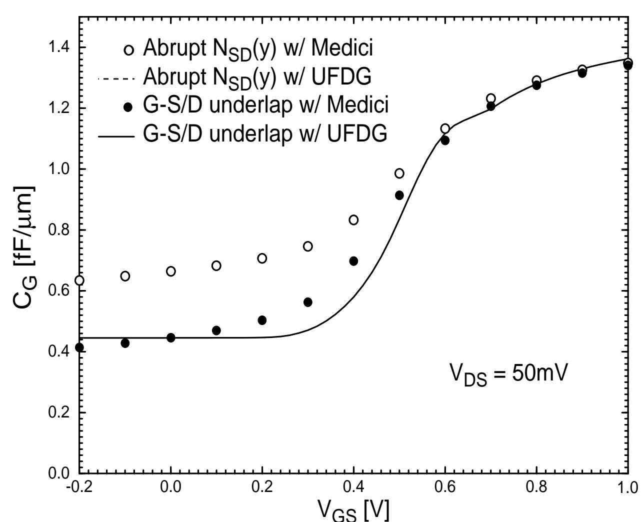


Fig. 7. UFDG-defined weak-inversion effective channel length of an undoped L_g=18nm DG FinFET for the different lateral doping-density profiles in the S/D fin-extension (of length L_{ext}) shown; V_{DS}=0. Note that for the abrupt, unrealistic $N_{SD}(y)$, $L_{eff} \cong L_g$.



(a)



(b)

Fig. 8. UFDG- and Medici-predicted (a) current-voltage and (b) gate capacitance-voltage characteristics (per h_{Si}) for undoped L_g=18nm DG nFinFETs, with ($L_{eS/D}$=3.4nm) and without (abrupt $N_{SD}(y)$) near-optimal underlap; w_{Si}=9nm, t_{ox}=1.0nm, midgap gate (Φ_G=4.6V) with height t_g=18nm. High-V_{DS} dependences of $L_{eS/D}$ and $R_{S/D}$ were neglected in (a).

implied by the strong-inversion UFDG-Medici discrepancy in Fig. 8(a), are now being modeled for UFDG.)

The G-S/D underlap enables, via an optimal $N_{SD}(y)$, good design tradeoffs of device SCE control (or I_{off}) versus $R_{S/D}$ (or I_{on}), and of CMOS speed versus power (as related to I_{on}, I_{off}, $C_{GS/D}$, and $R_{S/D}$). For CMOS speed projections and optimal-underlap study, we must ensure that the S/D-extension resistance, a significant component of $R_{S/D}$, is correlated properly with L_{eff} and $C_{GS/D}$, all of which depend on $N_{SD}(y)$. This can be done by using a 2-D device simulator (e.g., Medici) in conjunction with UFDG. Then, UFDG/Spice3 simulations can project the overall benefit of the G-S/D underlap in nanoscale FinFET CMOS. For example, the propagation delay predictions from simulations of well-tempered L_g = 18nm DG CMOS ring oscillators in Fig. 9 show a dramatic decrease in the delay afforded by the underlap. These simulation results, with others [13], [14], suggest that DG-FinFET CMOS can be designed pragmatically with optimal G-S/D underlap to yield outstanding performance for L_g scaled to less than 10nm. They also reflect the need for reliable modeling of FinFET parasitics, i.e., $C_{GS/D}$ and $R_{S/D}$, and their bias dependences.

5. NANOSCALE FINFETs

With L_g scaled toward 10nm and below, the FinFET UTB must be thinned to less than 10nm as well [15]. Carrier transport in such thin, short silicon channels is much different than that in classical MOSFETs. The strong-inversion carrier transport in UFDG is modeled appropriately as quasi-ballistic via a carrier-temperature accounting for velocity overshoot derived from the Boltzmann transport equation and its moments [16]. The mobility model has been upgraded [17], and the ballistic-limit current, defined by the thermal injection velocity at the source, has been implemented [7].

The new mobility model, which is based on the noted QM formalism in UFDG, accounts for Coulomb, phonon, and surface-roughness scatterings, with dependences on the (undoped) UTB thickness (t_{Si}), transverse electric field ($\mathcal{E}_{x(eff)}$), and silicon-surface orientation stemming from its connection to the eigenvalues (quantized subband energies) and eigenfunctions (wave functions) defined by the QM model. The model is quasi-predictive, having only two physics-based parameters: μ_0, the low-$\mathcal{E}_{x(eff)}$ mobility in a thick-t_{Si} version of the modeled device, and θ, a tuning factor to account for uncertainty in the magnitude of the

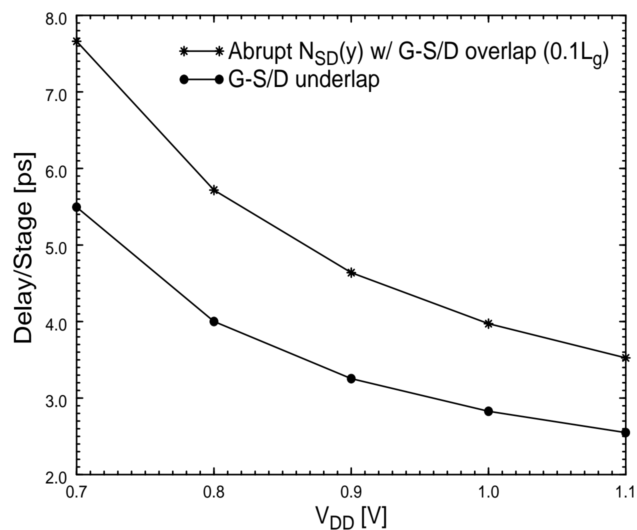


Fig. 9. UFDG/Spice3-predicted propagation delays versus supply voltage of unloaded 9-stage L_g=18nm DG-FinFET CMOS ring oscillators, with ($L_{eS/D}$=3.4nm) and without (w/ overlap) near-optimal G-S/D underlap; w_{Si}=9nm, t_{ox}=1nm, midgap gate, t_g=18nm. For the underlap devices, $R_{S/D}$ includes a fin-extension component defined by $N_{SD}(y)$.

surface roughness. With regard to the latter, the model assumes typical surface-roughness parameters, for which $\theta = 1$; smaller values of θ correspond to smoother surfaces. Further, the QM formalism enables variations in the pertinent effective masses when they (e.g., hole masses at {110} Si surfaces} are not well known.

Figure 10 exemplifies the verification of the mobility model via measurements of electron and hole effective mobilities versus N_{inv} in planar {100}-surface DG (and SG FD/SOI) undoped-UTB MOSFETs. Note the inferred, fixed values of μ_0 and θ for electrons and holes, respectively, which reflects the physical basis of the model. For comparison, we include in Fig. 10 the universal carrier

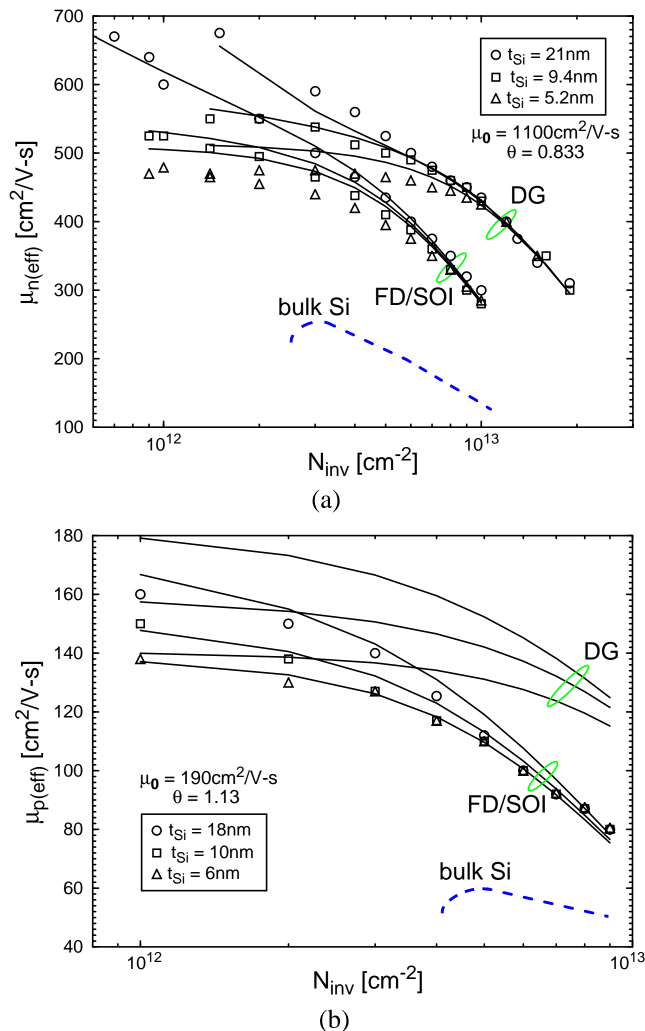


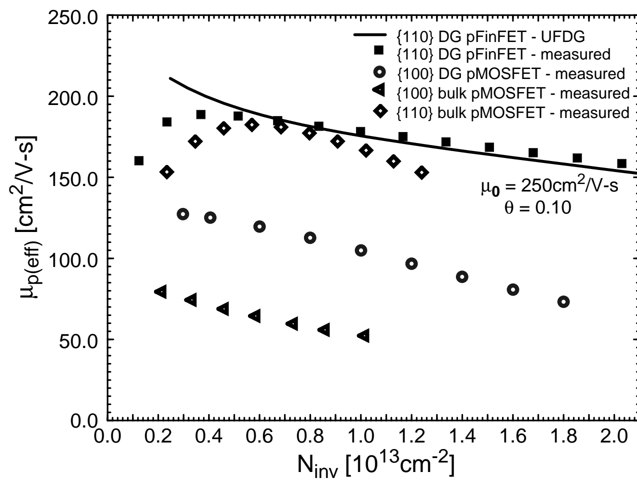
Fig. 10. Calibrated UFDG mobility-model predictions (solid curves with μ_0 and θ given), versus integrated inversion-carrier density, of (a) effective electron mobility in planar SG FD/SOI and DG undoped nMOSFETs on {100} Si with various t_{Si}, compared with experimental data (symbols) from [18], and (b) effective hole mobility in planar SG FD/SOI and DG undoped pMOSFETs on {100} Si with various t_{Si}, the former compared with experimental data (symbols) from [19]. For comparison, the universal electron and hole $\mu_{eff}(N_{inv})$ [20] (dashed curves) in bulk MOSFETs on {100} silicon with uniform channel doping of 10^{18}cm^{-3} is superimposed in (a) and (b), respectively.

mobilities in {100}-surface (unstrained) bulk-silicon MOSFETs with contemporary-like channel doping of 10^{18}cm^{-3}. Note that at $N_{inv} = 10^{13}$cm^{-2} (which typifies the on-state), the mobilities in the undoped-UTB MOSFETs are dramatically higher (3.3x for electrons and 2.4x for holes) than those in the bulk-silicon counterparts. For DG nMOSFETs with {110} surfaces, e.g., common nFinFETs, the $\mu_{n(eff)}$ superiority is less, but still ≅2x as implied by the model-predicted ratio of $\mu_{n(eff)}$ in {110}- and {100}-surface DG nMOSFETs [7]. For DG pMOSFETs with {110} surfaces, e.g., common pFinFETs, the $\mu_{p(eff)}$ superiority is expected to be substantially more (≅3x) than the noted 2.4x [21]. We note that μ_{eff} in DG MOSFETs is also higher than that in bulk counterparts with strained-silicon channels [22]. Further, note in Fig. 10 that μ_{eff} in DG (and SG FD/SOI) MOSFETs at high N_{inv} is virtually independent of t_{Si}, which means that, unlike μ_{eff} in classical (i.e., SG bulk-Si and PD/SOI) CMOS, μ_{eff} in DG CMOS will remain high for all future technology nodes as t_{Si} is scaled with L_g. These results then suggest that undoped DG CMOS will not need strained-silicon channels, which are essential today for continued development of classical CMOS [22].

We have corroborated the high mobilities in Fig. 10, and gained interesting insights, by calibrating UFDG to contemporary FinFETs having {110} fin-sidewall surfaces [23]. The number of model parameters in UFDG is relatively low, and the key parameters relate directly to device structure or physics. The parameter values are thus known, or can be reasonably estimated for initial guesses in the calibration process. Results are exemplified in Fig. 11 which shows effective hole mobility in DG pFinFETs with $t_{Si} \cong 30$nm, fabricated [24] at Freescale Semiconductor with a TiN gate and SiON dielectric, and effective electron mobility in DG nFinFETs with $t_{Si} \cong 26$nm, fabricated [1] at AMD with an n^+ polysilicon gate and SiON dielectric. Measured mobilities in planar-{100} DG MOSFETs and bulk-silicon counterparts are included for comparison. The results are in accord with Fig. 10, but the calibrations give interesting insights regarding carrier transport in undoped UTBs [23]. For example, we infer from the low derived values of θ, and the noted comparisons, unusually smooth {110} fin-sidewall surfaces (which could be due in part to the SiON dielectric). Also, with the high carrier mobilities, due to the smooth surfaces as well as low $\mathcal{E}_{x(eff)}$ in undoped UTBs, we project via UFDG simulations ballistic-like drive currents, limited by the maximum thermal injection velocity at the source, in n- and p-channel DG FinFETs with $L_g <\cong 20$nm.

6. SUMMARY

Our generic process/quantum-based compact model (UFDG) for DG MOSFETs has been reviewed, and recent upgrades needed for particular nonclassical-device applications have been overviewed. General modeling of the Gf-Gb charge coupling and a novel 2-D spline were noted for MIGFET applications, including an RF mixer and the 6T-



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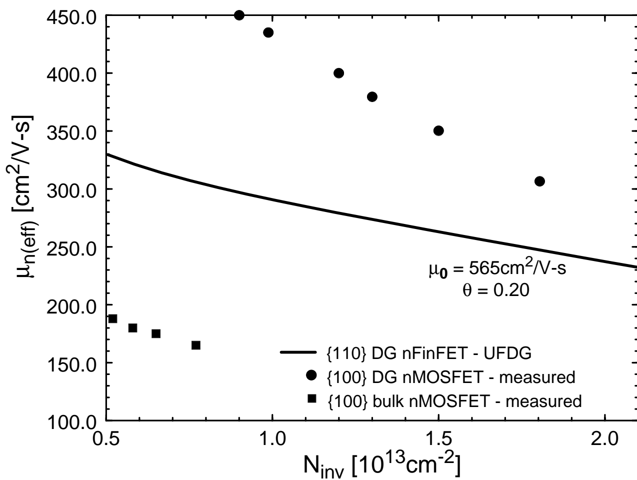

(b)

Fig. 11. UFDG-predicted effective hole (a) and electron (b) mobilities (curves with μ_0 and θ given) versus integrated inversion-carrier density derived from calibrations to pFinFETs [24] and nFinFETs [1]. The directly measured mobility for the {110}-surface pFinFET is also shown in (a), as well as those for a planar-{100} DG pMOSFET (t_{Si} = 18nm), based on [19], a contempory-like {100} bulk-Si pMOSFET ($N_D = 6.6 \times 10^{17} cm^{-3}$) [25], and an uncommon {110} bulk-Si pMOSFET *with low channel doping density* [21]. Superimposed in (b) are measured mobilities of a planar-{100} DG nMOSFET (t_{Si}=21nm) [18] and a contemporary-like bulk-Si nMOSFET ($N_A = 2.4 \times 10^{18} cm^{-3}$) [25].

SRAM cell. Bias-dependent L_{eff}, expanded SCE modeling, and parasitic fringe-capacitance modeling were noted for nonclassical devices with undoped UTB and G-S/D underlap, and benefits of the underlap in optimal nanoscale CMOS design were discussed. And for nanoscale FinFETs with undoped UTBs, new QM-based mobility modeling was noted, which, with calibrations of UFDG to recently fabricated FinFETs, revealed very high hole and electron mobilities relative to those in contemporary bulk-silicon counterparts, high enough to yield ballistic-limit currents for gate lengths less than about 20nm.

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