Compact Model for Short Channel Effects in Source/Drain Engineered Nanoscale Double Gate (DG) SOI MOSFETs

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ABSTRACT

In present paper, we propose an analytical model for short channel effects in nanoscale source/drain extension region engineered double gate (DG) SOI MOSFETs analyzing the impact of (i) lateral source/drain doping gradient, (ii) spacer width, (iii) spacer to doping gradient ratio, (iv) silicon film thickness and (v) high-κ gate dielectrics on short channel effects. The results of the analytical model confirm well with simulated data over the entire range of spacer widths, doping gradients and effective channel lengths. The optimal design guidelines are proposed for engineering the source/drain extension regions for 25 nm DG MOSFETs.

Keywords: Double Gate SOI MOSFET, Source/Drain Engineering, Compact Modeling, Short channel effects.

1 INTRODUCTION

The double gate (DG) silicon-on-insulator (SOI) MOSFET has received great attention in recent years owing to the inherent suppression of short channel effects (SCEs), improved drive current (I_{ds}) and transconductance (g_m) [1-3]. A strong demand to lower threshold voltage (V_{th}) to improve the on-current for high-speed operation, leads to an increase in off-current, which in turn leads to a catastrophic increase in stand-by power consumption in integrated circuits designed with nanoscale DG SOI MOSFETs. In nanoscale regimes, I_{off} can be minimized by reducing the silicon film thickness (T_{si}). However, for gate lengths (L_g) below 50 nm, the fabrication of ultra-thin (<< 10 nm) defect free silicon film remains a technological challenge. Moreover, reducing T_{si} introduces a parasitic resistance, which degrades the device performance.

A viable option to minimize SCEs and control I_{off} in a nanoscale DG MOSFET is the optimization of source/drain extension (SDE) regions [4-10]. In this context, it is important to model the SCEs in a SDE region engineered nanoscale DG MOSFET. Most of the previous works on analytical modeling of SCEs in DG devices [11-18] have focused on devices with abrupt SDE regions. In the present work, an analytical model for SCEs in a nanoscale source/drain engineered DG MOSFET (Fig. 1(a)) has been developed analyzing the impact of (i) lateral source/drain doping gradient (d), (ii) spacer width (s) and (iii) spacer to doping gradient ratio (s/d) to suppress SCEs – V_{th} lowering and degradation of subthreshold slope (S-slope). The present work provides valuable design guidelines in the performance of nanoscale source/drain engineered DG devices and serves as a tool to optimize important technological parameters for 65 nm technology node and below.

2 SIMULATION

The devices analyzed here have been simulated using 2D simulator, ATLAS [19]. The doping (N_a) of p-type SOI layer of 10^{21} m^{-3}, gate workfunction of 4.72 eV, gate oxide thickness (T_{ox}) = 1.3 nm and gate length (L_g) = 25 nm corresponding to the High Performance (HP) 65 nm node logic technology [1] was chosen for the devices. The gate dielectric permittivity (ε_κ) was varied from $3.9\varepsilon_o$ to $35\varepsilon_o$, where ε_o is the permittivity of free space. The spacer width (s) was varied from $(0.25)L_g$ to $(1.0)L_g$ for all the devices and source/drain doping profile defined by its gradient (d) at the gate edges, was varied from 1 to 6 nm/decade [8-10], as shown in Fig. 1(b). The simulations have been performed with drift diffusion (DD) model using CVT mobility model with default parameters with equivalent oxide thickness (EOT) in inversion accounting for the gate depletion, finite inversion layer capacitance and physical oxide thickness.

3 MODEL FORMULATION

In order to analytically evaluate SCEs in source/drain engineered DG MOSFETs, we start from the 2D Poisson equation in the weak inversion region, which is given as

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}\left(N_a-N_{SD}e^{\frac{-x^2}{\sigma^2}}-N_{SD}e^{\frac{-(L_g+2s-x)^2}{\sigma^2}}\right) \quad (1)$$

where $\psi(x,y)$ is the 2D potential in the silicon film, N_a is the silicon film doping, N_{SD} is the peak source/drain doping concentration, ε_{si} is the dielectric permittivity of silicon and σ is the parameter governing the roll-off of the Gaussian source/drain doping profile. The exact analytical solution of (1) is mathematically complicated and may not be suitable for implementation in a compact model. Therefore we approximate the impact of SDE regions by introducing the concept of an effective channel length (L_{eff}) as a function of spacer width, doping gradient, effective source/drain doping level and gate length. The proposed expression of L_{eff} is discussed later. Under these assumptions, (1) is approximated as

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}\left(N_a\right) \quad (2)$$

In the present analysis, we use superposition principle [20-21] to solve the 2D Poisson equation (2) for potential distribution in the silicon film. The 2D potential ($\psi(x,y)$) using the superposition principle is split into a long channel solution to 1D Poisson equation ($U(y)$) and a short channel solution to 2D Laplace equation ($V(x,y)$) i.e.

$\psi(x,y) = U(y) + V(x,y)$. The boundary conditions used for the solution of (2) are given as

$$\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=0} = \frac{C_{ox}}{\varepsilon_{si}}\left(\psi(x,y=0) - V'_{gs}\right) \quad (3a)$$

$$\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=t_{si}} = \frac{-C_{ox}}{\varepsilon_{si}}\left(\psi(x,y=T_{si}) - V'_{gs}\right) \quad (3b)$$

$$\psi(x=0,y) = V_{bi} \quad (3c)$$

$$\psi(x=L_{eff},y) = V_{bi} + V_{ds} \quad (3d)$$

where C_{ox} (= ε_{ox}/T_{ox}) is the gate oxide capacitance, ε_{ox} is the dielectric permittivity of oxide, C_{si} (= ε_{si}/T_{si}) is the silicon film capacitance, $V'_{gs} = V_{gs} - V_{fb}$ with V_{gs} and V_{fb} being the gate and flatband voltages, respectively, V_{ds} is the applied drain bias and V_{bi} is the built-in-voltage.

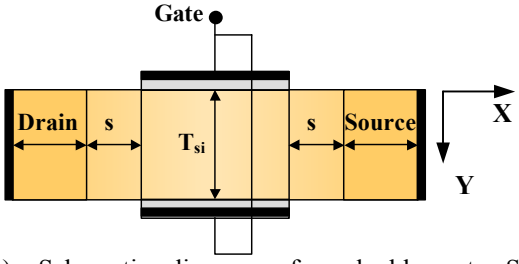

Fig. 1(a): Schematic diagram of a double gate SOI MOSFET.

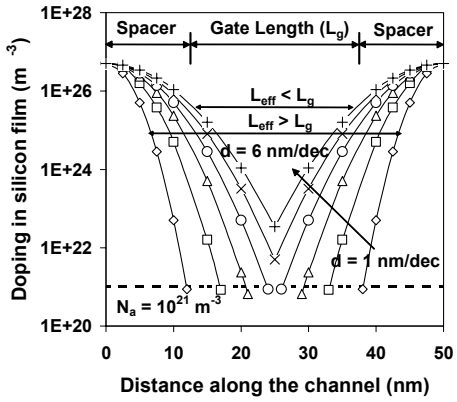

Fig. 1(b) Variation of d along the channel at a fixed spacer of $(0.5)L_g$. L_{eff} has been shown for two cases (i) d = 1 nm/dec, s = $(0.50)L_g$ and (ii) d = 1 nm/dec, s = $(0.50)L_g$.

It is important to note that the boundary condition (3d) has been evaluated at x = L_{eff} instead of L_g, as in the case of devices with abrupt SDE regions. In the present work, L_{eff} has been modeled as

$$L_{eff} = L_g + 2\left(s - \sigma\sqrt{\ln\left(N_{SD}/\eta_{SD}\right)}\right) \quad (4)$$

where η_{SD} = $(2.25\times10^{25}\ln(L_g/s) + 1.5\times10^{25})$, in units of m^{-3}, represents the effective source/drain doping level at which the effective channel length is determined. η_{SD} has been defined as a function of the spacer width to account for the fact that for larger spacer regions, the gate does not control the extension regions effectively. The effect of the doping gradient (d) is accounted for in L_{eff} through the parameter σ. Moreover, from (4) it can be seen that for large source/drain doping gradients (d) and smaller spacer widths (s), the second term in (4) becomes negative, thus implying that L_{eff} is smaller than the physical gate length (L_g) whereas for larger spacers, $L_{eff} > L_g$. The threshold voltage (V_{th}) and subthreshold slope (S-slope) of nanoscale DG MOSFET incorporating the impact of source/drain doping gradient and spacer width, can be obtained similar to the described in [17, 21].

In order to incorporate the effect of high – κ gate dielectrics in the model for SCEs in SDE source/drain engineered DG MOSFETs, we follow the approach of Frank et al. [22] and solve the 2D Poisson equation in the high – κ dielectric, in addition to the silicon film, along with the conditions of continuity of potential and normal component of electric displacement at the boundary of the high – κ dielectric and silicon film, accounting for the 2D effects in the gate oxide. The generalized eigenvalue equation valid for any dielectric material is obtained by incorporating the 2D effects in the oxide, taking into account the actual dielectric constants of different materials that incorporate the lateral 2D effect and is given as [22]

$$\frac{\varepsilon_{si}}{\varepsilon_{\kappa}}\left(\tan\left(\lambda_n T_{ox}\right)\tan\left(\frac{\lambda_n T_{si}}{2}\right)\right) = 1 \quad (5)$$

where ε_{κ} is the permittivity of the gate dielectric. In the present work, we have studied gate dielectric permittivities from $3.9\varepsilon_o$ to $35\varepsilon_o$. These values correspond to SiO_2 ($3.9\varepsilon_o$), Al_2O_3 ($9\varepsilon_o$), HfO_2 and ZrO_2($25\varepsilon_o$), Ta_2O_5 ($25\varepsilon_o$) and La_2O_3 ($30\varepsilon_o$) [24].

4 RESULTS AND DISCUSSION

As shown in Fig. 1(b), a variation of spacer width along with lateral source/drain doping gradient results in the modulation of L_{eff} in a SDE engineered DG MOSFET. Fig. 2 shows the variation of the product $\lambda_1 L_{eff}$ with d. The product $\lambda_1 L_{eff}$ must be greater than 4 to avoid SCEs in a given design [21]. Designing DG MOSFETs with T_{si} of $(0.6)L_g$ (= 15 nm) with abrupt SDE regions results in a $\lambda_1 L_{eff} < 4$ i.e. severe SCEs. However, using certain values of s and d i.e. s = $(0.75)L_g$ with d ≤ 5 and s = $(1.0)L_g$ with d ≤ 7, as shown in the figure, results in $\lambda_1 L_{eff} > 4$, thus minimizing SCEs.

The concept of L_{eff} in SDE engineered DG MOSFETs and its dependence on SCEs through λ_1 can also be understood in terms of the ratio of spacer width to lateral source/drain doping gradient (χ = s/d). Physically, χ represents the number of decades of source/drain doping gradient across the extension regions. As shown in Fig. 3, values of χ that are close to χ_{min} ($\cong$ 1.0) correspond to shorter L_{eff} whereas values near to χ_{max} ($\cong$ 25.0) indicate a larger effective channel length. Thus χ is an important technological parameter along with s and d in the design nanoscale source/drain engineered DG MOSFETs. In order to avoid SCEs in a given structure, L_{eff} should not be less than L_g for any choice of s and d. A careful investigation of L_{eff} for various values of s and d reveals that the above condition can be satisfied if $\chi \geq (0.1)L_g$. A value of χ lower than $(0.1)L_g$ would lead to severe SCEs and higher I_{off} than DG devices with abrupt source/drain regions. In order to achieve the same short channel immunity in DG devices with T_{si} = 15 nm i.e. $(\lambda_1 L_g)_{Tsi=15\ nm} \cong (\lambda_1 L_g)_{Tsi=10\ nm}$, χ must be increased from $(0.10)L_g$ to $(0.18)L_g$. This is because for $\chi = (0.1)L_g$, $(\lambda_1 L_{eff})_{Tsi=15\ nm} = (\lambda_1 L_g)_{Tsi=15\ nm} = 3.53$, which is less than $(\lambda_1 L_g)_{Tsi=10\ nm} = 4.65$). Thus improving SCEs in devices with thicker silicon films requires an increase in L_{eff}

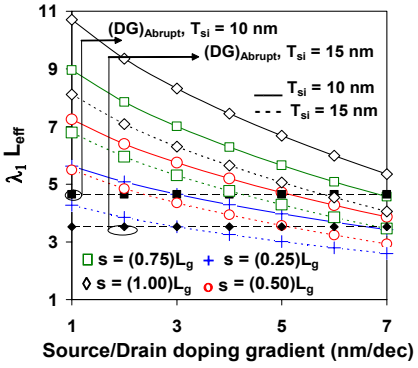

Fig. 2(a): Variation of $\lambda_1 L_{eff}$ with d for various values of T_{si} and s. λ_1 is the first root of the eq (5).

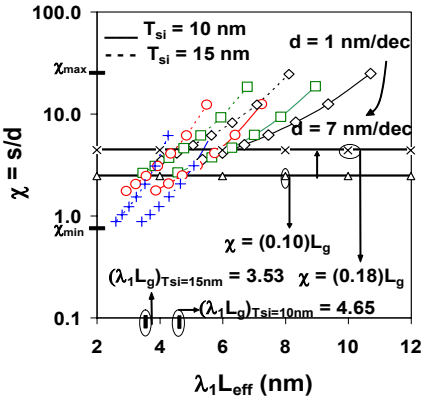

Fig. 3: Variation of χ with $\lambda_1 L_{eff}$ for various values of T_{si}. Symbols are same as in Fig. 2.

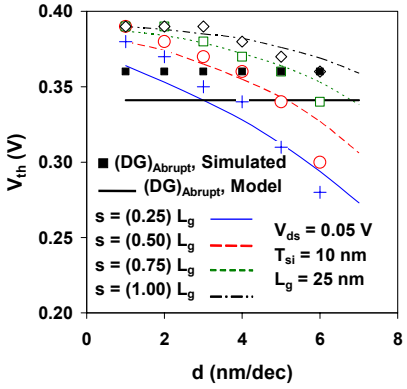

Fig 4(a): Variation of V_{th} with d for various spacer values.

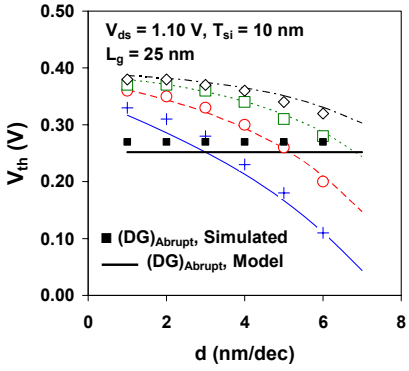

Fig 4(b): Variation of V_{th} with d for various spacer values. Symbols are same as in Fig. 3(a).

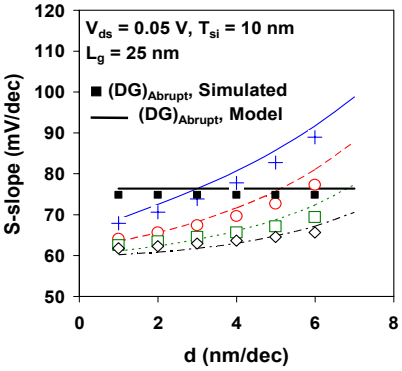

Fig 5(a): Variation of S with d for various s values. Symbols are same as in Fig. 4(a).

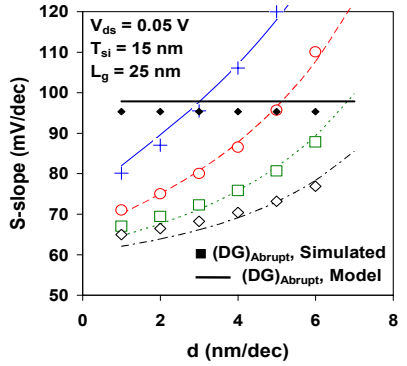

Fig 5(b): Variation of S with d for various s values. Symbols are same as in Fig. 4(a).

by increasing χ i.e. reducing the doping gradient for the same values of spacer width.

Fig. 4–5 show the dependence of V_{th} and S-slope on d for different values of s, T_{si} and V_{ds}. V_{th} was extracted from simulation as the gate bias when the normalized drain current ($I_{ds}/(W_g/L_g)$) reaches 100 nA, where W_g is the gate width (= 1 μm). The results for DG devices designed with abrupt source/drain doping profiles are also shown for comparison. A reasonable agreement of the modeled V_{th} and S with simulated data is obtained for the entire range of spacer widths ($(0.25)L_g$ – $(1.0)L_g$), doping gradients (1 – 6 nm/dec) and effective channel lengths (60 nm – 20 nm), thus showing the validity of the proposed model and more importantly of the simple yet efficient expression for L_{eff} used in the present analysis to accurately model the effect of s and d in nanoscale DG MOSFETs. Engineering SDE regions in nanoscale MOSFETs by optimizing d and s, offers another degree of freedom apart from the important device parameters such as T_{si} and T_{ox} to minimize SCEs. Since the requirement of abrupt source/drain junctions is technologically not possible, the present model is a significant improvement over previous analytical models [11-18] for nanoscale DG MOSFETs, as it includes the effect of source/drain doping gradient and spacer width.

As L_{eff} is a better parameter than L_g to evaluate short channel effects in a given structure, Fig. 6(a)-(b) show the dependence of V_{th} and S-slope on L_{eff} for various values of s and d. Higher doping gradient (for a given spacer width) at the gate edge shortens L_{eff} and results in an increase in SCEs. Simulated data for DG devices with abrupt SDE regions are also shown for comparison with the present generalized model. It should be noted that for DG MOSFET with abrupt source/drain regions, the effective channel length (L_{eff}) is the same as the gate length (L_g). At L_{eff} = 20 nm, some deviation is observed with the simulated data, because of severe SCEs in the structure as $\lambda_1 L_{eff}$ is lower than 4 i.e. T_{si} is not proportionally scaled with respect to L_{eff} and therefore the silicon film thickness must be reduced for a given s and d.

SDE extension region design can also be effectively used to minimize SCEs in devices with high – κ gate dielectrics. The penetration of 2D field through the gate dielectric, which degrades the gate controllability over the channel, results in severe SCEs and increase in I_{off}. We present our initial results for SDE region engineering in devices with high – κ gate dielectrics. The modeled and simulated values of subthreshold slope (S-slope) and threshold voltage (V_{th}) for different values of ε_κ are shown in Table 1. A reasonable agreement is observed in the values of V_{th} and S-slope predicted by our model. This table shows the usefulness of engineering source/drain spacer region in minimizing SCEs in devices with high – κ gate dielectrics. For a fixed doping gradient (d = 5 nm/dec), an S-slope < 80 nm/dec can be achieved with $\varepsilon_\kappa \leq 10\varepsilon_o$ with s = $(0.5)L_g$. Higher values of spacer regions (s > $0.5L_g$) will be necessary to minimize SCEs and reduce I_{off} in DG devices designed with $\varepsilon_\kappa \sim 25\varepsilon_o$.

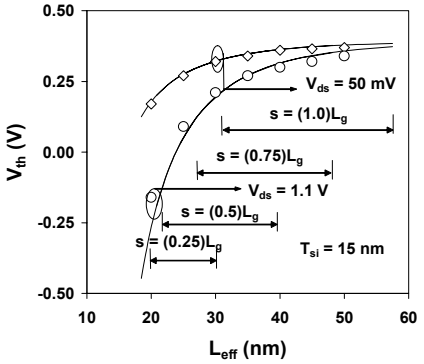

Fig. 6(a): Variation of V_{th} with L_{eff}. Solid lines denote analytical model whereas symbols represent simulation data.

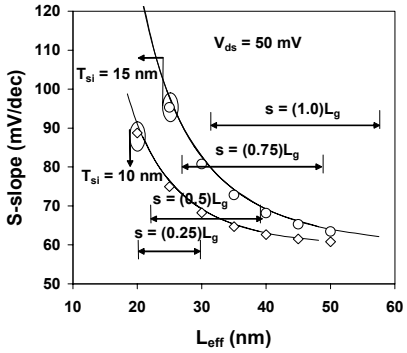

Fig. 6(b): Variation of S-slope with L_{eff}. Solid lines denote analytical model whereas symbols represent simulation data.

5 CONCLUSIONS

In this paper, we proposed an analytical model for short channel effects in nanoscale double gate SOI MOSFETs incorporating the effect of lateral source/drain doping gradient and spacer widths. The results of analytical model confirm well with simulated data over the entire range of spacer widths, doping gradients and effective channel lengths. Results show that optimizing SDE regions offer another degree of freedom in minimizing SCEs in a nanoscale device. The ratio of spacer to doping gradient lying between $(0.10)L_g$ and $(0.18)L_g$ are the optimum values for minimizing SCEs in source/drain engineered DG devices. The present work provides valuable design insights in the performance of nanoscale DG SOI devices with optimal source/drain engineering and serves as a tool to optimize important device and technological parameters for 65 nm technology node and below.

d = 5 (nm/dec)	S-slope (mV/dec) @ V_{ds} = 50 mV, s = (0.50) L_g	
ε_κ ($\times \varepsilon_o$)	Simulated	Model
3.9	65.70	65.67
10	74.44	77.48
25	85.60	90.38
d = 5 (nm/dec)	V_{th} (V) @ V_{ds} = 50 mV, s = (0.50) L_g	
ε_κ ($\times \varepsilon_o$)	Simulated	Model
3.9	0.331	0.343
10	0.326	0.338
25	0.292	0.298

Table 1: Modeled and simulation values of V_{th} and S-slope as a function of gate dielectric permittivity.

6 ACKNOWLEDGEMENT

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REFERENCES

[1] International Technology Roadmap for Semiconductor 2004 edition (http://public.itrs.net).
[2] F. Balestra et al., IEEE Electron Device Lett., 8, 410–412, 1987.
[3] Y. Taur, IEEE Trans. Electron Devices, 48, 2861–2869, 2001.
[4] V.P. Trivedi et al., IEEE SOI Conference, 192-194, 2004.
[5] R.J. Luyken et al., IEEE SOI Conference, 137-139, 2002.
[6] A. Kawamoto et al., IEEE Trans. Electron Devices, 51, 907-913, 2004.
[7] R.S. Shenoy et al., IEEE Trans. Nanotechnology, 2, 265-270, 2003.
[8] T.C. Lim et al., Solid-State Electronics, 49, 1034-1043, 2005.
[9] A. Kranti et al., IEEE SOI Conference, 96-98, 2005.
[10] A. Kranti et al., Semiconductor Science and Technology, 21, 409-421, 2006.
[11] Q. Chen et al., IEEE Trans. Electron Devices, 49, 1086-1090, 2002.
[12] Q. Chen et al., IEEE Trans. Electron Devices, 50, 1631-1637, 2003.
[13] K. Suzuki et al., Solid-State Electronics, 37, 327-332, 1994.
[14] K. Kim et al., International Journal of Electronics, 91, 139-148, 2004.
[15] K. Suzuki et al., IEEE Trans. Electron Devices, 40, 2326-2329, 1993.
[16] R.H. Yan et al., IEEE Trans. Electron Devices, 39, 1704-1710, 1992.
[17] A. Kranti et al., Semiconductor Science and Technology, 20, 423-429, 2005.
[18] X. Liang et al., IEEE Trans. Electron Devices, 51, 1385-1391, 2004.
[19] ATLAS Users manual: Silvaco International 2004.
[20] M. Shoji et al., Journal of Applied Physics, 85, 2722–2731, 1999.
[21] K.N. Ratnakumar et al., IEEE J. Solid-State Circuits, 17, 937–948, 1982.
[22] A. Kranti et al., Solid-State Electronics, 46, 1333-1338, 2002.
[23] D.J. Frank et al., IEEE Electron Device Lett., 19, 385-387, 1998.
[24] G. D. Wilk et al., Journal of Applied Physics, 89, 5243–5275, 2001.