A Compact Model of Ballistic CNFET for Circuit Simulation

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ABSTRACT

With the advent of carbon nanotube technology, evaluating circuit and system performance using these devices is becoming extremely important. In this letter, we propose a quasi-analytical device model for intrinsic ballistic CNFET, which can be used in any conventional circuit simulator like SPICE. The closed form expressions for I-V and C-V characteristics are obtained based on the physical device model. This quasi-analytical model is seen to be effective in a wide variety of CNFET structures as well as for a wide range of operating conditions in the digital circuit application domain.

1. INTRODUCTION

As silicon technology is approaching to its limit, several emerging devices are studied to find a suitable alternative to silicon. Carbon nanotube FETs (CNFET) are shown to have potential of taking this place in the post silicon era. It's interesting structural and electrostatic properties (e.g., near ballistic transport) make it attractive for the future integrated circuit applications [1]. Consequently, interests have grown to predict the performance of these devices in circuits and systems [2-6]. However, circuit simulation using CNFET at present is a difficult task, because most of the developed device models are numerical [2, 7], which conventional circuit simulators like SPICE can not handle. A good analytical model to express the electrostatic properties (e.g., I-V and C-V characteristics) of these devices is thus necessary for circuit simulation.

A few attempts have been recently made to achieve analytical model for CNFET [6, 8]. However, while the empirical model in [6] is not effective for all operating conditions due to its underlying assumptions, the nanowire model proposed in [8] may not be appropriate (as proposed) for CNFET because of its centroid based approach.

In this paper, we propose a circuit compatible quasi-analytical device model, which can be used for different semiconducting CNFET structures at all operating conditions in the digital circuit application domain. This compact model will greatly facilitate the circuit simulation using any conventional simulator like SPICE. The model is developed assuming the ballistic transport of CNFET [2] and shown to have close agreement with physical model for different CNFET diameters.

The rest of the paper is organized as follows. In section 2, we describe the developed compact model for ballistic CNFET. Section 3 compares the proposed analytical model with the numerically solved physical model followed by a conclusion in section 4.

2. COMPACT MODEL FOR CNFET

For circuit simulation using conventional simulator like SPICE we need an analytical expression for device (e.g., *I-V* and *C-V*) characteristics in terms of applied terminal voltages (e.g., V_{gs}, V_{ds}). However, it is impossible to obtain analytical expressions directly by solving self consistent device equations [2, 7]. As a result, all developed physical device models use numerical techniques to obtain device characteristics, where the reference point is the surface potential, ψ_s (*not the terminal potential*: V_g, V_d or V_s [Fig. 1(b)]) [2, 7]. In this paper, we empirically obtain closed form expressions in terms of the terminal voltages based on the observation from physical model. The developed quasi-analytical model also has a strong foundation on physics and hence, is seen to be effective for a wide variety of CNFET structures.

In this analysis, we assume ballistic transport in MOSFET like single-walled CNFET with one-dimensional (1-D) electrostatics [9]. Short channel MOSFET like CNFETs are of particular interest because they are shown to provide near ballistic current, thereby indicating the maximum performance [10, 11]. The carrier density for any sub-band (*p*th) of such nanotube transistor can be expressed as [2],

$$n_p = \int_{E_{e,p}}^{\infty} \frac{D_p(E)}{2}\left[f(E-\mu_s)+f(E-\mu_d)\right]dE \qquad (1)$$

where $\mu_{s(d)}$ is the source (drain) Fermi level, $E_{c,p}$ be the conduction band minimum for the *p*th sub-band, $f(E)$ is the probability that a state with energy E is occupied and $D(E)$ is the nanotube density-of-states, which can be approximated as $D_0 |E| \Big/ \sqrt{E^2 - E_{c,p}^2}$ for low bias [12]. $D_0 = 8/(3\pi V_{\Pi} b)$, where V_{Π} and b are respectively, the carbon-carbon bonding energy and the distance. Normalizing all energies and voltages by the thermal voltage, β ($k_B T/q$) and substituting $\varepsilon^2 - \varepsilon_{c,p}^2 = z^2$ ($\varepsilon = E/\beta$), Eq. (1) can be written as,

$$n_p = N_0 \sum_{v_i = v_s, v_d} \left[\int_0^{\infty} \frac{dz}{1 + e^{\left(\sqrt{z^2+\varepsilon_{c,p}^2} - (\varphi_s - v_i)\right)}} \right], \quad N_0 = \frac{\beta D_0}{2} \qquad (2)$$

where φ_s (ψ_s/β), v_s and v_d are the normalized surface, source and drain potentials, respectively. k_B is the

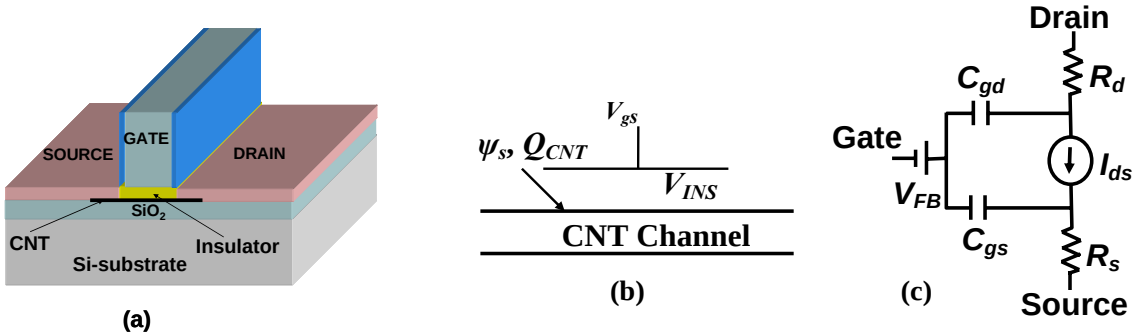


Fig. 1 (a) Schematic of a carbon nanotube transistor. (b) Electrostatic equivalent and (c) Equivalent circuit of a ballistic CNFET for circuit simulation. R_s and R_d are the source and drain contact resistance, respectively.

Boltzmann's constant, q is the electronic charge and T is the absolute temperature (°K). Note that n_p is a function of ψ_s, which is further related to terminal voltage, V_{gs} (neglecting the flat-band voltage; see Fig. 1) as,

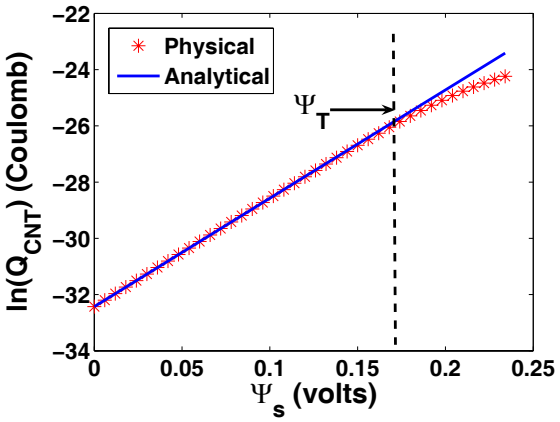
$$\psi_s = V_{gs} - V_{INS} = V_{gs} - \frac{Q_{CNT}}{C_{INS}} \qquad (3)$$

where Q_{CNT} ($\Sigma_p n_p$) and C_{INS} are the nanotube charge and insulator capacitance respectively. Analytically solving (2) and (3) simultaneously to obtain n_p (when ψ_s is not known) is impossible and hence, we empirically obtain analytical expressions for Q_{CNT} - ψ_s based on the following observations from physical model (which also matches closely with experiments [2, 10]).

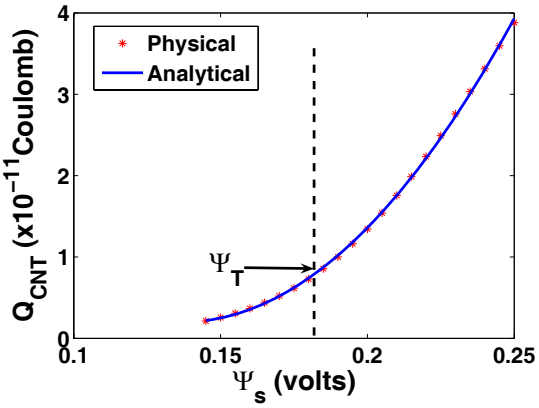
1. Q_{CNT} varies exponentially with ψ_s below a certain value (ψ_T, see Fig. 2a). The corresponding V_{gs} may be called as the threshold point, V_T. This is because the total charge in the channel for $\psi_s < E_{c,1}/q$ (the conduction band minima of the first sub-band) is very low and hence, V_{gs} is mostly dropped across the channel.
2. Above V_T, Q_{CNT} varies quadratically with ψ_s (V_{gs} is mostly dropped across insulator; Fig. 2b).
3. Effect of V_{ds} (drain to source potential) is insignificant for $V_{ds} > 3k_BT/q$ (Fig. 3).

The numerical model proposed in [7] represents the quantization effect and abrupt changes in slope (in Q_{CNT} vs. V_{ds}) is observed at low temperatures ($T \to 0$). However, for digital circuit simulation a closed form expression is required and hence, we model Q_{CNT} -V_{ds} as an approximate continuous variation. Based on the above observation, Q_{CNT} can be expressed as

$$Q_{CNT} = e^{(\alpha_0 + \alpha_1 \psi_s)} \quad \text{for } \psi_s < \psi_T$$
$$= \lambda_0 + \lambda_1(\psi_s - \psi_T) + \lambda_2(\psi_s - \psi_T)^2 \quad \text{for } \psi_s \geq \psi_T \qquad (4)$$



(a)



(b)

Fig. 2 Charge vs. channel potential of a ballistic carbon nanotube FET. (a) $\psi_s < \psi_T$; (b) $\psi_s > \psi_T$.

where α_0, α_1, λ_i (i = 1, 2, 3) are constants for a particular nanotube structure. Substituting Q_{CNT} in (3) an analytical closed form expression for V_g-ψ_s then can be obtained as

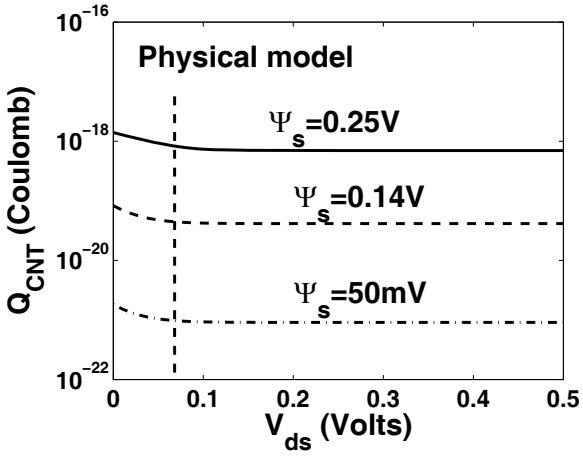


Fig. 3 Charge vs. channel potential of a ballistic carbon nanotube FET. Impact of drain potential (V_{ds}) on charge.

$$\psi_s = V_{gs} - lambertw\left[\frac{\alpha_1}{C_{INS}} e^{(\alpha_0+\alpha_1 V_{gs})}\right] \Big/ \alpha_1 \quad \text{for } V_{gs} \le V_T \tag{5}$$

$$= \psi_T - \frac{(\lambda_1 + C_{INS})}{2\lambda_2} + \frac{\left[(\lambda_1 + C_{INS})^2 - 4\lambda_2[\lambda_0 - C_{INS}(V_{gs} - \psi_T)]\right]^{1/2}}{2\lambda_2} \quad \text{for } V_{gs} > V_T$$

Based on the third observation, the effect of V_{ds} (2D effect) now can be included by modifying the constants α_0 and λ's by a factor $\left(1 + e^{-V_{ds}/(\eta\beta)}\right)$. η is usually '1' but can be adjusted empirically. Note that in [6], authors assumed ψ_s is equal to V_{gs} for $V_{gs} < V_T$ and it varies linearly with V_{gs} for $V_{gs} > V_T$. This assumption is valid only for very low gate voltages and is a special case of the proposed formulation. Knowing ψ_s in terms of the terminal voltages the drain current, I_{ds} and gate input capacitance, C_G (Fig. 1) can be easily obtained as follows [6].

$$I_{ds} = \frac{4qk_BT}{h}\sum_p \left[\ln(1 + e^{-\xi_s}) - \ln(1 + e^{-\xi_d})\right] \tag{6}$$

and $C_G = \dfrac{\partial Q_{CNT}}{\partial V_{gs}}$

where $\xi_i = \dfrac{\psi_s - E_{c,p} - \mu_i}{k_BT}$ ($i = s, d$) and h is the Planck's constant. Further, typical values for R_s and R_d (Fig. 1) can be used based on the experimental results for circuit simulation.

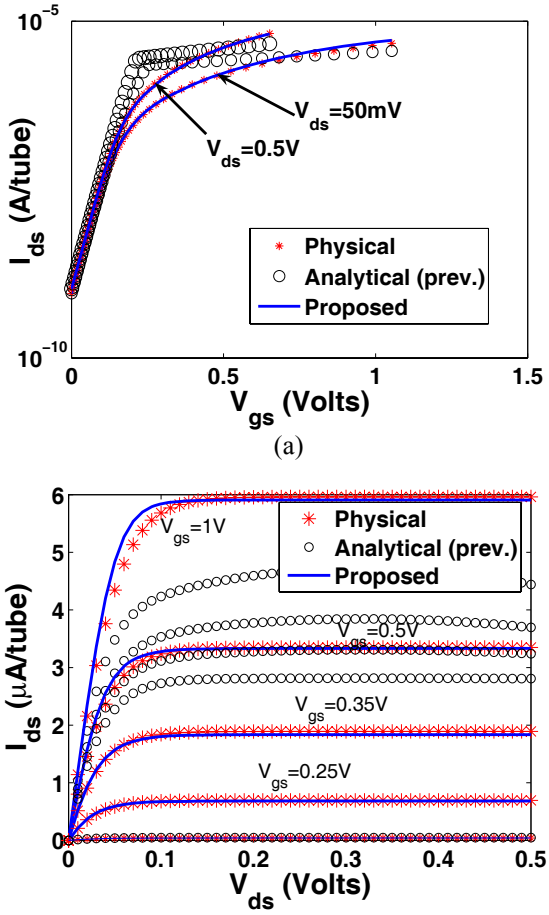


Fig. 4 Characteristics of CNFET with diameter = 2nm and C_{INS} = 48.3 pF/m, V_T = 0.3V (T = 300°K). (a) I_{ds}-V_{gs} for different V_{ds}; (b) I_{ds}-V_{ds} for different V_{gs}.

3. RESULTS AND DISCUSSION

Fig. 4 shows the I-V (I_d-V_g and I_d-V_d) characteristics of a CNFET with 2nm diameter and 48.3 pF/m insulator capacitance. Though $\psi_s = E_{c,1}$, the conduction band minima of the first sub-band can be assumed as the threshold point (and the corresponding V_{gs} as V_T) from physics point of view, we however, prefer V_T to be obtained empirically for better accuracy. This is because, there will be significant number of thermally generated free carriers even when ψ_s is slightly less than $E_{c,1}$. V_T then can be obtained by solving Eqs. (3) and (4) with $\psi_s = \psi_T$. It can be seen from Fig. 4 that while the model proposed in [6] does not match with the physical model for large bias conditions, our proposed model matches closely for a wide range of bias conditions. We also verified our model for different nanotube diameters (1-3nm) and obtained close match with physical model in all cases.

Fig. 5 shows the SPICE simulation result of a two input NAND gate driving three identical gates [CNT:

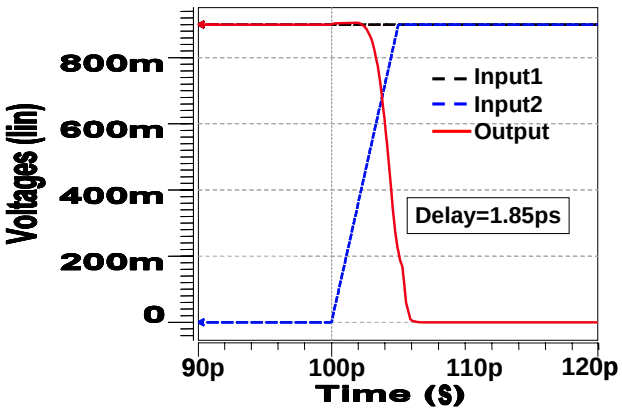


Fig. 5 Circuit performance of CNFET with diameter = 2nm and C_{INS} = 48.3 pF/m. Input/output waveform of a 2 input NAND with fanout 3 and assuming 100 tubes in one transistor.

diameter=2nm and L_{ch}=20nm (V_{dd} = 0.9V)]. We used 100 nanotubes for PCNFET and 200 parallel nanotubes for series connected NCNFETs. As can be seen from the figure, a considerably fast response time (1.85ps) was obtained using the intrinsic devices. We did not compare CNFET with the performance of 45nm CMOS gate using any technology model such as BPTM, because these models include parasitics, which is not considered in the developed CNFET model.

4. CONCLUSIONS

In this letter, we provided a quasi-analytical circuit compatible model for intrinsic ballistic CNFET. The empirical parameters used to develop the analytical model can be easily obtained from the device I-V measurements. This simple model is seen to be very effective for various CNFET structures with a wide range of bias conditions, and will greatly facilitate circuit simulations using these devices. To demonstrate the effectiveness of the model we simulated the performance of a two input NAND using HSPICE.

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