Explicit Threshold Voltage Based Compact Model of Independent Double Gate MOSFET

M. Reyboz [(1)], T. Poiroux[(1)], O. Rozeau[(1)], P.Martin[(1)] and J. Jomaah[(2)].

[(1)] LETI/CEA-Grenoble, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France
[(2)] IMEP, 23, rue des Martyrs, BP 357, Grenoble Cedex, France
Email: rozeau@chartreuse.cea.fr, Tel: (+33) 4 38 78 59 57, Fax: (+33) 4 38 78 51 59

Abstract: *This paper describes an explicit, continuous and threshold voltage (V_{th}) based compact model of Independent Double Gate (IDG) MOSFET with undoped channel. This model is derived thanks to Poisson equation resolution. Without any fitting parameter or charge sheet approximation, it provides explicit analytical expressions of drain current considering long and short undoped transistor. Consequently, this is a fully analytical and predictive model allowing the description of planar DG MOSFET (symmetrical, asymmetrical and independent) as well as FinFET structures. The validity of this model is demonstrated by comparison with Atlas simulations. The model was implemented in VerilogA in order to test it and to design circuits. Simulation circuit results of a signal mixer and of an inverter are presented.*

Introduction: DG MOSFETs are promising devices because they can be scaled to the shortest channel length, particularly IDG MOSFETs because the front and the back gate can be independently driven. They enlarge the circuit design space. That is why a compact model is crucial to take advantage of this new technology. However, explicit IDG MOSFET compact model does not really exist. Indeed, existing models require numerical resolutions or are not valid in all operating modes: [1]-[4].

This article presents a V_{th}-based model of IDG MOSFET, which could be integrated in standard BSIM model. Then, the model was validated by confrontation with numerical simulations [5] and implemented in VerilogA to design circuits. Circuit simulation results are presented to illustrate its robustness.

V_{th} model: We propose to model an IDG MOSFET, with undoped silicon film. IDG MOSFET is shown on Figure 1. L is the gate length, T_{si} is the silicon film (or body) thickness, T_{ox1} and T_{ox2} are the front and the back gate oxide thicknesses, respectively. V_{g1} and V_{g2} are the front and the back gate voltages. Without generality loss, $\Delta\Phi_{m1}$ (respectively $\Delta\Phi_{m2}$), the work function difference between the front (respectively back) gate and the intrinsic silicon is supposed zero. To model this device, some assumptions were taken into account: Boltzmann statistics was chosen, the current is the sum of the diffusion and drift currents as in the Pao and Sah model, no quantum effect and no ballistic transport are considered.

1D Poisson equation is solved to derive the drain current I_{ds}. Boundary conditions, electrical neutrality and physical assumptions allow getting explicit I_{ds}. Poisson's equation within the gradual channel approximation is:

$$\frac{d^2\psi(x,\,y)}{dy^2} = \frac{q.n_i}{\varepsilon_{Si}} \cdot \exp\left[\frac{\psi(x,\,y) - \phi_{imref}(x)}{u_t}\right] \qquad (1)$$

$\Psi(x,y)$ is the potential in the silicon film, q is the electron charge, n_i the intrinsic doping, ε_{si} the silicon permittivity. u_t is the thermal voltage and Φ_{imref} is the quasi Fermi level of electrons in the channel. Boundary conditions are:

$$V_{g1} - \Delta\phi_{m1} = \psi_{s1} + \frac{T_{ox1}Q_{g1}}{\varepsilon_{ox1}} \qquad Q_{g1} = -\varepsilon_{Si}\frac{\partial\psi_{s1}}{\partial y} \qquad (2)$$

$$V_{g2} - \Delta\phi_{m2} = \psi_{s2} + \frac{T_{ox1}Q_{g2}}{\varepsilon_{ox2}} \qquad Q_{g2} = \varepsilon_{Si}\frac{\partial\psi_{s2}}{\partial y} \qquad (3)$$

Ψ_{s1} and Ψ_{s2} are the front and the back surface potentials. Q_{g1} and Q_{g2} are the front and the back gate charge. ε_{ox1} is the front gate oxide permittivity and ε_{ox2} is the back one. Electrical neutrality is expressed as:

$$Q_{g1} + Q_{g2} + Q_{inv} = 0 \qquad (4)$$

Q_{inv} is the inversion charge.

After integration of Poisson's equation between both interfaces with Gauss's law, we get:

$$Q_{g1}^{\ 2} - Q_{g2}^{\ 2} = 2q.n_i\varepsilon_{Si}u_t\left[\exp\left(\frac{\psi_{S1} - \phi_{imref}}{u_t}\right) - \exp\left(\frac{\psi_{S2} - \phi_{imref}}{u_t}\right)\right] \quad (5)$$

The goal of this approach is to describe the inversion charge Q_{inv} as the sum of Q_{inv1} and Q_{inv2} related to front and back interface, depending respectively on V_{g1}-$V_{th1}(V_{g2})$ and V_{g2}-$V_{th2}(V_{g1})$. The obtained charge expressions will be smoothed between weak and strong inversion regimes. This approach leads to current expressions similar to that of bulk MOSFETs.

When both interfaces are in weak inversion, the silicon film is in volume inversion. We assume that the inversion charge contribution on the device electrostatic behavior is negligible. The transverse electric field is uniform since the channel is assumed undoped. When both interfaces are in strong inversion, both inversion charges are independent since front and back interfaces are not coupled. If one interface is in strong inversion and the other one in weak inversion, Q_{inv} is supposed to be equal to the strong inversion charge.

To calculate the threshold voltage at the front interface (for instance), we assume the silicon film to be in weak inversion and the inversion charge of back interface to be negligible compared to that of front interface. In this case:

$$\psi_{S1} - V_{g2} >> u_t \quad (6)$$

We obtain the front inversion charge at threshold condition:

$$Q_{inv1}^{th} = -n_1C_{ox1}u_t \quad (7)$$

With,

$$n_1 = 1 + \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} \quad (8)$$

$C_{ox1,2}$ are the front and the back gate oxide capacitances. C_{si} is the silicon film capacitance.

Moreover, the inversion charge of the front interface can be written as:

$$Q_{inv1}(x) = -n_1C_{ox1}u_t\exp\left(\frac{V_{g1} - V_{th1}(V_{g2}) - n_1\phi_{imref}(x)}{n_1u_t}\right) \quad (9)$$

With,

$$V_{th1} = n_1u_t\ln\left[\frac{2n_1C_{ox1}u_t}{q.n_iT_{Si}}\right] - (n_1 - 1)V_{g2} - n_1u_t\ln\left(\frac{\tanh\left[\frac{C_{eq}}{C_{Si}}\frac{V_{g2} - V_{g1}}{2u_t}\right]}{\frac{C_{eq}}{C_{Si}}\frac{V_{g2} - V_{g1}}{2u_t}}\right) \quad (10)$$

And with,

$$C_{eq} = \frac{1}{\frac{1}{C_{ox1}} + \frac{1}{C_{Si}} + \frac{1}{C_{ox2}}} \quad (11)$$

The threshold voltage expression (10) is valid as long as the opposite interface is in weak inversion. The threshold voltage dependence with the opposite gate voltage disappears when the opposite interface is in strong inversion, more precisely when the inversion charge of the opposite interface becomes significant compared to its threshold value. From the analogue expression to (9) for Q_{inv2}, we obtain the following coupling condition on V_{g2}:

$$V_{g2} < V_{th2} + n_2\phi_{imref} + n_2u_t \quad (12)$$

In (12), the threshold voltage V_{th2} is given by the analogue of (10) only when the coupling exists.

The value of V_{th2}, which must be taken into account in (12) is the maximum value between those given by expression (10) and the limit value V_{th2lim}.

$$V_{th2\,\lim} = u_t\ln\left[\frac{2n_2C_{ox2}u_t}{q.n_iT_{Si}}\right] + \frac{n_2 - 1}{n_2}\Delta V_{th} - u_t\ln\left(\frac{\tanh\left[\frac{C_{eq}}{C_{Si}}\frac{\Delta V_{th}}{2u_t}\right]}{\frac{C_{eq}}{C_{Si}}\frac{\Delta V_{th}}{2u_t}}\right) \quad (13)$$

With,

$$\Delta V_{th} = \frac{n_1n_2}{n_1 + n_2 - n_1n_2}u_t\ln\left[\frac{n_1C_{ox1}}{n_2C_{ox2}}\right] \quad (14)$$

In other words, the gate voltage, which should be considered in equation (10) is the maximum between V_{g2} and $V_{th2lim} + n_2.u_t$.

The drain current I_{ds} is given as:

$$I_{ds} = \mu\frac{W}{L}\int_{V_s}^{V_d}Q_{inv}\,d\phi_{imref} \quad (15)$$

$$I_{ds} = I_{ds1} + I_{ds2} \quad (16)$$

W is the gate width and μ is the mobility.

After some calculations, we get the following expressions of the front and back gate current:

$$I_{ds1} = \frac{W}{L}\mu.C_{ox1}V_{gt1,eff}\left(1 - n_{1,eff}\frac{V_{ds1,eff}}{2\left(V_{gt1,eff} + 2u_t\right)}\right)V_{ds1,eff} \quad (17)$$

$$I_{ds2} = \frac{W}{L}\mu.C_{ox2}V_{gt2,eff}\left(1 - n_{2,eff}\frac{V_{ds2,eff}}{2\left(V_{gt2,eff} + 2u_t\right)}\right)V_{ds2,eff} \quad (18)$$

$V_{gti,eff}$ (which have the same form as in [6]) represent the effective gate voltages and $n_{i,eff}$ are the effective coupling factors. They allow continuity between weak and strong inversion.

$V_{gti,eff}$ are defined thanks to a threshold voltage, which takes into account interface coupling between front and back interfaces.

$V_{dsi,eff}$ are the effective drain voltages, which allow continuity between linear and saturation regime.

Figures 2, 3, 4 and 5 present comparisons between Atlas simulations and the compact model.

Empirical Short Channel Effects (SCE): SCE are modelled only on the threshold voltage V_{th} and on the subthreshold slope. This kind of modelling is the one used in BSIM model [6].

The threshold voltage expressions are:

$$V_{th1} = V_{th1,long} - V_{th1,sce} - V_{th1,dibl} \quad (19a)$$

$$V_{th2} = V_{th2,long} - V_{th2,sce} - V_{th2,dibl} \quad (19b)$$

Where the $V_{thi,long}$ are the threshold voltage for long and large devices. $V_{thi,sce}$ is the threshold voltage degradation due to the short channel effect. $V_{thi,dibl}$ is the threshold voltage degradation due to the DIBL effect. Using numerical simulations, the V_{th} was extracted with the transconductance derivative method. Figure 6 shows the numerical V_{th} compared to the analytical model. Thanks to these extractions, the V_{th} parameters were obtained. To verify the model behaviour, a set of numerical simulations using Atlas (Silvaco) was performed. These simulations were realized for L=130, 70, 40 and 20nm.

For short-devices, the substhreshold slopes are modified by the electric fields at the silicon-oxide interfaces, which are modified near to the drain and source regions. As a consequence, the interface coupling is reduced. To model this effect, new coupling parameters were defined:

$$n_{1sce} = n_1\left(1 + CDSC\left(\exp\left(-\frac{DVT1SCE1 \cdot L}{2}\sqrt{\frac{C_{ox1}}{\varepsilon_{si}T_{si}}}\right) + 2\exp\left(-DVT1SCE1 \cdot L\sqrt{\frac{C_{ox1}}{\varepsilon_{si}T_{si}}}\right)\right)\right) \quad (20a)$$

$$n_{2sce} = n_2\left(1 + CDSC\left(\exp\left(-\frac{DVT2SCE1 \cdot L}{2}\sqrt{\frac{C_{ox2}}{\varepsilon_{si}T_{si}}}\right) + 2\exp\left(-DVT2SCE1 \cdot L\sqrt{\frac{C_{ox2}}{\varepsilon_{si}T_{si}}}\right)\right)\right) \quad (20b)$$

Currently, parameters *CDSC, DVT1SCE1* and *DVT2SCE1* are obtained by fitting but they will be replaced by analytical expressions. Figures 7a and 7b compare the simulations with the compact model for devices with channel length of 70nm and 20nm. These figures show the good agreement between the simulations and the compact model.

Model validation on basic designs: This compact model was implemented in VerilogA to allow simulations under Eldo (Anacad) or ADS (Agilent) software. Simulation results of a mixer and an inverter are presented on Figures 6 and 7 to illustrate robustness of this model in simulators.

Conclusion: In this work, an explicit compact model was developed for undoped IDG MOSFET which is valid for all operating modes. Comparisons with Atlas simulations prove the validity and accuracy of this model. Moreover, the model was implemented in VerilogA and circuits were simulated. The robustness of the model is excellent. This is demonstrated thanks to the simulation of a mixer and an inverter. Finally, equations of this model could easily be integrated in BSIM3v3 and BSIM4 models. For instance, the V_{th0}, n and V_{off} parameters of BSIM models were adapted for long DG MOSFET [6].

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References

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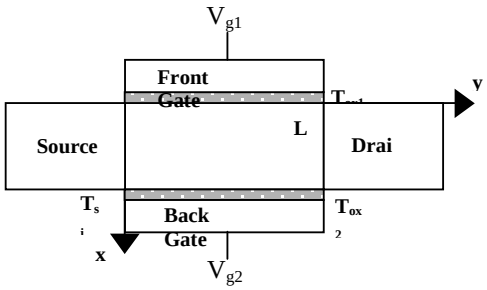

Figure 1: IDG MOSFET.

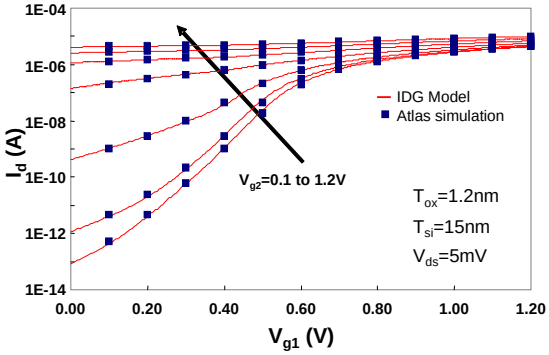

Figure 2: Drain current versus front gate voltage for several back gate voltage values at low drain voltage (V_{ds}=*5mV*) in logarithmic representation. *L=0.5μm* and *W=1μm*.

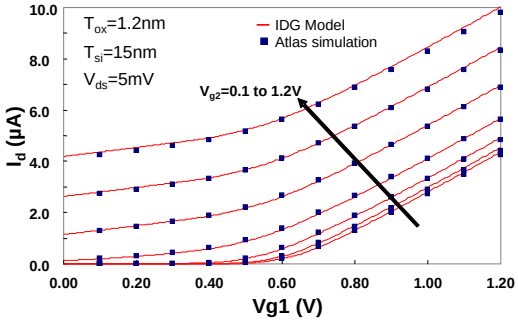

Figure 3: Drain current versus front gate voltage for several back gate voltage values at V_{ds}=*5mV* in linear representation. *L=0.5μm* and *W=1μm*.

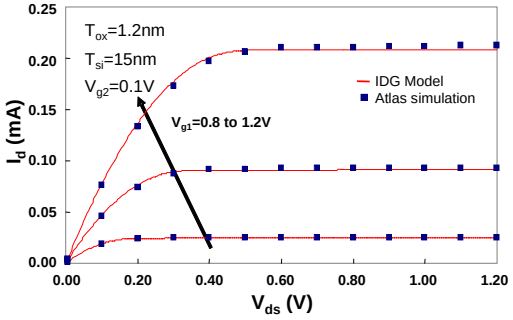

Figure 4: Drain current versus drain voltage for several front gate voltage values at low back gate voltage (V_{g2}=*0.1V*). *L=0.5μm* and *W=1μm*.

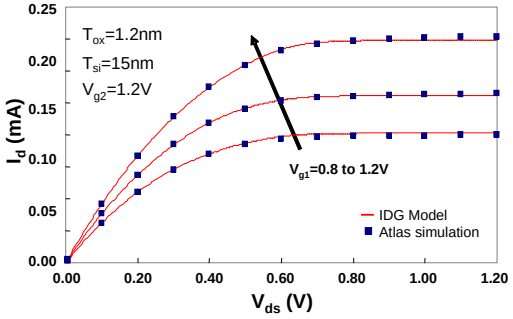

Figure 5: Drain current versus drain voltage for several front gate voltage values at high back gate voltage (V_{g2}=*1.2V*). *L=0.5μm* and *W=1μm*.

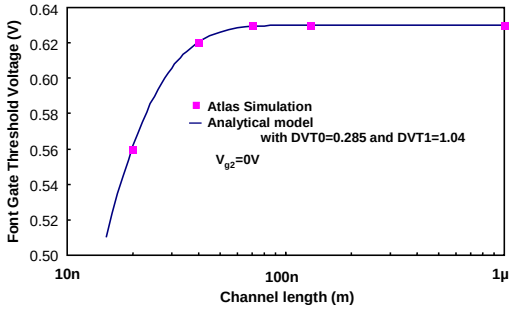

Figure 6: Threshold voltage versus channel length at V_{g2}=*0V* for a nMOSFET with T_{si}=*10nm* and T_{ox}=*1nm*.

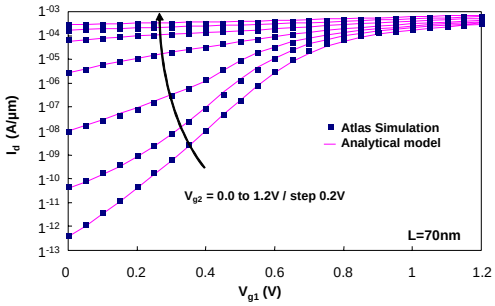

Figure 7a: Drain current versus front gate voltage for several back gate voltage values at V_{ds}=*50mV* in logarithmic representation, for a nMOSFET with T_{si}=*10nm*, T_{ox}=*1nm*, *L=70nm* and *W=1μm*.

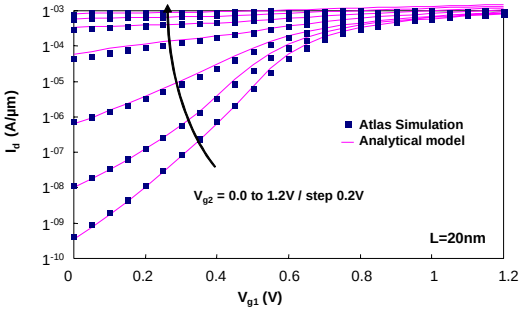

Figure 7b: Drain current versus front gate voltage for several back gate voltage values at V_{ds}=*50mV* in logarithmic representation, for a nMOSFET with T_{si}=*10nm*, T_{ox}=*1nm*, *L=20nm* and *W=1μm*.

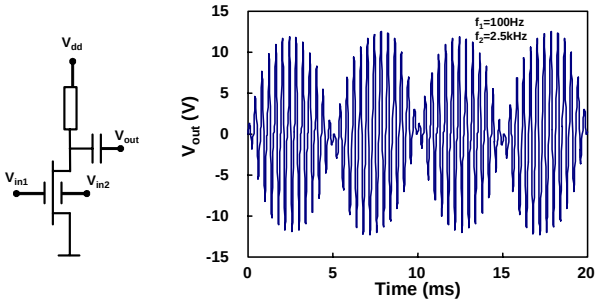

Figure 6a and 6b: Schematic of a basic mixer and simulation results. *L=0.5μm* and *W=1μm*.

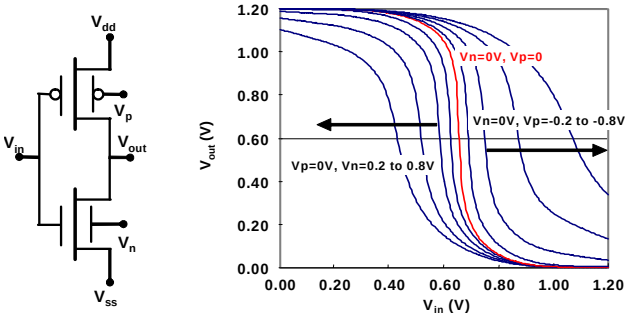

Figure 7a and 7b: Schematic of an inverter and simulations with back gate voltage control using IDG compact model. *Ln=Lp=1μm, Wn=5μm* and *Wp=10μm.*

TOPIC AREA: Double Gate MOS Models