A Carrier-Based Analytic Model for Undoped Surrounding-Gate MOSFETs

Jin He, Xing Zhang, Mansun Chan*, and Yangyuan Wang

Institute of Microelectronics, EECS, Peking University, Beijing, 100871, P.R.China
*Department of EEE, Hong Kong University of Science & Technology, Kewloon, Hong Kong
Tel: 86-10-62765916 Fax: 86-10-62751789 e-mail: jinhe@ime.pku.edu.cn

ABSTRACT

A carrier-based analytic model for undoped surrounding-gate MOSFETs is presented in this paper. It is based on an exact solution of the Poisson equation and the Pao-Sah current formulation in terms of the carrier concentration. From this model, the different dependences of the surface potential, centric potential, inversion charge and the current on the silicon body thickness and the gate oxide are elucidated analytically and then the predicted DCIV characteristics are compared with the 3-D numerical simulations. The analytical results of the model presented also show in a good agreement with the 3-D simulation, demonstrating the model is valid for all operation regions and traces the transition between them without any need for the fitting parameter..

Keywords: Non-classical MOSFETs; Device physics; Compact modeling; Surrounding-gate MOSFET; Carrier-based model

1 INTRODUCTION

When the semiconductor industry is facing the rapid approach of conventional or classical CMOS technologies to the likely end of their ability to address the most advanced 32-nm and 22-nm technology of the ITRS, very promising results are reported for new directions of CMOS transistors utilizing the concepts of the non-classical MOSFET structures for the 32-nm technology node and below[1-5]. These devices structures include Double-Gate (DG) MOSFETs, the Pi-Gate (PG) MOSFETs, and the cylindrical Surrounding Gate (CSG) MOSFETs. In particular, CSG MOSFETs offer the best control of short channel effect and sub-threshold characteristic.

The development of compact models for those device structures is a key to enabling successful circuit and product design. Research activities to address compact modeling of these new devices have been started, but are not nearly at the level required for successfully supporting production design cycles in the near future. Hence, a new era of fundamental research for compact modeling is necessary, which will facilitate and enable our learning curve of circuit design with non-classical devices. Compact modeling of such non-classical MOSFET devices calls for a fundamentally different device physics and approach from the conventional bulk CMOS because of several special physical effects such as the carrier energy level quantization and the 'volume inversion', a non-charge-sheet phenomena. In contrast, the previous studies on CSG MOSFETs only focused on the threshold characteristics [5-6] with semi-empirical models [7-8].

In one recent publication [9], D.Jimenez and his co-workers developed a potential-based model and the result matched well with the 3-D simulation. This models is , however, still tedious for practical compact model application in the CAD simulation due to the numerical complexity and time consuming nature of iteration technique in solutions of the intermediate variables and auxiliary functions such as β, $g_r(\beta)$ and $f_r(\beta)$. On the other hand, some special physics effects such as the gate oxide and silicon body thickness on the channel potential distribution and the device performance have not been demonstrated and discussed in the detail in this letter.

Following a quite different method and extending our previous work [10], a carrier-based non-charge-sheet analytic model for CSG MOSFETs is developed from both the Poisson equation solution and the Pao-Sah current formulation [11] in this paper. It is shown that the developed analytic model covers all three regions of CSG MOSFET operation in terms of the carrier concentration function, and yet is completely physics based without any need for the additional assumptions, the auxiliary functions or variables. The different dependences of the surface potential, centric potential, inversion charge and the current on the silicon body thickness and the gate oxide are demonstrated and elucidated in details from this model. Further, the model has also been validated by the 3-D numerical simulations, implying it is an ideal model framework for CSG MOSFET compact modeling if the appropriate second order effects such as the poly-silicon depletion and quantum-mechanical effects, and the velocity saturation effect are integrated into it.

2 MODEL DEVELOPMENT

The undoped CSG MOSFET is shown in Fig.1. The cylindrical coordinate formulation of the Poisson-Boltzmann equation this case is given by

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right)=\frac{kT}{qL_i^2}\exp\left[\frac{q(\phi-V_{ch})}{kT}\right] \tag{1}$$

subject to the boundary conditions

$$\left.\frac{d\phi}{dr}\right|_{r=0}=0 \quad \text{and} \quad \phi\big|_{r=R}=\phi_s\,,\ \ \phi\big|_{r=0}=\phi_0 \tag{2}$$

On the other hand, the applied gate voltage, surface potential and total inversion charge density must satisfy the boundary condition according to the Gauss's law

$$V_G-\Delta\phi_i=\phi_S+E_{ox}t_{ox}=\phi_s+\frac{Q_{in}}{\varepsilon_{ox}}R\ln\left[1+\frac{t_{ox}}{R}\right] \tag{3}$$

Following our previous work, the analytical solution of (1) is given by

$$\phi=\phi_0-\frac{2\,kT}{q}\ln\left[1-\alpha r^2\right] \tag{4}$$

The solution of Eq. (4) is substituted into Eq. (1) and using the boundary condition (2), we obtain

$$\alpha=\frac{\exp[\theta_0-v_{ch}]}{8L_i^2} \tag{5}$$

Finally, the concise analytical solution of the potential distribution in the silicon film is obtained from Eq. (4)

$$\phi(r)=\phi_0-\frac{2kT}{q}\ln\left[1-\frac{r^2}{8L_i^2}\exp\left[\frac{q(\phi_0-V_{ch})}{kT}\right]\right] \tag{6}$$

This equation seems too complex because of exponential and logarithm characteristics. Here we use the Boltzmann statistics to simplify the related calculation

$$n=n_i\exp\left(\frac{q(\phi-V_{ch})}{kT}\right) \tag{7}$$

$$n_0=n_i\exp\left(\frac{q(\phi_0-V_{ch})}{kT}\right) \tag{8}$$

The term ϕ_0-V_{ch} in Eq. (6) can be replaced by a function of the silicon center mobile electron concentration. In this case, Eq. (6) is converted into

$$\phi(r)=V_{ch}+\frac{kT}{q}\ln\left[\frac{n_0}{n_i}\right]-\frac{2kT}{q}\ln\left[1-\frac{r^2}{8L_i^2}\frac{n_0}{n_i}\right] \tag{9}$$

Differentiating Eq.(9) gives the vertical field distribution in the silicon film

$$E(r)=\frac{rkT}{2qL_i^2}\frac{\frac{n_0}{n_i}}{\left[1-\frac{r^2}{8L_i^2}\frac{n_0}{n_i}\right]} \tag{10}$$

And then the differentiation of Eq. (10) gives the carrier distribution in the silicon film

$$n(r)=\frac{n_0}{\left[1-\frac{r^2}{8L_I^2}\frac{n_0}{n_i}\right]^2} \tag{11}$$

As a result, we have obtained the analytical surface potential and surface electrical field expressions from Eqs. (9) and (10), respectively

$$\phi_s=V_{ch}+\frac{kT}{q}\ln\left[\frac{n_0}{n_i}\right]-\frac{2kT}{q}\ln\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right] \tag{12}$$

$$E_s=\frac{RkT}{2qL_i^2}\frac{\frac{n_0}{n_i}}{\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]} \tag{13}$$

Finally, the inversion charge density is also obtained from the surface electrical field

$$q_I=\frac{\varepsilon_{si}RkT}{2qL_i^2}\frac{\frac{n_0}{n_i}}{\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]} \tag{14}$$

Substituting Eqs.(12) and (14) into the Gauss's law-Eq.(3), a complete equation of the silicon center mobile carrier concentration as a function of the gate voltage, quasi Fermi potential, and the geometry structure is derived

$$V_G-\Delta\phi-V_{ch}=\frac{kT}{q}\ln\left(\frac{n_0}{n_i}\right)-\frac{2kT}{q}\ln\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]+\frac{R^2\varepsilon_{si}kT\ln\left[1+\frac{t_{ox}}{R}\right]}{2qL_i^2\varepsilon_{ox}}\frac{\frac{n_0}{n_i}}{\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]} \tag{15}$$

It is evidently that the mobile carrier concentration on the silicon film center can be obtained from Eq. (15) for the given gate voltage, quasi Fermi potential and structure parameters such as the oxide layer thickness and the silicon film thickness. As a result, Eqs. (11) and (9) directly give the channel potential and carrier distribution in the silicon film.

Following the Pao-Sah current formulation [13], integrating $I_{ds}dy$ from the source to the drain and expressing V_{ch}/dy as $(dV_{ch}/dn_0)(dn_0/dy)$, the drain current is written as

$$I_{DS}=\mu\frac{W}{L}\int_0^{V_{DS}}Q_i(V_{ch})dV=\mu\frac{W}{L}\int_{n_{0S}}^{n_{0D}}Q_i(n_0)\frac{dV_{ch}}{dn_0}dn_0 \tag{16}$$

Where n_{0S} and n_{0D} are solutions of (15) corresponding to $V_{ch}=0$ and $V_{ch}=V_{ds}$, respectively. Note that the dV_{ch}/dy can also be expressed as a function of n_0 by differentiating (15). Substituting these factors into (16), integrating can be performed analytically to yield:

$$I_{ds}=\mu\frac{2\pi\varepsilon_{si}}{L}\left(\frac{2kT}{q}\right)^2\left[\ln\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]+\frac{2\left[\varepsilon_{ox}-2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)\right]}{\varepsilon_{ox}\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]}+\frac{2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)}{\varepsilon_{ox}\left[1-\frac{R^2}{8L_i^2}\frac{n_0}{n_i}\right]^2}\right] \tag{17}$$

The analytical trans-conductance and output conductance are derived out from (17), respectively

3 RESULTS AND DSICUSSION

CSG MOSFET characteristics for all regions: linear, saturation, and sub-threshold, is generated from this continuous, analytic model. In order to test the analytic model we have simulated one well-tempered surrounding-gate MOSFETs with 3-D numerical simulations from DESSIS-ISE® for comparison with the analytical model. A constant effective mobility of 400 cm^2/V-s has been used for both the numerical simulation and analytical calculations. The simulated device has a channel length of

10 μm, different silicon body diameter, and silicon gate oxide t_{ox} of 2 nm.

Fig.2 illustrates the electron concentration and electrical potential distribution in the silicon film predicted by the analytical model for three different effective gate voltages. In low gate voltage or the sub-threshold region, the electron distribution is almost constant along the vertical direction of the film. With the increase of the effective gate voltage, the device goes into the strong inversion region where the surface electron concentration shows several order higher than that of the silicon film center. In this case, the device behaves like a surface channel bulk MOSFET and the surface electron concentration dominates the inversion charge density.

Fig.3 shows the potential at the surface and center of the active silicon versus the applied gate voltage for the different quasi-Fermi-Potential in a SRG MOSFET. It is found that the surface potential versus gate voltage characteristics in a SRG MOSFET is similar to that in a bulk MOSFETs. The potential. at the silicon center, ϕ_0 however, remains constant with the further increase of the gate bias beyond strong inversion, as in the DG MOSFETs. Since the value within logarithm function in (12) must exceed or almost zero ϕ_0 should be pinned by an upper bound of $V_{ch} + kT/q \ln\left[8L_i^2 / R^2\right]$. This effect comes from the fact the high concentration electron near the silicon surface screens the gate field from the silicon center.

Fig.4 demonstrates the total inversion charge versus gate voltage characteristics with different silicon diameter. There are two distinct sub-threshold and strong inversion in CSG MOSFETs, just like that in a conventional MOSFET. One significant difference between the CSG MOSFETs and the conventional thick film MOSFET, however, is the silicon diameter effect. The inversion charge in the sub-threshold region is almost proportional to the square of the silicon diameter because of the area effect, where the volume inversion effect of non-charge-sheet phenomenon dominates, just like that in DG MOSFET. Further, the inversion charge of the CSG MOSFETs in the strong inversion region shows a slight increase with decrease of the silicon body diameter where the effective oxide thickness decreases with decrease of the silicon body diameter as shown in (3): $T_{oxeff} = R * \ln\left[1 + t_{ox}/R\right]$. This unique physical behavior distinguishes the operation of CSG MOSFET from that of DG MOSFETs where the silicon thickness only changes the sub-threshold inversion charge without any effect on the strong inversion charge.

Fig. 5 shows the good comparison of Ids versus Vgs between the analytic model and the 3-D simulation. It is easily found that the analytical prediction matches well with the 3-D simulation. Again, it is found that the sub-threshold current is almost proportional to the square of the silicon body diameter because of the "volume inversion" effect. To optimize the device performance, the silicon film body diameter should be reduced as much as possible to suppress the off-current. Note that the sub-threshold current in (20) is proportional to the cross-sectional area of the CST MOSFET and independent of t_{ox}. This is a characteristic of the volume inversion effect that cannot be captured by standard charge-sheet based model [12].

Fig.6 is I_{ds}-V_{ds} curves calculated from the analytic model (solid curves), compared with the 3-D numerical results (open stars). Both match well in both the linear and the saturation region.

4 CONCLUSIONS

A carrier-based analytic model for the long channel undoped cylindrical surrounding-gate MOSFETs has been derived in this paper by solving the Poisson-Boltzmann equation and the Pao-Sah current formulation in terms of the mobile carrier concentration. All the regions of operation and the transitions of the device are correctly described by single equation of the carrier concentration. In particular, the volume inversion that cannot be captured by using the classical charge-sheet approximation is well accounted and demonstrated in the details by this model. It is also shown that the predicted I-V curves from the model are in complete agreement with the 3-D numerical simulation results without any need for fitting parameter or auxiliary function.

ACKNOWLEDGEMENT

This work is subsided by the special funds for major state basic research project and nature science funds of China. This work is also partially support by a competitive Earmarked Grant HKUST6289/04E from the Research Grant Council of Hong Kong SAR.

REFERENCES

[1] ITRS,"International technology roadmap for semiconductors 2004 update". http://www.itrs.org.

[2] Yuan Taur, IEEE EDL -21, No.5, pp.245-247, 2000.

[3] Jin He, X. Xi, M. Chan, A. Niknejad, C. Hu, Nanotech-2004.vol.2, pp. 45-50. Boston, March, 2004.

[4] Jong-Tae Park, J.P.Collinge, and Carlos H Diaz, IEEE EDL-22, No.8, pp. 405-406, 2001.

[5] S.H.Oh, D.Monore, and J.M.Hergenrother, IEEE EDL-21, No.9, pp. 445-447, 2000.

[6] C.P.Auth and J.D.Plummer, IEEE EDL-18, No.2, pp. 74-76, 1997.

[7] S.L.Jang and S.S.Liu, Solid State Electronics, vol.42, No.5, pp.721-726, 1998.

[8] T.Endoh, T.Nakamura, and F.Masuoka, IEICE Trans Electron, E80-C, No.7, pp.905-910, 1994.

[9] D. Jiménez, J. J. Sáenz, B. Iñíguez, J. Suñé, L. F. Marsal, and J. Pallarès, IEEE EDL-25, No.8, pp. 571-573, 2004.

[10] Jin He, Mansun Chan, 15th IEEE Int. Conf. on Devices, Circuits and Systems, Nov.3-5, pp. 26-28, 2004.

[11] H. C. Pao and C. T. Sah, *Solid-State Electronics*, vol. 9, pp. 927-937, 1966.
[12] J. R. Brews, Solid-*State Electronics*, vol.21, pp.345-352, 1978.
[13] P.Tsividis. Operation and modeling of the MOS transistor. New York: McGraw-Hill, 1999.

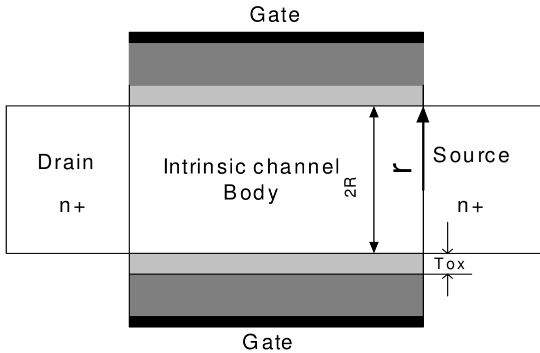

Fig.1 Cross section of CSG MOSFETs.

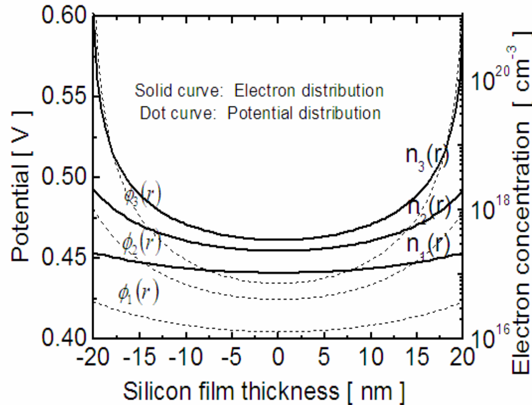

Fig.2 Potential and electron concentration distribution in the active silicon at the different gate voltage in CSG MOSFETs for $V_{GS1} - \Delta\phi_i = 0.420V$ for ϕ_1 and n_1, $V_{GS2} - \Delta\phi_i = 0.450V$ for ϕ_2 and n_2, $V_{GS3} - \Delta\phi_i = 0.520V$ for ϕ_3 and n_3, and $V_{ch} = 0$.

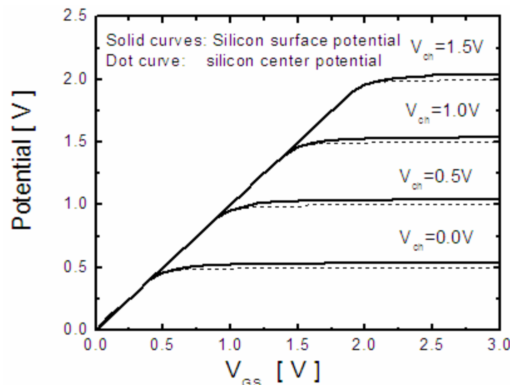

Fig.3 Surface and silicon center electrostatic potentials versus gate voltage for the different quasi Fermi potential in undoped cylindrical surrounding-gate MOSFETs with the midgap gates, for a 40-nm silicon body diameter and oxide layer of 2nm.

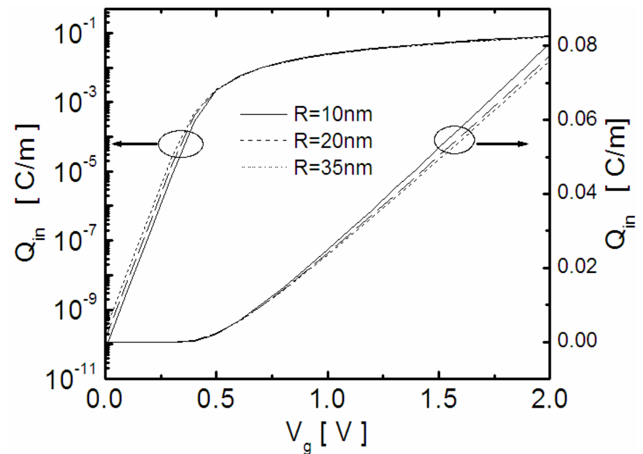

Fig.4 Inversion charge density versus gate voltage for different silicon diameter R in undoped CSG MOSFETs with the midgap gates for $V_{ch} = 0$.

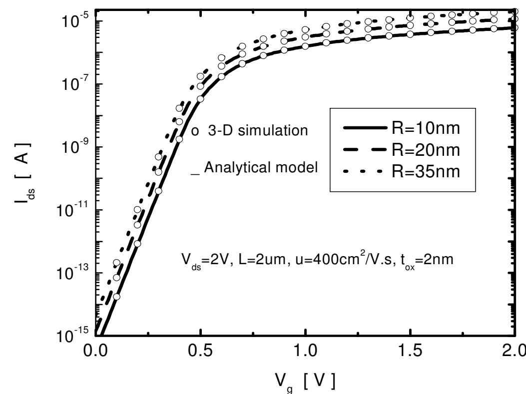

Fig.5 I_{ds}-V_{gs} curves calculated from the analytic model (solid curves) for the different silicon diameter R, compared with the 3-D numerical simulation results (open circles).

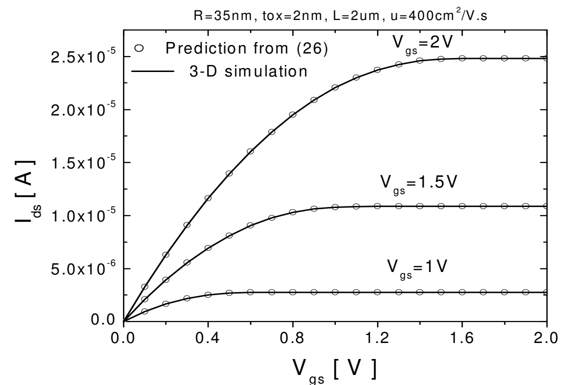

Fig.6 I_{ds}-V_{ds} curve calculated from the analytic model (solid curves), compared with the 3-D numerical simulation results (open circles).