Compact Modeling of Threshold Voltage in Nanoscale Strained-Si/SiGe MOSFETs

Susheel Nawal, Vivek Venkataraman and M. Jagadesh Kumar*

Department of Electrical Engineering, Indian Institute of Technology, New Delhi 110016, India
*Phone: 91-11-26591085, FAX: 91-11-26581264, Email: mamidala@ieee.org

ABSTRACT

Strained-silicon devices have been receiving considerable attention owing to their potential for achieving higher performance due to improved carrier-transport properties, i.e., mobility and high-field velocity [1]. The aim of this paper is to propose, for the first time, a novel analytical model for the threshold voltage of nanoscale strained-Si/SiGe MOSFETs and analyze its dependence on various device parameters. The proposed model correctly predicts the threshold voltage over a wide range of channel lengths and different Ge contents. Our compact model also accurately demonstrates the effect of increasing Ge content on threshold voltage roll-off.

Keywords: strained-Si/SiGe MOSFET, threshold voltage, two-dimensional modeling, short channel effects

1 INTRODUCTION

The conventional method of producing strained Si is pseudomorphic Si epitaxial growth on relaxed SiGe alloys. By increasing the Ge content of the relaxed SiGe alloy, the amount of biaxial strain and therefore the magnitude of the mobility enhancement can be increased. Tremendous improvement in static and dynamic CMOS circuit performance has been demonstrated using strained-Si/SiGe MOSFETs [2]. Developing compact models for the nanoscale SOI MOSFETs will help in designing devices with improved performance [3-7]. Our model provides an efficient tool for design and characterization of high performance strained-Si/SiGe nanoscale MOSFETs including the short channel effects. The effect of varying device parameters can easily be investigated using the analytical model presented in this work. The model is compared with 2-D simulation results using MEDICI [8].

2 EFFECT OF STRAIN

Due to strain, the electron affinity of silicon increases, while the bandgap and effective mass of carriers decreases [9]. The effect of strain on Si band structure can be modeled as [10]:

$$(\Delta E_C)_{s-Si} = 0.57x,\ (\Delta E_g)_{s-Si} = 0.4x,$$
$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{3/2} \approx 0.075x \quad (1)$$

where x is the Ge mole fraction in $Si_{1-x}Ge_x$ substrate, $(\Delta E_C)_{s\text{-}Si}$ is the decrease in electron affinity of silicon due to strain, $(\Delta E_g)_{s\text{-}Si}$ is the decrease in bandgap of silicon due to strain, V_T is the thermal voltage, $N_{V,Si}$ and $N_{V,s\text{-}Si}$ are the density of states in the valence band in normal and strained silicon respectively, $m^*_{h,Si}$ and $m^*_{h,s\text{-}Si}$ are the hole density of states (DOS) effective masses in normal and strained silicon, respectively. The band structure parameters for relaxed $Si_{1-x}Ge_x$ substrate can also be estimated as [11]-[12]:

$$(\Delta E_g)_{SiGe} = 0.467x,\ \ \varepsilon_{SiGe} = 11.8 + 4.2x$$
$$N_{V,SiGe} = \left(0.6x + 1.04(1-x)\right) \times 10^{19}\, cm^{-3} \quad (2)$$

where, $(\Delta E_C)_{SiGe}$ is the decrease in bandgap of $Si_{1-x}Ge_x$ from that of Si, $N_{V,SiGe}$ is the density of states in the valence band in relaxed $Si_{1-x}Ge_x$, and ε_{SiGe} is the permittivity of $Si_{1-x}Ge_x$.

2.1 Flat Band Voltage

Accordingly, the flat-band voltage is modified as [9]:

$$(V_{FB,f})_{s-Si} = (V_{FB,f})_{Si} + \Delta V_{FB,f} \quad (3)$$

where,

$$\Delta V_{FB,f} = \frac{-(\Delta E_C)_{s-Si}}{q} + \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \quad (4)$$

is the change in flat band voltage due to strain, and

$$(V_{FB,f})_{Si} = \phi_M - \phi_{Si} \quad (5)$$

where, ϕ_M is the gate work function, and ϕ_{Si} is the unstrained Si work function.

2.2 Built-in Voltage

The built-in voltages across the source-body and drain-body junctions in the strained-Si thin film is also affected by strain as

$$V_{bi,s-Si} = V_{bi,Si} + (\Delta V_{bi})_{s-Si} \quad (6)$$

where,

$$(\Delta V_{bi})_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} + V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \quad (7)$$

is the change in built-in voltage due to strain, and

$$V_{bi,Si} = \frac{E_{g,Si}}{2q} + \phi_{F,Si} \quad (8)$$

where, $E_{g,Si}$ is the bandgap in unstrained Si, q is the electronic charge, and $\phi_{F,Si}$ is the Fermi potential in unstrained Si.

The built-in voltage across the source-body and drain-body junctions in the relaxed $Si_{1-x}Ge_x$ substrate can be written as

$$V_{bi,SiGe} = V_{bi,Si} + (\Delta V_{bi})_{SiGe} \quad (9)$$

where,

$$(\Delta V_{bi})_{SiGe} = \frac{-(\Delta E_g)_{SiGe}}{q} + V_T \ln\left(\frac{N_{V,Si}}{N_{V,SiGe}}\right) \quad (10)$$

3 THRESHOLD VOLTAGE MODEL

Figure 1 shows the cross-section of a short channel strained-Si/SiGe n-MOSFET. The depletion region under the gate for short channel MOSFETs is not uniform and is affected by the lateral source-body and drain-body depletion widths (x_{dl}) and their respective charges. The exact solution of the 2-D Poisson equation for such a case is too complicated and would most probably require numerical methods. To obtain a compact analytical solution, a box type approximation of the depletion region is computed with a uniform charge density $N_{A,eff}$ and a uniform depth of depletion thickness x_d.

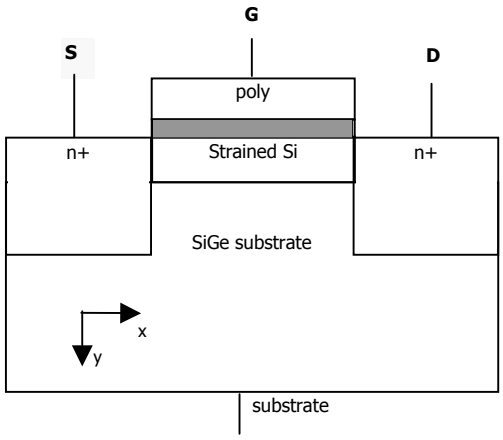

Figure 1: Cross-sectional view of the strained-Si/SiGe MOSFET

3.1 Box Approximation

The gate-S/D charge sharing [13] and source-body/drain-body built-in potential barrier lowering [14] due to overlap of the lateral source-body and drain-body depletion regions become important as the channel length reduces. To incorporate these short channel effects, the effective doping $N_{A,eff}$ is defined taking into account only the effective charge under the influence of the gate [13] as

$$N_{A,eff} = N_A\left[1 - \left(\sqrt{\left(1 + \frac{2x_{dv}}{r_j}\right)} - 1\right)\frac{r_j}{L}\right] \quad (11)$$

where

$$x_{dv} = \sqrt{\frac{2\varepsilon_{SiGe}(\phi_{th} - V_{sub})}{qN_A}}, \quad \phi_{th} = 2\phi_{F,Si} + \Delta\phi_{s-Si}, \text{ and}$$

$$\Delta\phi_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} + V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \quad (12)$$

where x_{dv} is the vertical depletion region depth due to gate bias only, ϕ_{th} is the minimum surface potential required for inversion [9], r_j is the source/drain junction depth, L is the channel or gate length, and V_{sub} is the substrate bias. ϕ_{th} is that value of surface potential at which the inversion electron charge density in the strained-Si device is the same as that in unstrained-Si at threshold [9] (i.e. $\Delta\phi_{s\text{-}Si}=0$ for unstrained-Si).

To complete the box approximation, an average vertical depletion region depth (x_d) is calculated as

$$x_d \cong \frac{2x_{dl}\left(r_j + \frac{\pi}{4}x_{dl}\right) + \left(L - 2x_{dl}\right)x_{dv}}{L} \quad \text{for} \quad L \geq 2x_{dl} \quad (13)$$

and,

$$x_d \cong r_j + \sqrt{x_{dl}^2 - \frac{L^2}{4}} + \frac{\theta}{2}x_{dl} \quad \text{for} \quad L \leq 2x_{dl} \quad (14)$$

where

$$\theta = \sin^{-1}\left(\frac{L}{2x_{dl}}\right) \quad (15)$$

and

$$x_{dl} = \sqrt{\frac{2\varepsilon_{SiGe}V_{bi,SiGe}}{qN_A}} \quad (16)$$

is the lateral source-body and drain-body depletion region width.

3.2 Threshold Voltage Model

The 2-D Poisson equation in the strained silicon thin-film, before the onset of strong inversion can be written as:

$$\frac{d^2\phi_1(x,y)}{dx^2}+\frac{d^2\phi_1(x,y)}{dy^2}=\frac{qN_{A,eff}}{\varepsilon_{Si}} \quad \text{for } 0\le x\le L,\ 0\le y\le t_{s-Si} \tag{17}$$

where ε_{Si} is the dielectric constant of silicon, and $t_{s\text{-}Si}$ is the strained-Si thin film thickness. The potential profile in the vertical direction in the strained-Si film and the depletion region in the SiGe substrate below can be approximated by a parabolic function as:

$$\phi_1(x,y)=\phi_s(x)+c_{11}(x)y+c_{12}(x)y^2 \quad \text{for } 0\le x\le L,\ 0\le y\le t_{s-Si} \tag{18}$$

$$\phi_2(x,y')=V_{sub}+c_{21}(x)y'+c_{22}(x)y'^2 \quad \text{for } 0\le x\le L,\ 0\le y'\le t_{SiGe} \tag{19}$$

where $t_{SiGe}=x_d - t_{s\text{-}Si}$, $\phi_S(x)$ is the surface potential.
The Poisson equation is solved using the appropriate boundary conditions to obtain the surface potential as

$$\phi_s(x)=A\exp(\lambda x)+B\exp(-\lambda x)-\sigma \tag{20}$$

where A, B, λ, σ are constants depending on device parameters. The minimum surface potential is

$$\phi_{s,\min}=2\sqrt{AB}-\sigma \tag{21}$$

The threshold voltage is the gate voltage at which the inversion charge becomes equal to the background doping [2-6]. The inversion condition can be written as [9]:

$$\phi_{s,\min}=2\phi_{F,Si}+\Delta\phi_{s-Si}=\phi_{th} \tag{22}$$

where

$$\Delta\phi_{s-Si}=\frac{-(\Delta E_g)_{s-Si}}{q}+V_T\ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \tag{23}$$

is the effect of strain. Solving the above equation (22), we get the compact model for threshold voltage as:

$$V_{th}=k\left(\frac{-V_{\phi 1}+\sqrt{V_{\phi 1}^{\ 2}-4\xi V_{\phi 2}}}{2\xi}\right) \tag{24}$$

where

$$\xi=2\cosh(\lambda L)-2-\sinh^2(\lambda L),\ V_{\phi 2}=V_{bi1}V_{bi2}-(\phi_{th}-u)^2\sinh^2(\lambda L),$$

$$V_{\phi 1}=V_{bi1}(1-\exp(\lambda L))+(2\phi_{th}-2u)\sinh^2(\lambda L)-V_{bi2}(1-\exp(-\lambda L)),$$

$$V_{bi1}=(V_{bi,s-Si}-u)(1-\exp(-\lambda L))+V_{DS},\ V_{bi2}=(V_{bi,s-Si}-u)(\exp(\lambda L)-1)-V_{DS},$$

$$u=\frac{V_{sub}'}{\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}-\frac{qN_A}{\varepsilon_{Si}\alpha}-\frac{\left(\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}{\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}(V_{FB,f})_{s-Si},$$

$$k=\frac{\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}{\left(\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)} \tag{25}$$

4 RESULTS AND DISCUSSIONS

Figure 2 shows the variation of threshold voltage with gate length for different values of effective Ge mole fraction. It is observed that short channel effects become prevalent below 70-80 nm gate length and is marked by the sharp decrease in V_{th} value. Also, threshold voltage is lower for higher strain for the same gate length.

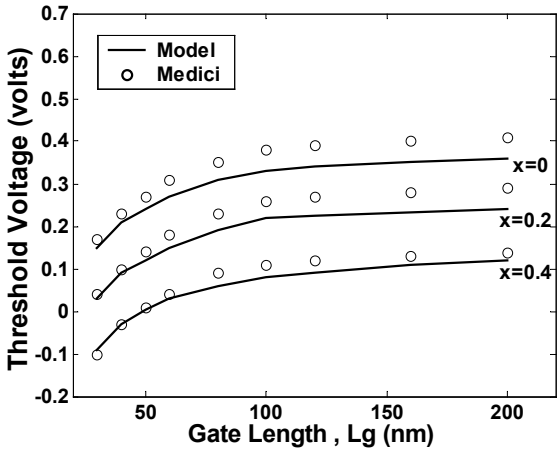

Figure 2: Variation of threshold voltage with Gate Length (tsi=15nm)

This result can be confirmed from Figure 3, which shows the variation of threshold voltage with change in strain for a gate length of 50 nm. The fall in threshold voltage is significant and is almost linear. The threshold voltage decreases with increasing *x* because of decrease in flat-band voltage and earlier onset of inversion. It can also be concluded from Figure 3 that the threshold voltage can be controlled by gate workfunction engineering. Choosing an appropriate gate material can afford lower doping and higher strain levels for the same V_{th}, resulting in enhanced performance. Figure 4 shows that V_{th} also reduces slightly with increase in source/drain junction depth. This may be due to increased gate-S/D charge sharing and overlap of the lateral source-body and drain-body depletion regions. Thus lower junction depths are desirable for better performance.

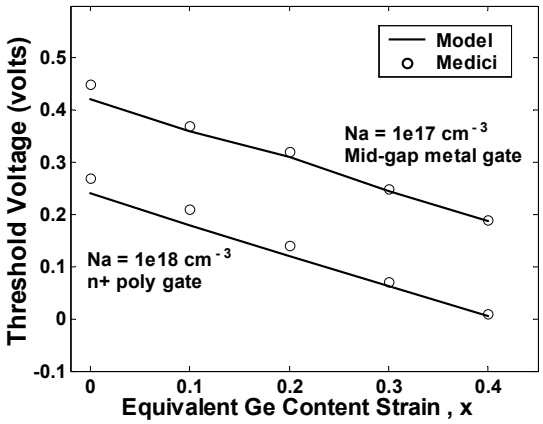

Figure 3: Variation of threshold voltage with strain (L=50nm) for different dopings

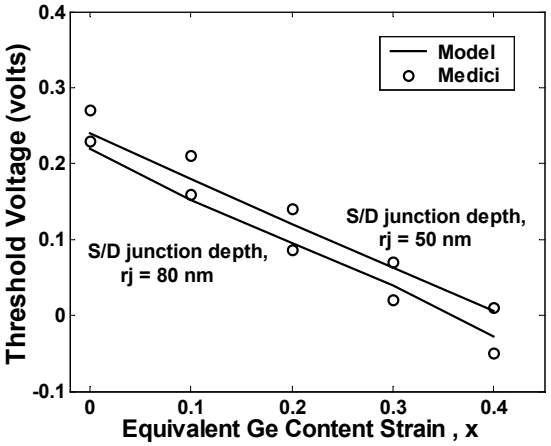

Figure 3: Variation of threshold voltage with strain (L=50nm) for different junction depths

5 CONCLUSIONS

The increase in strain enhances the performance of MOSFETs in terms of transconductance and speed because of increase in carrier mobility [1]. However, as demonstrated by our results, there are undesirable side effects with increasing Ge content such as a roll-off in V_{th}. Our compact model accurately predicts the threshold voltage over a large range of device parameters and can be effectively used to design strained Si/SiGe MOSFETs with the desired performance.

REFERENCES

[1] K. Rim, *et al.*, "Strained Si NMOSFET's for high performance CMOS technology," *Symp. VLSI Tech. Dig.*, pp.59–60, June 2001

[2] S. G. Badcock, A. G. O'Neill, and E. G. Chester, "Device and circuit performance of SiGe/Si MOSFETs," *Solid-State Electronics*, vol. 46, pp. 1925–1932, 2002

[3] M. J. Kumar and A. A. Orouji, "Two-Dimensional Analytical Threshold Voltage Model of Nanoscale Fully Depleted SOI MOSFET with Electrically Induced Source/Drain Extensions," *IEEE Trans. on Electron Devices,* Vol.52, pp.1568-1575, July 2005.

[4] G. V. Reddy and M. J. Kumar, "A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFET –Two-dimensional Analytical Modeling and Simulation," *IEEE Trans. on Nanotechnology,* Vol.4, pp.260 – 268, 2005.

[5] M. J. Kumar and A. Chaudhry, "Two-Dimensional Analytical Modeling of Fully Depleted Dual-Material Gate (DMG) SOI MOSFET and Evidence for Diminished Short-Channel Effects", *IEEE Trans. on Electron Devices,* Vol.51, pp.569-574, April 2004

[6] A. Chaudhry and M. J. Kumar, "Controlling Short-channel Effects in Deep Submicron SOI MOSFETs for Improved Reliability: A Review," *IEEE Trans. on Device and Materials Reliability,* Vol.4, pp.99-109, March 2004.

[7] M. J. Kumar and A. A. Orouji, "Two-dimensional analytical modeling of Nanoscale Electrically Shallow Junction (EJ) Fully depleted SOI MOSFET," Proc.of *The 16th Intl. Conf. on Microelectronics,* Tunis, Tunisia, pp.376-379, 06-08 December 2004

[8] MEDICI 4.0, Technology Modeling Assoc., Palo Alto, CA,1997

[9] W. Zhang and J. G. Fossum, "On the threshold voltage of strained-Si–$Si_{1-x}Ge_x$ MOSFETs," *IEEE Trans. on Electron Devices*, vol. 52, pp.263-268, Feb. 2005

[10] Ji-Song Lim, S. E. Thompson, and J. G. Fossum, "Comparison of Threshold-Voltage Shifts for Uniaxial and Biaxial Tensile-Stressed n-MOSFETs," *IEEE Electron Device Lett.*, Vol.25, pp.731- 733, Nov. 2004.

[11] T. Numata, T. Mizuno, T. Tezuka, J. Koga, and S. Takagi, "Control of Threshold-Voltage and Short-Channel Effects in Ultrathin Strained-SOI CMOS Devices," *IEEE Trans. on Electron Devices*, vol. 52, no. 8, pp. 1780-1786, August 2005

[12] ATLAS Users Manual, Silvaco International, Santa Clara, CA, 2000.

[13] L.D. Yau, "A simple theory to predict the threshold voltage of short-channel IGFETs," *Solid-State Electronics*, vol. 17, pp. 1059-1063, 1974

[14] P. Su, S. Fung, P.Wyatt, H.Wan, A. Niknejad, M. Chan, and C. Hu, "On the body-source built-in potential lowering of SOI MOSFETs," *IEEE Electron Device Letters*, vol. 24, no. 2, pp. 90-92, February 2003.