Fabricating Nanoscale Features Using the 2-Step NERIME TSI Nanolithography Process

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ABSTRACT

The 2-step negative resist image by dry etching (2-step NERIME) focused ion beam (FIB) top surface imaging (TSI) process is a novel nanolithography technique for creating nanometer scale resist features using conventional DNQ/novolak resists. The 2-step NERIME process combines the advantages of FIB lithography and TSI processing, delivering high aspect ratio nanometer-scale resist CDs. Previous work has reported 90nm resist critical dimensions (CDs) on topography using the 2-Step NERIME process. We present 90nm resist CDs over substrate topography, and 80nm etched features masked using the 2-step NERIME process. The 2-step NERIME process uses equipment sets and materials commonly found in microelectronic device fabrication (FIB and O_2 plasma etch tools, DNQ/novolak resists), and we demonstrate its potential as a low-cost and convenient nanolithography option for proof-of-concept nanoscale processing.

Keywords: NERIME, nanolithography, ion beam lithography, semiconductor device fabrication

1 INTRODUCTION

FIB technologies are used in advanced lithographic techniques, and applications include the fabrication of optical masks, nanoimprint stamps and the patterning of small geometry integrated circuits. FIB technologies are also used in the direct lithography patterning of photoresists.

In FIB lithography, ion beams of different elements (Ga^+, Si^+, Al^+, H^+, Be^+, He^+) can be used to introduce energy into a resist film through ion implantation, resulting in exposure of the resist film. Resist exposure is followed by a wet or dry development process [3].

In direct-write electron beam lithography, minimum CD resolution is limited by electron scattering effects and beam spot size. While both FIB lithography and direct-write electron beam lithography share write-speed limitations due to their serial processing (writing one pixel at a time), FIB lithography retains important advantages over electron beam lithography, particularly in the areas of proximity and backscattering effects, and resist sensitivity [2]. However, FIB lithography suffers from limited ion penetration depths in the resist film and the possibility of substrate damage during ion beam exposure. Ga^+ ions implanted at 100keV energies into resist films have typical penetration depths of approximately 50nm. To ensure full exposure of the resist layer during FIB lithography, thin resist layers would be required. Small aspect ratio resist features patterned using thin resist layers can cause problems for subsequent processing steps such as plasma etching. In conventional microelectronic device fabrication, thick resist layers are usually desirable, as they can tolerate poor plasma etch selectivity to the resist during plasma etch processing.

A solution to the problem of limited ion penetration depths in resist is the use of TSI processing. In FIB TSI schemes, the ion beam does not penetrate the full thickness of the resist layer, but only a thin surface layer. Subsequent wet or dry processing develops away the unexposed resist, leaving only the exposed areas [4], [5]. TSI processes can overcome common lithography problems such as substrate topography effects and low depth-of-focus.

The 2-step NERIME process is a single layer FIB TSI scheme optimised for DNQ/novolak based photoresists commonly used in microelectronic device fabrication. The 2-step NERIME process combines the advantages of FIB lithography and TSI processing, and delivers high aspect ratio nanometer-scale resist CDs [6]-[9]. The 2-step NERIME process diagram is shown in Figure 1.

The first step of the 2-step NERIME process flow is the exposure of the DNQ/novolak resist film through the implantation of Ga^+ ions. Ga^+ was chosen because of its low penetration depth in resist. The Ga^+ ions are implanted into the resist layer by the FIB tool to depths of between 10-50nm.

The formation of negative resist images by the 2-step NERIME process is made possible through the mechanism of ion-beam inhibited etching. The ion-implanted resist regions form a Ga_2O_3 mask during the oxygen plasma dry

etch develop step of the process flow. The implanted Ga_2O_3 regions have a much slower etch rate in oxygen plasma when compared with the unexposed resist areas. This difference in etch rates between exposed and unexposed resist areas during the dry develop step results in the formation of a negative resist image on the wafer surface.

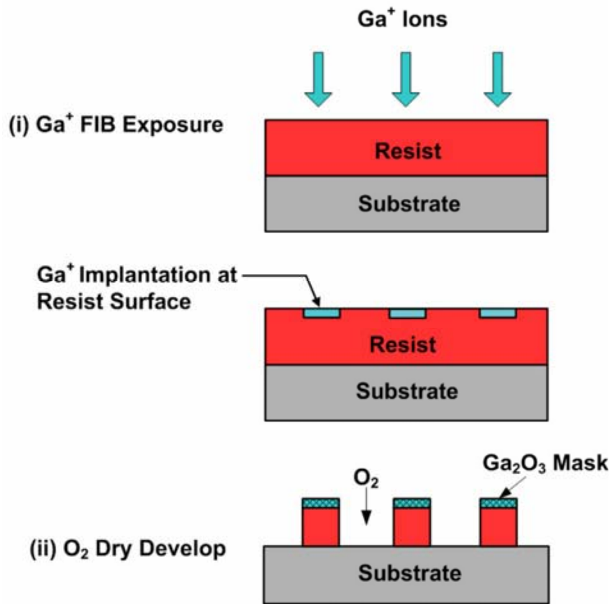

Figure 1: The 2-step NERIME process diagram, showing (i) Ga^+ FIB exposure step and (ii) oxygen plasma develop step.

2 EXPERIMENTAL METHOD

We demonstrated the 2-step NERIME process over topography using substrate wafers that contained LOCOS and etch-defined features. A 250nm thick LOCOS field oxide isolation and 200nm thick polycide layer (Poly1) were defined, followed by the deposition of a 300nm thick CVD oxide dielectric. A 400nm thick Metal layer (Metal1) was then defined and covered by a 400nm thick CVD oxide dielectric layer. The final 600nm metal layer (Metal2) was then deposited, with TiN as the top surface layer of the Metal2 stack.

The wafers used to demonstrate nanoscale etched features masked using the 2-step NERIME process contained a polycide stack (60nm WSi_x on 90nm doped polysilicon) with 250nm LOCOS field oxide isolation and 12.5nm gate oxide areas.

Resist features were patterned on the topography substrate wafers by depositing a layer of the DNQ/novolak resist Shipley SPR660, and processing the resist-coated wafers on the 2-step NERIME process. The resist coat process is designed to coat planar wafers with a resist thickness of 800nm, but resist planarisation over the topography substrates caused resist thickness to vary between 650nm and 1000nm. A series of process experiments were performed on the NERIME Ga^+ exposure and O_2 dry etch develop steps. The FIB beam spot size, beam current and exposure time were optimised during the exposure step. Pressure, power, O_2 flow, magnetic field and etch time were then optimised during the plasma etch dry develop step. An FEI 200 FIB tool was used for the exposure step, and a Balzers MERIE plasma etch chamber used for the dry develop step. Imaging of the resultant resist features was carried out using a Hitachi S4500 SEM and FEI 200 FIB.

The polycide stack was etched in an Applied Materials DPS etch chamber using $CF_4/Cl_2/O_2/HBr$ etch process chemistries. The resist was then removed with an O_2/N_2 plasma strip, and polymer residues were removed from the etched structures using a dilute HF acid dip.

3 RESULTS

Figure 2 shows a SEM micrograph of a 90nm SPR660 resist CD formed on a topography substrate. The resist feature was patterned using the 2-step NERIME process. Figure 3 shows a FIB image, in plan view, of 90nm resist structures patterned using the 2-step NERIME process. The wafer sample received an optimised Ga^+ beam exposure dose of 8.6×10^{-4} C/cm^2, and a dry develop process of 260s in an O_2 plasma etch at 0.032mTorr pressure. The images show well-resolved resist features with smooth sidewalls and no visible line edge roughness, a significant parameter in other TSI process schemes.

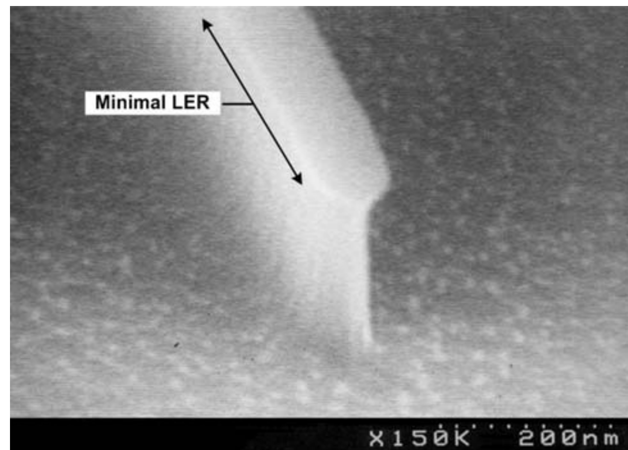

Figure 2: SEM micrograph of a 90nm SPR660 resist feature patterned using the 2-step NERIME process.

Nanolithography schemes must be capable of patterning nanoscale resist features over substrate topography if they are to integrate successfully with fabrication process flows. Resist planarises over topography, and the degree to which this planarisation occurs depends on resist type, resist deposition conditions, and substrate topography.

Resist thickness variations due to underlying topography can cause imaging problems in many lithography processes, making it difficult to control resist CDs and profiles over a range of topography heights. The 2-step NERIME TSI process can overcome poor aspect ratio and unwanted substrate topography effects that affect many other lithographic techniques

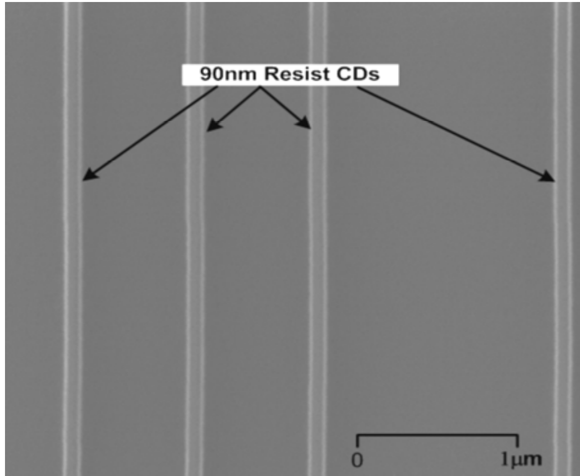

Figure 3: FIB micrograph, planar view, of 90nm SPR660 resist features patterned using the 2-step NERIME process.

Figure 4 shows a FIB cross-section, at 45 degrees sample tilt, through the substrate topography. 90nm resist features are visible on the highest and lowest topography areas of the sample, demonstrating a well-resolved resist pattern with profile and CD control across the substrate topography.

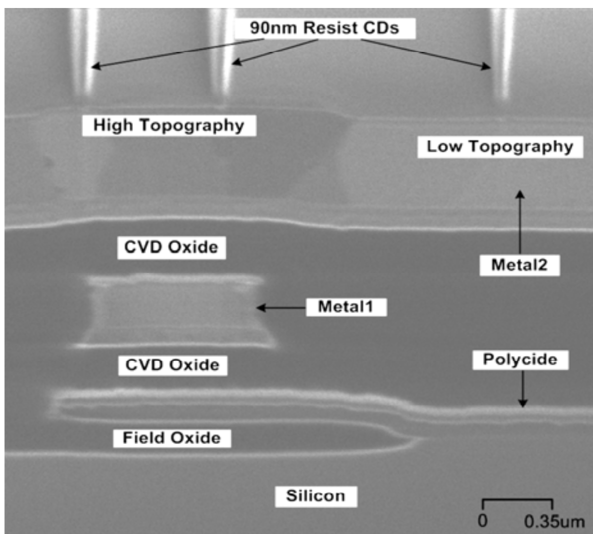

Figure 4: FIB micrograph, at 45 degrees sample tilt, of 90nm SPR660 resist features patterned over a topography substrate using the 2-step NERIME process.

Figures 5 and 6 show SEM micrographs of an 80nm etched polycide feature. The polycide features on this wafer were masked by resist patterned using the 2-step NERIME process. The 80nm etched features exhibit excellent profile control with less than 5nm LER per side, and demonstrate nanoscale etched features formed using the 2-step NERIME process. Such etched features are of potential use in a variety of applications such as nanosensors, NEMs, MEMs, DRAM, and BiCMOS processing.

When compared with conventional microelectronic lithography, nanolithography techniques such as EUV, electron beam and nanoimprint lithography require expensive process equipment and the use of non-standard process materials. The 2-step NERIME process uses equipment sets and materials commonly found in microelectronic device fabrication (FIB and plasma etch tools, DNQ/novolak resists), and provides a low-cost and convenient nanolithography option for proof-of-concept nanoscale processing. The low-cost nanolithography and etch definition module described here provides a convenient sub-100nm processing capability, and this nanoscale processing capability enables nanoscale wafer processing and the exploration of novel nanotechnology applications and devices.

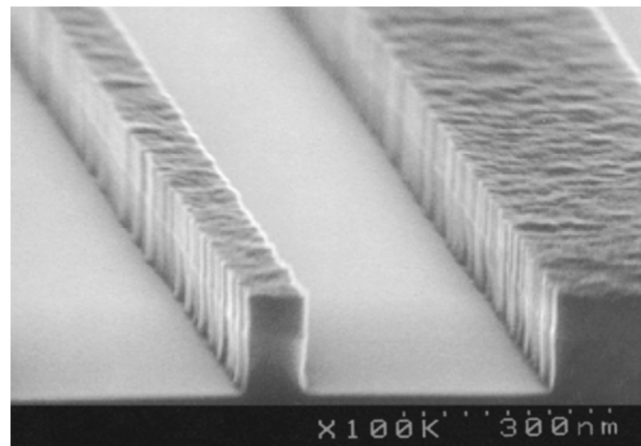

Figure 5: SEM micrograph of a 90nm etched polycide feature. The structure was masked during plasma etch by resist patterned using the 2-step NERIME process.

4 CONCLUSIONS

We have shown experimentally that the 2-step NERIME TSI process can successfully pattern nanoscale resist CDs using DNQ/novolak based photoresists on topography substrates. We report 90nm resist CDs on topography, using 8000A thick layers of SPR600 resist, with no profile degradation or significant CD loss evident across the topography. We also demonstrate 80nm etched polycide CDs masked using the 2-step NERIME process. The nanoscale etched features exhibit excellent profiles.

The results presented here demonstrate the 2-step NERIME process to be an attractive low-cost nanolithography option for applications requiring nanoscale etched features. We expect that the 2-step NERIME process can be further extended to etch sub-40nm features over topography, and suitable applications include nanosensors, NEMs, MEMs, DRAM, and BiCMOS processing.

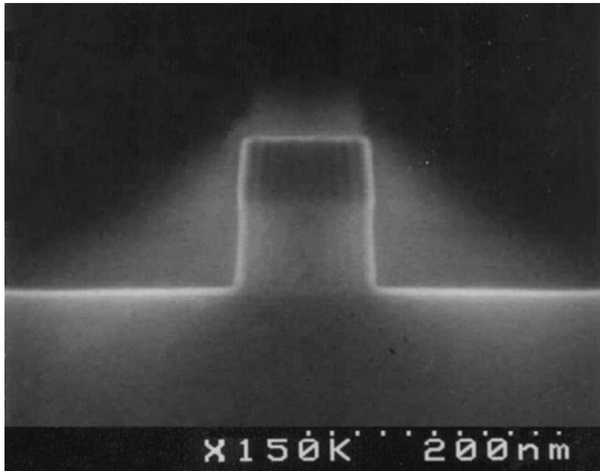

Figure 6: SEM micrograph cross-section of a 90nm polycide etched feature. The Polycide feature was masked during plasma etch by resist patterned using the 2-step NERIME process.

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