# A Circuit-Compatible Model for Ballistic Nanowire Transistors

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## ABSTRACT

Silicon nanowire transistors (SNWTs) have attracted broad attention as a promising device structure for future integrated circuits. Silicon nanowires with a diameter as small as 2nm and having high carrier mobility have been achieved. Consequently, to develop TCAD tools for SNWT design and to model SNWT for circuit-level simulations have become increasingly important. This paper presents a circuit-compatible model for ballistic SNWTs. Both the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the device have been efficiently modeled in terms of device parameters and terminal voltages. Such a model provides an opportunity to effectively perform transistor-level simulations of SNWT circuits.

***Keywords***: ballistic silicon nanowire transistor, circuit-compatible model, Fermi-Dirac integrals.

## 1 SURFACE-POTENTIAL-BASED MODLE

Silicon nanowire transistors (SNWTs) are being extensively explored as a successor to CMOS. Silicon nanowires with a diameter as small as 2nm and having high carrier mobility have been achieved. Such developments shed light on the potential use of silicon nanowire transistors in future integrated circuits. Consequently, to develop TCAD tools for SNWT design and to model SNWT for circuit-level simulations have become increasingly important.

Fig. 1 illustrates the essential aspects of a semi-numerical ballistic SNWT FET model [1-4]. The gate voltage $V_{GS}$ induces charge in the SNWT channel. It also modulates the top of the energy band between the source and the drain. As the source-drain barrier is lowered, current flows between the source and the drain. For ballistic transport, all scattering mechanisms are neglected. Since the current remains constant throughout the channel, it is often computed at the top of the energy barrier (e.g., at the beginning of the channel). An important aspect of ballistic transport is at the top of the barrier, electrons coming from the source fill up the $+k$ states and the electrons coming from the drain fill up the $-k$ states [1-5]. The gate voltage $V_G$ lowers the channel potential and causes accumulation of mobile charge in the channel. On the other hand, it is this mobile charge that causes a voltage drop across the insulator gate and causes the energy band to be lowered. As a result, for a given $V_G$, the potential at the top of the barrier $U_{TOP}$ must be computed self-consistently. In [1], a self-consistent numerical model between the electrostatic potential $U_{TOP}$ and the charge distribution has been developed to assess SNWT performance. The model consists of three capacitors ($C_G$, $C_S$, *and* $C_D$), which represent the effects of the three terminals (the gate, source and drain) on the potential at the top of the barrier. The height of the potential barrier between the source and the drain is obtained as [1-2]

$$U_{TOP} = -q\left[\begin{array}{l}\left(\dfrac{C_G}{C_G+C_D+C_S}\right)V_G \\ +\left(\dfrac{C_D}{C_G+C_D+C_S}\right)V_D \\ +\left(\dfrac{C_S}{C_G+C_D+C_S}\right)V_S\end{array}\right]+\frac{q^2 N_{mobile}}{\left(C_G+C_D+C_S\right)} \quad (1)$$

where the first three terms, the Laplace solution, describes the influence of the three terminals and the last term, the charging energy, describe the effect of the mobile charge at the top of the barrier. For a well-designed SNWT, $C_G >> C_D$ , $C_S$, and the potential is primarily controlled by the gate voltage. For a nanowire FET, the gate oxide capacitance often needs to be numerically computed by solving a 2D Poisson equation at the cross-section of the SNWT. For a coaxial gate geometry, the gate oxide capacitance $C_G$ however can be analytically obtained as

$$C_G = \frac{2\pi\kappa\varepsilon_0}{\ln\left(\dfrac{2t_{ox}+t_{Si}}{t_{Si}}\right)} \quad (2)$$

where $\kappa$ is the oxide dielectric constant, $\varepsilon_0$ is the permittivity of vacuum, $t_{ox}$ is the oxide thickness, and $t_{Si}$ is the diameter of the silicon body. Knowing the bottom of the band at the top of the barrier, the mobile charge $N_{mobile}$ is calculated by filling the $+k$ states according to the source Fermi level (set by the source voltage), and the $-k$ states according to the drain Fermi level (set by the drain voltage). The mobile charge $N_{mobile}$ is obtained as

$$N_{mobile} = n^+ + n^- = \frac{N_{1D}}{2}\varsigma_{-1/2}\left(\eta_F\right)+\frac{N_{1D}}{2}\varsigma_{-1/2}\left(\eta_F - U_D\right). \quad (3)$$

In Eq. (3), $N_{1D} = M\sqrt{\dfrac{2k_B T m_x^*}{\pi\hbar^2}}$ where $m_x^*$ is the electron effective mass in the transport direction, $\hbar$ is the Plank constant, $k_B$ is the Boltzmann constant, T is the temperature and M is the valley degeneracy (for a cylindrical SNWT with <100> orientation, $M = 4$ and $m_x^* = 0.19m_e$). The $\eta_F$ in Eq. (3) is defined as

$$\eta_F = \frac{\mu_S - (\varepsilon(0) + U_{TOP})}{k_B T} \tag{4}$$

where $\mu_S$ is the source Fermi level and $\varepsilon(0)$ represents the lowest subband level at the top of the barrier when $U_{TOP}$ = 0. $U_D$ in Eq. (3) is defined as $U_D = \frac{V_{DS}}{k_B T}$ where $V_{DS} = V_D - V_S$ is the applied drain bias. The function $\varsigma_j(\eta)$ in Eq. (3) is the so-called Fermi-Dirac integral, which is defined as

$$\varsigma_j(\eta) = \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{x^j dx}{1 + \exp(x - \eta)} \tag{5}$$

where $\Gamma$ is the gamma function. The electron current for a SWNT can be analytically expressed as

$$\begin{aligned} I = I^+ - I^- &= M \frac{q k_B T}{\pi \hbar} [\varsigma_0(\eta_F) - \varsigma_0(\eta_F - U_D)] \\ &= M \frac{q k_B T}{\pi \hbar} \ln\left(\frac{1 + e^{\eta_F}}{1 + e^{\eta_F - U_D}}\right) \end{aligned} \tag{6}$$

The self-consistent simulation scheme developed in [1] starts with a guess solution of the electrostatic potential $U_{TOP}$, and the mobile charge $N_{mobile}$ is thus evaluated from Eq. (3). Then the computed $N_{mobile}$ is fed back into Eq. (1) to obtain an updated $U_{TOP}$. This process is iterated until a converged $U_{TOP}$ is achieved. After that, the electron current can be evaluated from Eq. (6).

The mobile charge $N_{mobile}$ is dependent on the potential at the top of the barrier $U_{TOP}$. With the knowledge of the mobile charge and surface potential, a non-linear quantum or semiconductor capacitance can be obtained as

$$C_Q = \frac{\partial(q N_{mobile})}{\partial(U_{TOP}/-q)}. \tag{7}$$

The total quantum capacitance can be split up into $C_{gs}$ and $C_{gd}$ via Eq. (3). Under high drain bias (e.g., ON-state), $N_{mobile} = n^+ = (N_{1D}/2)\zeta_{-1/2}(\eta_F)$, so,

$$\begin{aligned} C_Q &= -q^2 \frac{\partial(N_{mobile})}{\partial(U_{TOP})} = -q^2 \frac{\partial N_{mobile}}{\partial \eta_F} \frac{\partial \eta_F}{\partial U_{TOP}} \\ &= \frac{q^2 N_{1D}}{2 k_B T} \frac{\partial \varsigma_{-1/2}(\eta_F)}{\partial \eta_F} \end{aligned} \tag{8}$$

Eqs. (6-8) are the guiding equations for calculating a SNWT device $I_D$ ($V_{GS}$, $V_{DS}$) characteristic and the quantum gate-input capacitance $C_{gs}$ and $C_{gd}$ for a given $V_{GS}$, and $V_{DS}$. The model is based on the effective-mass approximation and can be used to obtain a quick estimation of the ballistic performance limit for a given SNWT FET structure.

## 2 CIRCUIT-COPMATIBLE MODEL

The model described in the previous section is a surface-potential-based model and the starting point of the model is the top of the barrier potential $U_{TOP}$. Such a model provides accurate numerical computation and is flexible in terms of the device parameters. However, such a model is not easy-to-use form a circuit engineering point of view. The self-consistent loop to solve $U_{TOP}$ and the numerical calculation of the quantum capacitance $C_Q$ make it impossible to incorporate the model into a SPICE-type circuit simulator. For efficient circuit-level simulations, it is desirable to obtain device characteristics in terms of transistor terminal voltages (namely $V_G$, $V_S$, and $V_D$) and to be able to explicitly express the device drain current and quantum capacitance $C_Q$ as closed or quasi-closed analytical forms. In this paper we describe techniques to construct a circuit-compatible SNWT transistor model.

The mobile charge at the beginning of the channel is given by Eqs. (3-5). To obtain the mobile charge, the Fermi-Dirac integral of order -1/2 defined in Eq. (5) needs to be numerically calculated. It is not possible to obtain an analytical closed-form expression for $\varsigma_{-1/2}(\eta)$ and in [5] curve fitting was resorted to model the mobile charge. In this paper, we propose to use an analytically approximated $\varsigma_{-1/2}(\eta)$ (the so-called Aymerich approximation) developed in [6] to obtain a closed-form analytical approximation of the mobile charge. The Aymerich approximation of the Fermi-Dirac integral is given by [6]

$$\varsigma_j(\eta) = \frac{1}{\Gamma(j+1)} \left( \frac{(j+1) 2^{j+1}}{\left[ b + \eta + \left( |\eta - b|^c + a^c \right)^{1/c} \right]^{j+1}} + \frac{\exp(-\eta)}{\Gamma(j+1)} \right)^{-1} \tag{9}$$

where

$$\begin{aligned} a &= \left[ 1 + \frac{15}{4}(j+1) + \frac{1}{40}(j+1)^2 \right]^{1/2} \\ b &= 1.8 + 0.61 j \\ c &= 2 + \left(2 - \sqrt{2}\right) 2^{-j} \end{aligned} \tag{10}$$

Fig. 2 shows the relative error of the approximated $\varsigma_{-1/2}(\eta)$ across the reduced Fermi energy of interest. With the use of the approximated Fermi-Dirac integral of order -1/2, the mobile charge can thus be related to the source Fermi level $\mu_S$ and the drain bias $V_{DS}$ as a closed analytical form with a maximum error of less than 1.2%.

The next step in the model development is to relate the surface electrostatic potential $U_{TOP}$ with the transistor bias voltages of $V_{GS}$ and $V_{DS}$. To model $U_{TOP}$ in an analytical closed-form expression, curve fitting is performed. Similar to [5], we observed that the surface potential $U_{TOP}$ follows the gate voltage $V_{GS}$ when $V_{GS}$ is less than the first equilibrium conduction band minima; once $V_{GS}$ exceeds the first equilibrium conduction band minima, $U_{TOP}$ follows $V_{GS}$ in a relatively linear manner and also weakly depends on $V_{DS}$. The curve fitting takes these observations into account. The $U_{TOP}$ and $V_{GS}$ can be approximately related by the following equation:

$$V_{GS} - U_{TOP} = 0, \qquad \text{for } V_{GS} < \Delta_1 \tag{11a}$$

$$V_{GS} - U_{TOP} = k(V_{GS} - \Delta_1), \quad \text{for } V_{GS} \geq \Delta_1. \tag{11b}$$

The slope of the curve $k$ is a function of the applied drain

bias $V_{DS}$ and the device parameters. The slope $k$ can be approximated as a polynomial of $V_{DS}$ as

$$k = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 + \alpha_3 V_{DS}^3 . \quad (12)$$

For a given SNWT device, firstly the $U_{TOP}$ needs to be iteratively calculated using the surface-potential-based model described in section-1; then curve fitting can be performed to relate $U_{TOP}$ with $V_{GS}$ and $V_{DS}$ using Eqs. (11-12). For a coaxial gate geometry SNWT device with $t_{ox}$ = 1nm, $t_{Si}$ = 1nm and $\kappa$ = 3.9, $\Delta_1$ is obtained as 0.0526V, $\alpha_0$ = -1.15, $\alpha_1$ = 3.59 (Volts$^{-1}$), $\alpha_2$ = -4.24 (Volts$^{-2}$), and $\alpha_3$ = 2.36 (Volts$^{-3}$). In Fig. 3, we plot the curve fitted $U_{TOP}$ *vs.* $V_{GS}$ for different $V_{DS}$ of the example device.

Once the surface potential $U_{TOP}$ as a function of $V_{GS}$ and $V_{DS}$ is obtained, the transistor drain current can then be evaluated assuming a particular $V_{GS}$ and $V_{DS}$ according to Eq. (6) where $U_{TOP}$ is obtained from Eqs. (11-12). In Figs. 4 and 5, we plot the simulated $I_{DS}$ *vs*. $V_{DS}$ for different $V_{GS}$ (the $V_{GS}$ is from 0V to 1.0V with a step size of 0.05V) and the $I_{DS}$ *vs*. $V_{GS}$ for different $V_{DS}$ characteristics of the example SNWT device, respectively. Simulation results of the closed-form analytical model are compared with the surface-potential-based model. In Fig. 6 we plot the mobile charge $N_{mobile}$ *vs*. $V_{DS}$ for different $V_{GS.}$ The mobile charge is evaluated using Eq. (3) where the Fermi-Dirac integral $\varsigma_{-1/2}(\eta)$ is obtained using the Aymerich approximation given by Eqs. (9-10).

With the knowledge of the mobile charge and the surface potential as functions of transistor $V_{GS}$ and $V_{DS}$, the nonlinear quantum gate-input capacitance $C_Q$ can then be computed in terms of device parameters and terminal voltages. The quantum gate-input capacitance is obtained as

$$C_Q = -q^2 \frac{\partial N_{mobile}}{\partial V_{GS}} = -q^2 \frac{\partial N_{mobile}}{\partial \eta_F} \frac{\partial \eta_F}{\partial U_{TOP}} \frac{\partial U_{TOP}}{\partial V_{GS}} . \quad (13)$$

In Eq. (13), to obtain $\partial N_{mobile}/\partial \eta_F$, we first plug the Aymerich approximation of $\varsigma_{-1/2}(\eta)$ into Eq. (3) and then derive the partial derivative of $N_{mobile}$ with respect to $\eta_F$. The $\partial \eta_F/\partial U_{TOP}$ term is obtained from Eq. (4) as $1/k_BT$. The last term $\partial U_{TOP}/\partial V_{GS}$ can be obtained from the curve fitted $U_{TOP}$ *vs*. $V_{GS}$ relationship shown in Eqs. (11-12) as $\frac{\partial U_{TOP}}{\partial V_{GS}} = 1$ for $V_{GS} < \Delta_1$ and $\frac{\partial U_{TOP}}{\partial V_{GS}} = 1 - k$ for $V_{GS} \geq \Delta_1$.

With the above operations, the quantum gate-input capacitance $C_Q$ can thus be expressed as an analytical closed-form in terms of device terminal voltages. The total quantum gate capacitance can be split up into $C_{gs}$ and $C_{gd}$ according to Eq. (3). In Fig. 7, we plot the $C_Q$ *vs.* $V_{GS}$ characteristic for different $V_{DS}$ of the example device. Simulation results of the surface-potential-based model and the analytical circuit model are compared.

Fig. 8 shows the complete circuit equivalent model of a ballistic SNWT device. In the model, two series resistors have been inserted to take care of the electrode resistance (the ohmic resistance at the highly doped source and drain regions and also any resistance due to imperfections at the contact). The equivalent circuit model breaks the iteration loop in the surface-potential-based model for calculating the surface potential $U_{TOP}$ allowing device characteristics such as the drain current $I_{ds}$, the mobile charge $N_{mobile}$ as well as the quantum gate-input capacitance $C_Q$ to be expressed explicitly as closed-form analytical forms in terms of device parameters and terminal voltages. Such a circuit model can be conveniently inserted into a SPICE-type circuit simulator enabling SNWT circuit performance (such as delays and power consumption) to be assessed.

## 3 CONCLUSION

Most of the developed SNWT models are numerical involving self-consistent equations which circuit solvers like SPICE are not able to handle. This paper presents techniques for developing circuit-compatible models for ballistic SNWT transistors. Such techniques break the loop for calculating the surface potential $U_{TOP}$ and enable analytical formulations describing device performance (including the quantum charge, quantum capacitance as well as drain current) to be obtained as closed-form analytical functions in terms of the transistor bias voltages of $V_{GS}$ and $V_{DS}$. From a circuit engineering point of view, such a model is easy-to-use and provides an opportunity to effectively perform transistor-level simulations of SNWT circuits.

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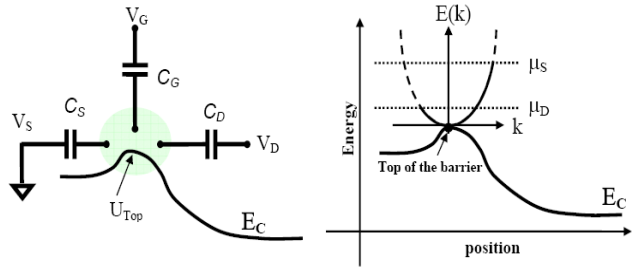


Fig. 1. Illustration of the essential features of the semi-numerical SNWT FET model. The $E_C(x)$ curve represents the lowest electron subband in the device.

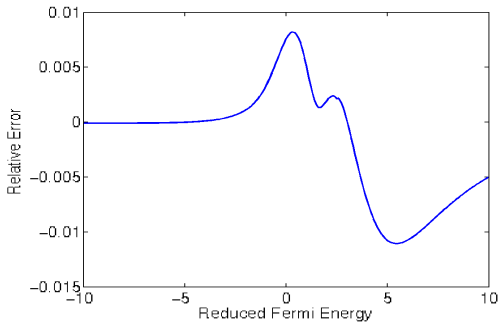


Fig. 2. Relative error of the $\varsigma_{-1/2}(\eta)$ approximation in Eq. (8).

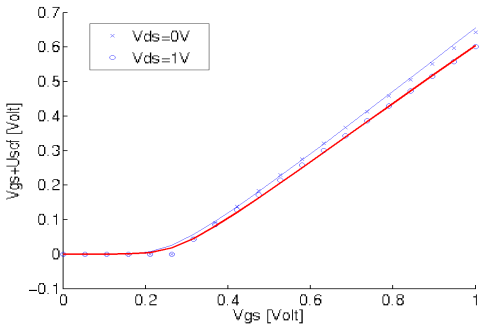


Fig. 3. Curve fitting of the surface potential $U_{TOP}$ *vs.* $V_{GS}$ for different $V_{DS}$ of the simulated SNWT.

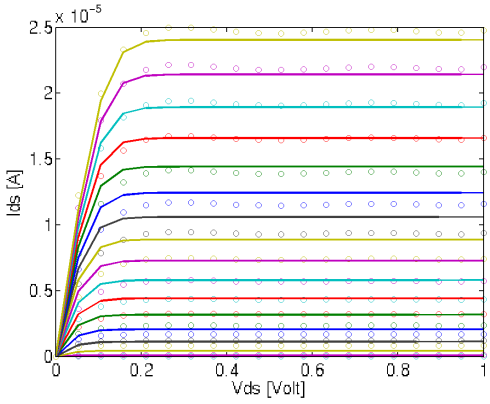


Fig. 4. Plot of $I_{DS}$ *vs.* $V_{DS}$ for different $V_{GS}$ of the example SNWT. Simulation results of the surface-potential-based model and the equivalent circuit model are compared. $V_{GS}$ is from 0V to 1.0V with a step size of 0.05V.

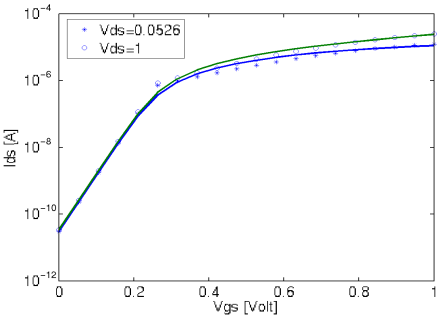


Fig. 5. Plot of $I_{DS}$ *vs.* $V_{GS}$ for different $V_{DS}$ of the simulated SNWT. Simulation results of the surface-potential-based model and the equivalent circuit model are compared.

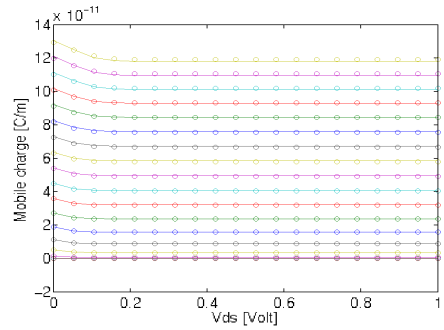


Fig. 6. Plot of the mobile charge $N_{mobile}$ *vs.* $V_{DS}$ for different $V_{GS}$ of the simulated SNWT. Simulation results of the surface-potential-based model and the equivalent circuit model are compared. $V_{GS}$ is from 0V to 1.0V with a step size of 0.05V.

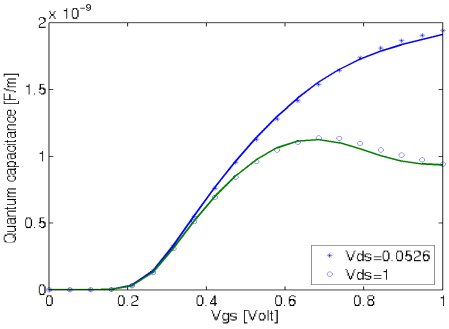


Fig. 7. Plot of the quantum capacitance $C_Q$ *vs.* $V_{GS}$ for different $V_{DS}$ of the simulated SNWT. Simulation results of the surface-potential-based model and the equivalent circuit model are compared.

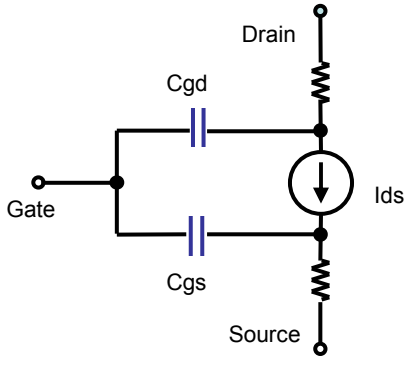


Fig. 8. A schematic diagram of the circuit-compatible model of the SNWT.