Compact Iterative Field Effect Transistor Model

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ABSTRACT

We propose an iterative approach that uses a simple seven-parameter model (based on Unified Charge Control Model – UCCM [1]). This first-order approximation model accounts for the velocity saturation in the device channel, for source and drain series resistance, and for drain barrier lowering. The Universal Current Model (UCM) is used for the output current-voltage characteristics. All other non-ideal effects are accounted for using iterations based on the values of the TFT current obtained using this basic model.

As examples, we consider the effects of the source and drain series resistance on the linearity of the current voltage characteristics at low drain biases, the effect of the current dependent source series resistance, and the effect of the gate-dependent field effect mobility on the current-voltage characteristics.

Keywords: thin film transistors, compact model, gate dependent field effect mobility

1 BASIC MODEL

Compact models for field effect transistors should satisfy two conflicting requirements. On one hand, they should be simple enough and should contain a small number of physics-based parameters to be suitable for parameter extraction. On the other hand, they should accurately account for complicated device phenomena and accurately reproduce device characteristics over many orders of magnitude of the device current and for a wide range of frequencies. This latter requirement is especially important for modeling analog or mixed analog/digital circuits. We propose an iterative approach that uses a simple six-parameter model (based on Unified Charge Control Model – UCCM [1]). This first-order approximation model accounts for the velocity saturation in the device channel, for source and drain series resistance, and for drain barrier lowering. The Universal Current Model (UCM) is used for the output current-voltage characteristics. This model is suitable for parameter extraction and allows for excellent conversion even at very small feature sizes because of the continuity of all derivatives of the current and voltage with respect to extrinsic gate and drain voltages. The model can be augmented by the unified Meyers capacitance model that accounts for capacitance dispersion at high frequencies via Elmore constants. Using this model, we derive the intrinsic drain and gate bias and corresponding drain current and gate-to-source and gate-to-drain capacitance. These values are used for the second iteration model to account for such effects as the channel mobility dependence on the intrinsic gate and drain bias. We start from our MOS saturation model using the following equation from [1]:

\[ I_{sat} = \frac{\beta V_{gt}^2}{1 + \beta R_{gt} V_{gt} + \sqrt{1 + 2\beta R_{gt} V_{gt} + \left(V_{gt}/V_L\right)^2}} \]  

(1)

At small \( V_{ds} \) (in the linear regime)

\[ I = g_{ch} V_{ds} \]  

(2)

Here

\[ g_{ch} = \frac{g_{chi}}{1 + R_{sd} g_{chi} + R_s g_{mi}} \]  

(3)

\[ R_{sd} = R_s + R_d \]

and

\[ g_{chi} = \beta V_{GT} \]

\[ g_{mi} = \beta V_{DS} \]

Therefore, \( g_{mi} \) is much smaller than \( g_{chi} \) at small \( V_{di} << V_{gt} \) and

\[ g_{ch} \approx \frac{\beta V_{gt}}{1 + R_{sd} \beta V_{gt}} \]  

(5)

(provided that \( \beta V_{gt} V_{ds} R_s << V_{gt} \)).

Now we can use the following general expression for the current [1]
\[ I = \frac{g_{ch} V_{ds} (1 + \lambda V_{ds})}{1 + \left( \frac{g_{ch} V_{ds}}{I_{sat}} \right)^{1/m}} \]  

(6)

which accounts for the Drain Induced Barrier Lowering by including the \(1 + \lambda V_{ds}\) term.

This model has only seven parameters, which are the knee parameter \(m, \lambda, \beta = \frac{eW \mu}{dL}, V_T, V_l = \Phi_e L/\mu, R_s,\) and \(R_d\). In the next Section, we use the iteration approach to account for different non-ideal effects important for realistic FET modeling. This makes this model to very convenient for parameter extraction. As an example, we show the I-V characteristics of ZnO TFTs reported in [2] fitted using the above model. Table 1 lists the parameters extracted following the extraction procedure described in [1].

\[ V_{gve} = V_{the} \left(1 + \frac{V_{gve}}{2V_{the}} + \sqrt{\delta^2 + \left(\frac{V_{gve}}{2V_{the}} - 1\right)^2}\right) \]  

(7)

and with

\[ g_{chi} = \beta V_{the} \ln \left(1 + \frac{V_{the}}{2e^{V_{the}/q}}\right) \]  

(8)

respectively. Here \(V_{the} = \eta V_{th} = \eta k_B T / q\) is the effective thermal voltage, \(V_{th}\) is the thermal voltage, \(T\) is temperature, \(q\) is the electronic charge, \(\eta\) is the subthreshold ideality factor, and \(\delta\) is the parameter that determines the transition width between the above threshold and subthreshold regimes (a typical value of \(\delta\) is 3).

In this paper, we use the above model as a basis for the iterative model that allows accounting for different non ideal effects.

## 2 ITERATIVE MODEL EXAMPLES

### 2.1 Constant Series Resistance

The iterative approach can reveal the nonlinearity of the current-voltage characteristics at relatively small values of the drain bias when the series resistance is large and the voltage drop across \(R_s\) is no longer negligible compared to \(V_{ds}\) but still can be accounted for as a correction. In this case, we find

\[ g_{ch} = \beta \left(\frac{V_{gt} - g_{ch} V_{ds}}{R_s}\right) \]

\[ g_{cho} = \frac{1}{\beta R_s + R_{sd}} \left(\frac{V_{gt}}{R_s - g_{ch} V_{ds}}\right) \]  

(9)

This is a quadratic equation with respect to \(g_{cho}\). However, Eq. (9) can be expanded to yield

\[ g_{ch} = g_{cho} \left[1 - \frac{V_{ds}}{V_{gt} g_{cho} R_s} (1 - g_{cho} R_{sd})\right] \]  

(10)

where \(g_{cho} = \frac{\beta V_{gt}}{1 + \beta V_{gt} R_{sd}}\).

Since \(g_{cho} R_{sd} < 1\), Eq. (10) shows that constant source and drain series resistances lead to a sublinear current-voltage characteristics at small \(V_{ds} < V_{gt}\). As an example, Figure 2 shows the \(g_{ch} / g_{cho}\) ratio as a function of \(V_{ds} / V_{gt}\) for \(g_{cho} R_s = 0.2\) and \(g_{cho} R_{sd} = 0.4\). As seen, this effect is quite small. As shown in the next Section, the current-dependent series resistance that is linked to a relatively poor

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**Table 1.** Model parameters used in the calculation of the characteristics shown in Figure 1.

<table>
<thead>
<tr>
<th>(V_T) (V)</th>
<th>(R_s, R_d)</th>
<th>(W) (m)</th>
<th>(\lambda)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-8.5</td>
<td>10</td>
<td>0.001</td>
<td>0.023</td>
</tr>
<tr>
<td>(\mu) (cm²/V-s)</td>
<td>(m)</td>
<td>(L) (m)</td>
<td>(d)</td>
</tr>
<tr>
<td>1.35 (10^{-5})</td>
<td>1.8</td>
<td>8 (10^{-5})</td>
<td>3.75 (10^{-7})</td>
</tr>
</tbody>
</table>

In [1], this model has been generalized to include the Subthreshold regime. This has been achieved by replacing \(V_{gt}\) and \(\beta V_{gt}\) in Eq. (1) with

\[ V_{gve} = V_{the} \left(1 + \frac{V_{gve}}{2V_{the}} + \sqrt{\delta^2 + \left(\frac{V_{gve}}{2V_{the}} - 1\right)^2}\right) \]  

(7)

and with

\[ g_{chi} = \beta V_{the} \ln \left(1 + \frac{V_{the}}{2e^{V_{the}/q}}\right) \]  

(8)

respectively. Here \(V_{the} = \eta V_{th} = \eta k_B T / q\) is the effective thermal voltage, \(V_{th}\) is the thermal voltage, \(T\) is temperature, \(q\) is the electronic charge, \(\eta\) is the subthreshold ideality factor, and \(\delta\) is the parameter that determines the transition width between the above threshold and subthreshold regimes (a typical value of \(\delta\) is 3).
quality Schottky type contacts that often occur in thin film transistors has a much more dramatic effect on the current-voltage characteristics.

2.2 Current Dependent Series Resistance

The iterative model can account for the current dependent source series resistance. First, the current-voltage characteristics are calculated using the basic model described in Section 1 and in [1]. Then the series resistance dependent on current is evaluated using the values of the current predicted by the basic model. We use the following expression for the current dependent series resistance:

\[ R_{si} = R_{so} + \frac{R_{sio}}{I_o + \alpha_{Rs}} \],

(11)

where \( R_{so}, R_{sio}, I_o, \) and \( \alpha_{Rs} \) are current and voltage independent constants. Then we substitute \( R_s \) given by Eq. (11) into the equations of the basic model instead of \( R_s \) and calculate the current-voltage characteristics. Figure 3 shows the effect of the current dependent source series resistance on the current voltage characteristics of long channel a-Si thin film transistors. The model reproduces quite well a superlinear current dependence on the drain bias typical for Schottky type source and drain contacts. Table 2 lists parameters used in the calculation.

Table 2. Model parameters used in the calculation of the characteristics shown in Figure 3.

<table>
<thead>
<tr>
<th>( V_T ) (V)</th>
<th>( R_{so}, R_d )</th>
<th>( W ) (m)</th>
<th>( \lambda )</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>( 2 \times 10^3 )</td>
<td>0.0025</td>
<td>0</td>
</tr>
<tr>
<td>( \mu ) (cm²/V-s)</td>
<td>( m )</td>
<td>( L ) (m)</td>
<td>( d )</td>
</tr>
<tr>
<td>( 1.1 \times 10^{-4} )</td>
<td>2</td>
<td>( 2 \times 10^{-3} )</td>
<td>( 3.5 \times 10^{-4} )</td>
</tr>
</tbody>
</table>

2.3 Gate Dependent Mobility

In thin film transistors, the field effect mobility is a strong function of the intrinsic gate bias. We have adopted the following mobility model accounting for this dependence (related to the movement of the electron Fermi level in the energy gap with the gate bias [3]):

\[ \mu = \frac{1}{\frac{1}{\mu_o} + \frac{1}{\mu_1 N^\kappa}} \],

(12)

where

\[ N = 2 \ln \left(1 + \frac{1}{2} e^{V_g/V_{we}}\right) \],

(13)

is the dimensionless electron concentration in the TFT channel, and \( \mu_o, \mu_1, \) and \( \kappa \) are constants.

Figure 4 shows a typical dependence of the field effect mobility on the gate bias. Parameters used in the calculation are \( \eta = 7, V_T = 4 \) V, \( \mu_o = 1 \) cm²/Vs, \( \mu_1 = 2 \times 10^{-9} \) cm²/Vs, \( T = 300 \) K, and \( \kappa = 3 \).
Figure 5 shows the effect of the gate voltage dependent mobility on the TFT transfer characteristics. Parameters used in the calculation are given in Table 2 and stated above for the gate voltage dependent mobility. The drain bias is 5 V. As seen from Figure 5, this mobility dependence on the gate bias is very pronounced close to the threshold and the effect persists up to fairly large gate biases.

![Graph](image)

Figure 5. Effect of gate voltage dependent mobility on TFT transfer characteristics. Linear (a) and semi log scales (b).

3 CONCLUSIONS

Our iterative approach uses a simple seven-parameter Unified Charge Control Model [1] as the first-order approximation. All other non ideal effects are accounted for using iterations based on the values of the TFT current obtained using this basic model.

The applications of this model for the analysis of the effects of the source and drain series resistance on the linearity of the current voltage characteristics at low drain biases, of the effect of the current dependent source series resistance, and of the effect of the gate-dependent field mobility on the current-voltage characteristics have been demonstrated.

REFERENCES