Three-Dimensional Simulation of Polysilicon Thin Film Transistors with Single-, Double- and Surrounding-Gate Structures

Yiming Li* and Bo-Shian Lee**

* Department of Communication Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsinchu 300, Taiwan, ymli@faculty.nctu.edu.tw
** Display Institute, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsinchu 300, Taiwan

ABSTRACT

In this paper, a three-dimensional simulation of single-, double-, and surrounding-gate polysilicon thin film transistors (TFTs) is presented. Grain trap model is considered in the transport model. Calculations of the driving current, I_D-V_D and I_D-V_G curves are performed. Among three device structures, polysilicon TFTs with surrounding-gate structure reduce the leakage current and improve the short channel effects due to the excellent infinite-gate channel controllability.

Keywords: Polysilicon TFTs, single-gate, double-gate, surrounding-gate, modeling and simulation

1 INTRODUCTION

It is known that polysilicon thin film transistors (TFTs) exhibit large off-state leakage current, and present the pseudo-subthreshold region in transfer characteristics. TFTs with high mobility and low leakage current are necessary in many display product applications; especially in liquid crystal display (LCD) panels. The polysilicon uses a thin polysilicon as the channel layer which consists of many grains. The grains are the monocrystalline lattices, and the interface between the two grains is called grain boundary. With using modern metal-induced lateral crystallization or excimer laser annealed methods, controlling the grain growth allows us to fabricate devices with only a single or small number of discrete grain boundaries existing in the device channel. This results in high performance polyslicon TFTs [1, 2]. The channel length of polysilicon TFTs has been scaled down to submicron region. Unfortunately, the off-state leakage current in these advanced polysilicon TFTs are rather large. A possible mechanism in a conventional device is due to the inversion charge density modulated by the gate [3] resulting in a steep subthreshold slope in their transfer characteristic. Polysilicon TFT exhibits much higher carrier mobility and better driving capability because of higher crystalline [9-12]. With having better driving capability of polysilicon TFT transistors, we can increase the performance of pixel as well as possible. So the plate size will become large and brightly colored.

To improve the performance of TFT, we explore and compare the electrical characteristics of the polysilicon TFTs with different gate structures. By evaluating the transfer and output characteristics, the surrounding-gate polysilicon TFTs demonstrate better driving capability than that of single-gate and double-gate ones. It mainly results from that the surrounding-gate TFTs with a sufficiently large coverage ratio, and can improve short channel effects [13-17]. We computationally analyze electrical properties of thin film transistors using three-dimensional (3D) simulation. The grain size can be connected to device performance by substitution into physically based models for device behavior. So the model must be included trap model. Position-dependent grain trap model is considered in our transport model. Lightly doped drain polysilicon TFTs are proposed to reduce the leakage currents and hot carrier effect. Also, it is shown that some structures are able to improve the current drivability, short channel effects and subthreshold slope of these devices.

This paper is organized as follows. In the section 2, we state the simulation model including device geometry. In the section 3, we show the simulation results and discuss the effect of gate structure on the electrical characteristics. Finally, we draw conclusions and suggestion future work.

2 THE SIMULATION MODEL

We in this work adopt a set of 3D drift-diffusion equations with grain trap model to describe transport phenomena [18-20]. Firstly, we state the Poisson equation with traps.

$$\nabla \cdot \varepsilon \nabla \phi = -q \begin{pmatrix} p - n + N_D - N_A + \sum_{E_t} (N_{Dt} - n_{Dt}) \\ -\sum_{E_t} (N_{At} - p_{At}) + \sum_{E_t} p_t - \sum_{E_t} n_t \end{pmatrix}, \quad (1)$$

$$n_{Dt} = N_{Dt} f_n, \quad (2)$$

$$n_t = N_{Et} f_n, \quad (3)$$

$$p_{At} = N_{At} f_p, \quad (4)$$

and

$$p_t = N_{Ht} f_p, \quad (5)$$

where N_{Dt} is the donor trap concentration, N_{At} is the acceptor trap concentration, N_{Et} is the neutral electron trap concentration, N_{Ht} is the neutral hole trap concentration, n_{Dt} is the electron concentration of the donor trap level, P_{At} is the hole concentration of the acceptor trap level, n_t is the

electron concentration of the neutral electron trap level, and P_t is the hole concentration of the neutral hole trap level.

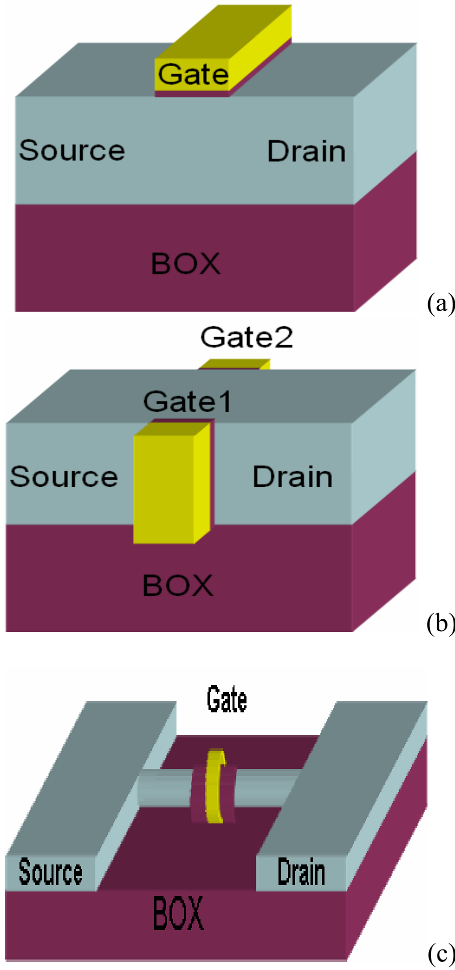


Figure 1: The 3D schematic plots of the simulated polysilicon TFT devices with (a) single-, (b) double-, and (c) surrounding-gate (i.e., gate-all-around), respectively.

The equations (1)-(5) are coupled with the electron and hole continuity equations

$$q\frac{\partial n}{\partial t} - \nabla \cdot \mathbf{J_n} = -qR \quad (2)$$

and

$$q\frac{\partial p}{\partial t} + \nabla \cdot \mathbf{J_p} = -qR, \quad (3)$$

where $\mathbf{J}_n = -qn\mu_n \nabla \phi_n$ and $\mathbf{J}_p = -qp\mu_p \nabla \phi_p$ are the electron and hole current densities. μ_n and μ_p are the electron and hole mobility, and ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials.

The 3D drift-diffusion equations are self-consistently solved in the polysilicon TFT with different gate structures, shown in Fig. 1. Numerical solution is obtained by employing the Gummel's decouping algorithm, the adaptive finite volume method, and the monotone iterative method [18-20]. In the numerical studies, the simulated oxide thickness (T_{ox}) is 0.1 μm, the channel length (L_G) is 3 μm, the channel silicon thickness is equal to 5 μm for all structures, and polysilicon grain size is about 0.3 μm.

As shown in Fig. 2, the expression for trap concentration versus energy (E) is defined as Gaussian distributions. Trapped electron and hole concentrations on one energy level are related to occupation probabilities for electrons (f_n) and holes (f_p).

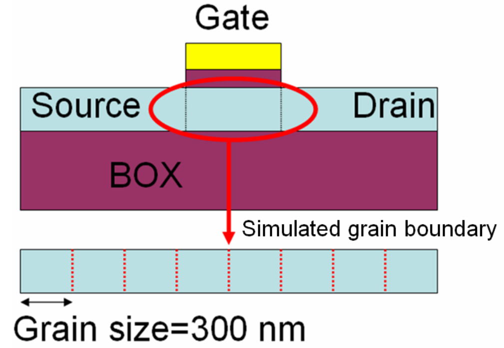
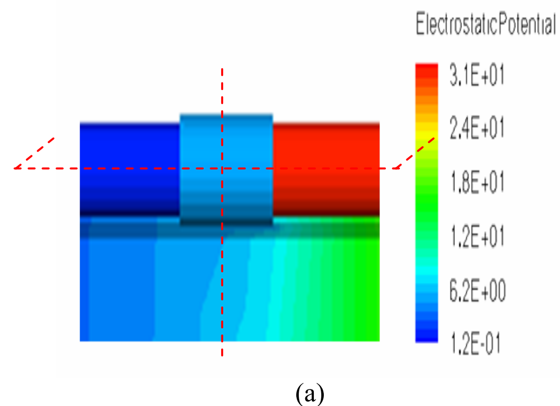


Figure 2: An illustration of the simulated grain boundary in the device channel of three polysilicon TFT structures.

3 RESULTS AND DISCUSSION

We examine the terminal characteristics of single-, double-, and surrounding-gate (SG, DG, and AG) polysilicon TFTs, shown in Fig. 1. We simulate the n-type polysilicon TFTs fabricated on the glass box. In the n-type TFTs, the channel is boron doped and its concentration is equal to 5E+19/cm^3. The source and drain is phosphor doped which concentration is equal to 1E+18/cm^3. Figure 3a shows the 3D plot of the simulated electrostatic potential for the surrounding-gate polysilicon TFT. Different 2D cross-section views along the vertical red line, where the on-state and off-state potentials are shown in Figs. 3b and 3c. The horizontal red line cuts the potential from source to drain in the middle of channel, shown in Fig. 3d.



(a)

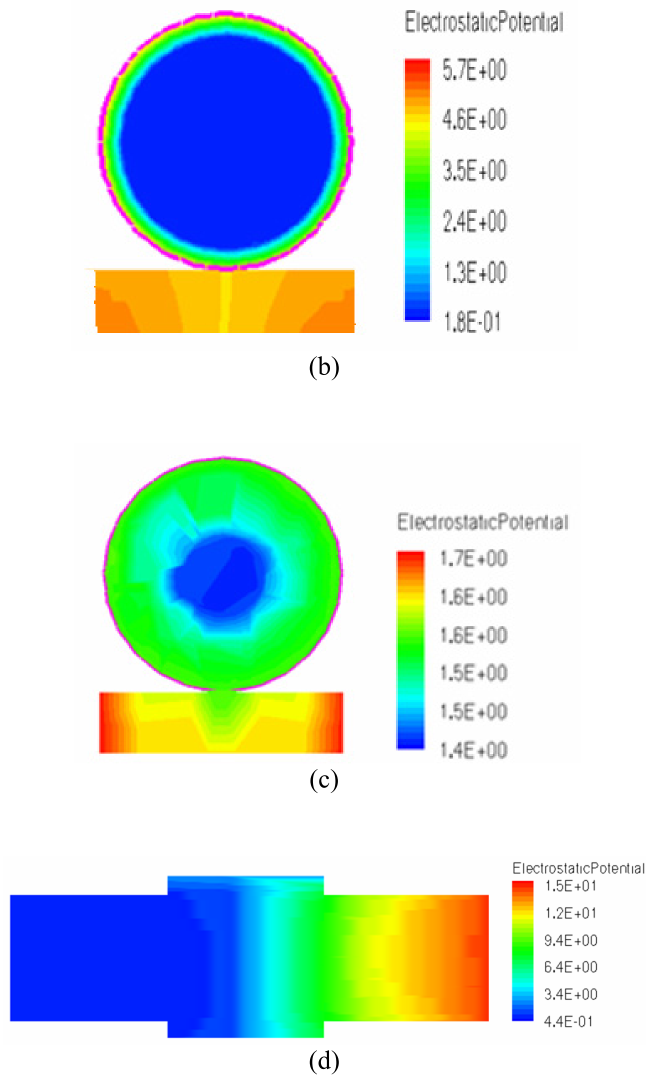


Figure 3. The simulated potential of the surrounding-gate polysilicon TFT, where (a) is a 3D plot with V_D = 30V and V_G = 4.5V. The plot of (b) shows a 2D on-state potential, where the V_D = 30V and V_G = 6.0V. The plot of (c) shows a 2D off-state potential, where the V_D = 30V and V_G = 1.0V. The plot (d) is horizontal cross section view when device is with V_D = 15V and V_G = 6.0V.

As shown in Fig. 3b and 3c, clear identification between the on-state and off-state operations is observed under the gate region. Due to grain boundary effects on the potential, shown in Fig. 3d, it is found that there is a weakly periodical oscillation from source to drain. The significance of periodical potential is strongly dominated by the number of grain boundary and the supplied bias. Our investigation shows that the polysilicon TFT with SG structure possesses largest grain boundary effect due to poor channel controllability, and shows significant oscillation of potential. It may account for the low driving current of polysilicon TFT compared with the single crystal metal-oxide-semiconductor field effect transistor. In contrast with the SG device, the AG TFT device demonstrates excellent channel controllability due to the natural of infinite-gate.

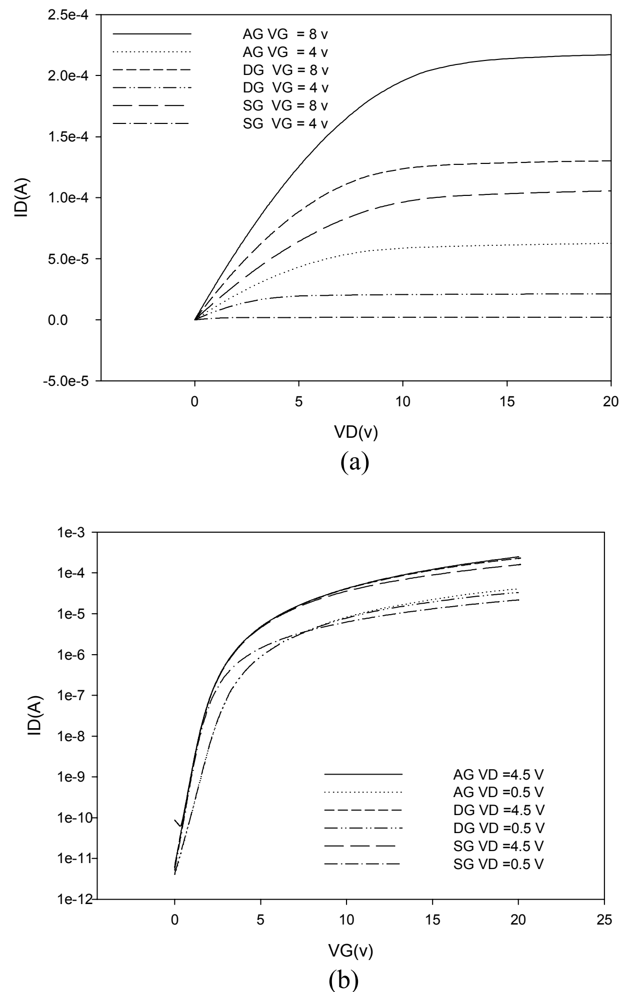


Figure 4. The simulated (a) I_D-V_D and (b) I_D-V_G curves for the explored SG, DG, and AG polysilicon TFTs.

According to this unified 3D simulation, it is found that the surrounding-gate polysilicon TFT, shown in Fig. 4, has its superiority over conventional TFT structures. The drain current of surrounding-gate polysilicon TFT is about 2.5 times higher than that of single-gate one. Both the I_D-V_D and I_D-V_G curves confirm that the promising electrical characteristics of the surrounding-gate TFT. It may benefit device fabrication and display panel circuit design.

4 CONCLUSIONS

We have applied the adaptive finite volume method to solve the 3D DD model with grain boundary traps in polysilicon TFTs. The I_D-V_D and I_D-V_G curves of the single-, double-, and surrounding-gate have been explored.

We have for the first time theoretically proposed the cycle-shaped-surrounding-gate polysilicon TFT, which has shown favorable characteristics among polysilicon TFTs with different gate structures. Among the SG, DG, and AG polysilicon TFT devices, the DG and AG devices with thin channel thickness are promising for obtaining higher driving circuit. We note that the performance of polysilicon TFTs is also limited by the large amount of randomly oriented grain boundaries existing in the channel. The random grain orientation leads to significant device-to-device variation and poor circuit yield.

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