

# Effect of Fin Angle on Electrical Characteristics of Nanoscale Bulk FinFETs

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## ABSTRACT

Bulk fin-shaped field effect transistor (finFET) has been viewed as a promising candidate for sub-45 nm very large-scale integrated (VLSI) circuit design and manufacturing. The structure features excellent device characteristics in comparing with the conventionally planar devices. In fabricating the bulk finFETs, the effect of a nonrectangular fin angle has to be carefully concerned that an ideal fin angle (90 degree) is not easy to be manufactured. Therefore, the short channel effect may be arisen due to the non-ideal manufacturing conditions and influence the device electrical properties. In this paper, the performance impacted by angles and heights of bulk finFETs are for the first time comprehensively investigated to draw the optimal strategy in novel VLSI circuit design.

**Keywords:** Bulk finFET, 3D simulation, optimal angle, geometry effect, electrical characteristics, nanoscale VLSI devices.

## 1 INTRODUCTION

Scaling conventional complementary metal-oxide-semiconductor (CMOS) transistors below 50 nm encounters significant challenges. Traditionally, thin gate dielectrics and heavily doped channel region are always necessary to suppress the short channel effects. Double-gate fin-shaped field effect transistor (finFET) structure can overcome these limitations by placing an additional gate on the back side. Therefore, the gate capacitance is doubled in comparing with the single gate devices; consequently, the device's channel controllability is strongly improved. However, planar double-gate FETs face new challenges: (1) definition of both gates to the same size accurately, (2) self-alignment of source/drain regions to both top and bottom gates, (3) alignment of the two gates to each other, and (4) a low-resistance gate material must be introduced to conquer the problems of time delay. In further improving the channel controllability and suppressing short channel effects, the tri-gate FET's structure has been proposed. The tri-gate finFET structures are fabricated on the silicon-on-insulator (SOI) wafers [1-2]. And the impacts of nonrectangular fin cross section on the electrical characteristics of finFET on SOI wafers has been studied [3]. However, fabricating on the SOI wafers encounters in problems of high cost, difficult in heat dissipation, and hard in electrostatic design. As a result, bulk finFETs are proposed in eliminating the

previously described troubles [4-7]. In fabricating the bulk finFET structures, the fin is not actually rectangular for the lithography and silicon etching processes. The non-ideal processes will result in a wider fin bottom with respect to fin top; thus lead to a slanted edge of the channel fin.

In this work, we will discuss the fin angles and fin heights impact the performance electrical characteristics of a bulk FinFET; and finally demonstrate the optimal strategies. For the studied 20 nm bulk finFET, on-state current, subthreshold swing (SS), drain induced barrier lowering (DIBL), potential, and current density have been calculated with respect to different fin taper angle. The investigation is computationally performed with a three-dimensional (3D) density-gradient simulation [8]. Significant short channel effects are mainly due to slant of the sideward wall of fin. Nonrectangular structure of fin leads to current crowding and deteriorates the performance of a device. The height and angle of fin are two most important parameters in the fabrication processes. The critical angles when the ratios of the fin height and the top fin width are 1.5, 2 and 2.5, are 78.0 degree, 81.3 degree, and 83.6 degree accordingly. Large ratio of the fin height and the top fin width implies a large critical angle. We note that it is hard to find the critical angle when the ratio of the fin height and the top fin width is too large.

This paper is organized as follows. In the section 2, we state the computational model including simulation geometry. In the section 3, we show the simulation results and discuss the effect of fin angle on the interested physical quantities. Finally, we draw conclusions and suggestion future work.

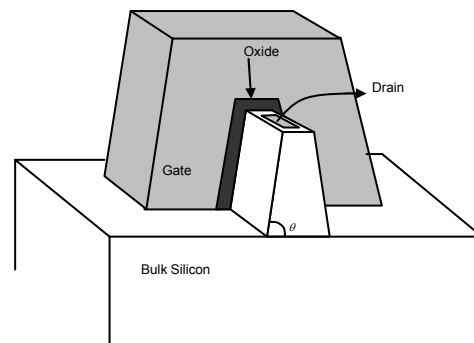


Figure 1: A schematic plot of the bulk finFET for the 3D simulation. The fin angle, the fin height, and the top fin width are considered in our examination.

## 2 THE COMPUTATIONAL MODEL

An illustration of the simulated bulk finFET structure is shown in Fig. 1. Different fin taper angle ( $\theta$ ) is examined in the simulation of aforementioned electrical characteristics for a 20 nm bulk finFET, where the oxide thickness and the top fin width are fixed at 1.2 nm and 20 nm, respectively. Constant doping concentration in silicon substrate is assumed. The concentration of born channel doping is  $6 \times 10^{17} \text{ cm}^{-3}$ . A Gaussian doping distribution on both source and drain is adopted which is with  $1 \times 10^{19} \text{ cm}^{-3}$  of arsenic. The physical parameters of the devices are detailed disclosed in Tab. 1.

Parameters	Value
Gate length (nm)	20
Gate oxide thickness (nm)	1.2
Top fin width (nm)	20
Source / Drain doping concentration ( $\text{cm}^{-3}$ )	$1 \times 10^{19}$
Channel doping concentration ( $\text{cm}^{-3}$ )	$6 \times 10^{17}$

Table 1: Physical parameters for simulation.

To concentrate our attention on the transfer characteristics, the on-state current, the SS, the DIBL, the electrostatic potential, and the current density, a 3D density-gradient simulation is adopted and performed to explore these electrical characteristics of the 20 nm bulk finFET with different fin taper angles. The 3D density-gradient equations are solved with the adaptive finite volume method as well as the monotone iterative method [9-10]. To valid the simulation, mobility with considering phonon scattering, for example, should be adjusted carefully with respect to an optimal setting on the fin angles.

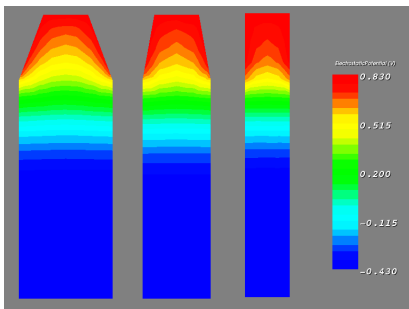


Figure 2: Cutting-plane plots of the simulated electrostatic potential at the central of channel of the 30 nm height bulk finFET. The fin angles are the 90, 80 and 70 degrees from the right figure to the left plot.

## 3 RESULTS AND DISCUSSION

Figures 2-7 show the 2D cutting plane of electrostatic potential and current density at the center location of

channel length with different fin taper angles of 70, 80 and 90 degree, respectively. The device simulation for all cases is biased at 1.0 volt at drain electrode and 1.0 volt at gate electrode. A nonuniform potential and current density along the vertical direction is observed because of distribution of donors and impacts of gate and drain bias on the channel in the direction of fin top to bottom. It is found that the electrostatic potential has its minimum value at the location of fin bottom. It increases rapidly toward the fin top, and the larger potential with larger fin taper angle is perceived at the same distance from fin bottom.

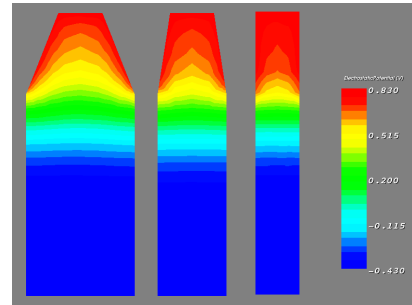


Figure 3: Potential distributions at the central of channel of the 40 nm height bulk finFET. The fin angles are 90, 80 and 70 degrees, respectively

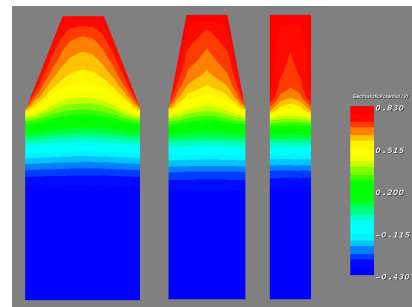


Figure 4: Potential distributions at the central of channel of the 50 nm height bulk finFET. The fin angles are 90, 80 and 70 degrees, respectively.

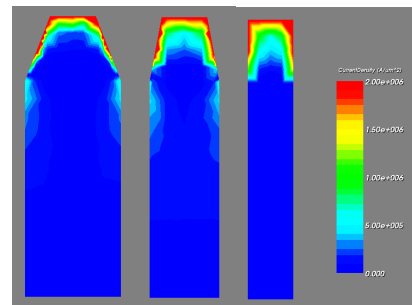


Figure 5: The current density distributions at the central of channel of the 30 nm height bulk finFET. The fin angles are 90, 80 and 70 degrees, respectively.

The current density also attains its minimum value at the location of fin bottom, which reduces as the distance counted from the top fin is enlarged. Moreover, it has been also found that a fin with a larger fin taper angle has a better gate controllability because the current in the channel is more uniformly distributed.

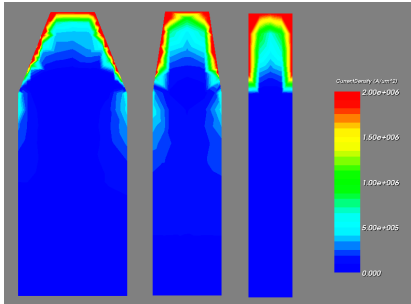


Figure 6: The current density distributions at the central of channel of the 40 nm height bulk finFET. The fin angles are 90, 80 and 70 degrees, respectively.

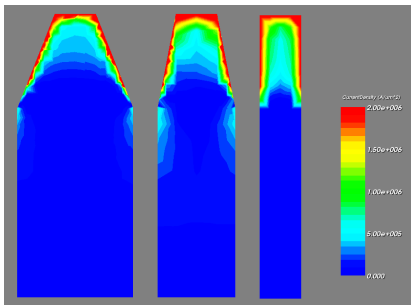


Figure 7: The current density distributions at the central of channel of the 50 nm high bulk finFET. The fin angles are 90, 80 and 70 degrees, respectively.

Figure 8 shows the drain induced barrier height lowering for the bulk finFET with different angles, where the fin height is equal to 30 nm, 40 nm and 50 nm, respectively. We observed that a greater taper angle is wanted for obtaining a robust electrical characteristic. Besides, what is shown in the diagram tells us that lower fin height is desirous in the case of sub-50 nm gate length. The subthreshold swing is exhibited in Fig. 9. It presents a significant result that an increment of fin angle will result in a better SS, especially for the fins with higher fin height, which can improve the short channel effect remarkably. This result is similar with the DIBL one. Side effect becomes more serious with the smaller fin angle. For this reason, we can summarize that the fin height and angle are the critical limiting factor when device scales down. In other word, they are the most important parameters that have to be optimized during the fabrication processes. The structure of a bulk finFET which is closer to a rectangular configuration leads to a better electrical properties. If the larger than one of the ratio between the fin height and the top fin width (the fin height / the top fin width), the

significantly fin taper angle improves the device characteristics. This means in the case of large ratio of the fin height and the top fin width, the controllability of manufacturing the fin taper angle is extremely important and needs to pay much more effort on processing.

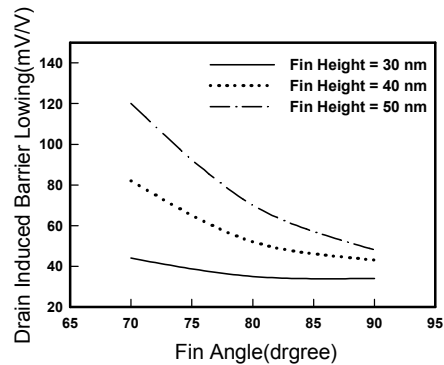


Figure 8: The extracted DIBL effect for the bulk finFET devices with different fin angles. The fin height of device is 30 nm, 40 nm and 50 nm, respectively.

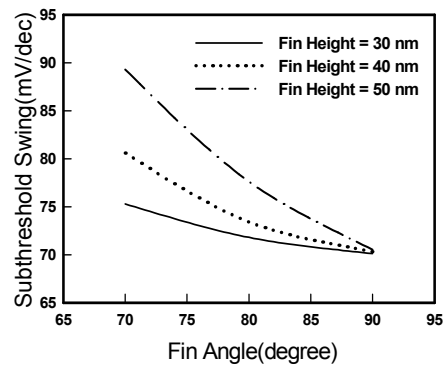


Figure 9: The extracted SS effect for the bulk finFET devices with different fin angles. The fin height of device is 30 nm, 40 nm and 50 nm, respectively.

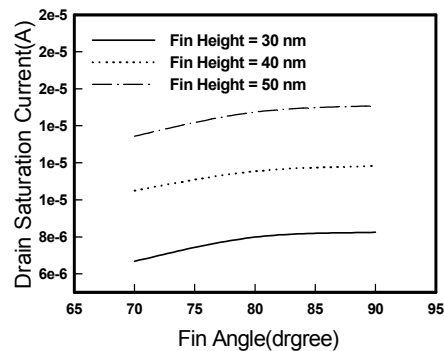


Figure 10: The extracted result of the on-state drain current for the bulk finFET devices with different fin angles. The fin height of device is 30 nm, 40 nm and 50 nm, respectively.

Figure 10 shows the result of considering series resistance. Drain saturation current increases with the rising of the fin angle. Higher fin height results in higher drain saturation current because larger-scale gate contact will control more current and induce more electrons from the donors.

Fin height (nm)	30	40	50
Fin height / Top fin width	1.5	2.0	2.5
Critical angle (degree)	78.0	81.3	83.6

Table 2: The suggested design rules for fabrication of nanoscale bulk finFETs.

## 4 CONCLUSIONS

In this paper, electrical characteristics of nanoscale bulk finFET have been numerically studied by using a 3D density-gradient simulation. For the studied 20 nm bulk-finFET, the on-state current, the SS, the DIBL, the distribution of electrostatic potential, and the distribution of current density have been calculated with respect to different fin taper angle for the first time. The short channel effects are degraded due to slant of the sideward wall of fin. Nonrectangular structure of fin leads to current crowding and deteriorates the performance of a device. Consequently, we can conclude that fin height and the fin angle of device are the two most important parameters in optimizing the fabrication processes. That a nearly rectangular shaped fin is only crucial for the device with a higher fin height. From Tab. 2, we can find the critical angles when the fin height / the top fin width are 1.5, 2 and 2.5, and the critical angles are 78.0 degree, 81.3 degree and 83.6 degree, respectively. Therefore, with the greater of the fin height / the top fin width, the critical angle becomes larger. But if the ratio of the fin height / the top fin width gets too large, it is hard to find the critical angle. Which means an ideal rectangular shape of fin is necessary for good electrical characteristics.

Nanoscale bulk finFETs demonstrate potential application to sub-45 nm CMOS devices, such as SRAM fabrication. Examinations into the effects of the top fin width and wider variation of ratio (e.g., ratio < 1) on electrical characteristics will also benefit the device design. Fluctuation of bulk finFETs should be controlled for high performance design. We believe that a full quantum mechanical modeling and simulation, such as NEGF approach produces more accurate estimations, but the main tendency explored in this work should not be altered.

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