Comparison of Three Region Multiple Gate Nanoscale Structures for Reduced Short Channel Effects and High Device Reliability

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ABSTRACT

New structures which have three gate materials in the gate region and an asymmetric or symmetric stack in the oxide region have been modeled. The 2-D model for surface potential and electric field distribution for the channel region has been derived, using universal depletion width boundary conditions. Comparison of various parameters of previously proposed models with the new structures is carried out. Verification of the new three region model is done by using simulator: ATLAS. A unified model for already existent MOSFETs is provided in addition to the new proposed structure for reduced short channel effects and high device reliability.

***Keywords*:** SCEs, Hot electron effects, Asymmetric oxide stack

1. INTRODUCTION

As the scaling of the bulk CMOS is approaching palpable limit, novel device architectures using shallow junctions are being fabricated with gate lengths realized to be as short as ~14nm. The Electrically variable shallow Junction (EJ) - MOSFET and Straddle-gate transistor [1-2] are viable options to form source/drain (S/D) extension not by doping but by creating an inversion layer. Although these structures have the advantage of reducing short channel effects (SCEs), but large S/D resistance and low-on current prove hindrance in its usage for actual LSI's [1]. One feature common to both of these structures is that both of them have 3 gates (1 main gate and 2 side gates). So we realized the need of modeling the MOSFET structure in three regions in order to understand the device physics of such structures.

In order to reduce the SCEs, hot electron effects and gate transport efficiency the DMG MOSFET structure was proposed [3-4] which modifies the electric field pattern and the surface potential profile along the channel such that the gate transport efficiency increases. The step potential profile, ensures reduction in the SCEs. But, the DMG structure could not rectify the gate leakage current due to the thinning of oxide layer. Thus, it was proposed to use high-K materials in the oxide region, replacing the SiO_2 so that the physical thickness of oxide layer increases, keeping the effective oxide thickness same. But, increasing the physical gate dielectric thickness results in a higher gate-fringing field, which reduces the gate control and aggravates the SCEs [5]. Thus, an ultra thin SiO_2 interlayer between the high-K layer and silicon substrate was introduced which also improves the interface quality and stability. In order to introduce the stacked dielectric architecture symmetrically in DMG the DUMGAS MOSFET [6] and asymmetrically in bulk MOSFET, ASYMGAS MOSFET [7] was proposed. We saw that all of these structures are capable of reduction of SCEs and thus a unified model is required.

So in this paper we have divided our analysis of various MOSFET structures into 3 regions. Division of our analysis into 3 regions enables us to model various already proposed MOSFET structures as will be described later. 2 new structures namely DMGASYMOX (Dual Material Gate Asymmetric Oxide) MOSFET and TRIMGAS (Triple Material Gate Symmetric Oxide) MOSFET have been explored. Our model results are matched with simulated data from 2-D device simulator ATLAS [8] in order to check its validity and not with experimental work since no experimental data are available for DMGASYMOX and TRIMGAS structures.

2. MODEL FORMULATION

Fig 1 and 2 show the schematics of DMG-ASYMOX and TRIMGAS MOSFETs respectively. M1, M2 and M3 are the three gate materials of gate lengths L_{G1} , L_{G2} and L_{G3} for three regions I, II and III respectively. The 2-D Poisson's equation for potential distribution in the channel region is given as

$$\frac{d^2\phi_i(x,y)}{dx^2}+\frac{d^2\phi_i(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{Si}} \qquad 0<y<d \qquad (1)$$

where i=I, II, III corresponds to regions I, II and III of lengths L_{G1} , L_{G2} and L_{G3} respectively, ϕ_i (x,y) is the electrostatic potential in the channel, q is electronic charge, N_A is the substrate doping density , ε_{Si} is the permittivity of silicon and d is sor channel depletion width [4]. The work function is different for metal M1, M2 and M3 so the Poisson's equation is solved separately under the three regions L_{G1}, L_{G2} and L_{G3} assuming a third order polynomial for $\phi_i(x,y)$ and using continuity of potential and electric flux at the interfaces. The 2-D Potential distribution is found to be expressed as

$$\phi_i(x,y)=\phi_{Si}(x)-\left(\frac{V'_{Gi}-\phi_{Si}(x)}{\gamma t_{oxi}}\right)y+\left[\frac{(3\gamma t_{oxi}+2d)}{d^2\gamma t_{oxi}}(V'_{Gi}-\phi_{Si}(x))-\frac{3(V'_{Gi}+V_{sub})}{d^2}\right]y^2-\left[\frac{(2\gamma t_{oxi}+d)}{d^3\gamma t_{oxi}}(V'_{Gi}-\phi_{Si}(x))-\frac{2(V'_{Gi}+V_{sub})}{d^3}\right]y^3 \quad \text{for} \quad 0<y<d \qquad (2)$$

where $\phi_{Si}(x)$ is the surface potential for the region i, $\gamma=\frac{\varepsilon_{Si}}{\varepsilon_{ox}}$, $t_{ioxeff}=t_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_k}t_k$, where t_{ox} and t_k are the oxide thicknesses of dielectrics ε_{ox} and ε_k respectively. $V'_{Gi}=V_{GS}-V_{fbi}$, where V_{GS} is the applied gate-to-source voltage and V_{fbi} is the flat band voltage of region i. On substituting (2) in (1) and using continuity of potential and electric flux at interfaces, we obtain $\phi_i(x,0)$ i.e. $\phi_{Si}(x)$

$$\phi_{Si}(x)=\frac{\eta_{i1}\sinh\left(\frac{\sum_{j=1}^{i}L_{Gj}-x}{\lambda_i}\right)+\eta_{i2}\sinh\left(\frac{x+L_{Gi}-\sum_{j=1}^{i}L_{Gj}}{\lambda_i}\right)}{\sinh\left(\frac{L_{Gi}}{\lambda_i}\right)}+V'_{Gi}\left(1-\frac{6\lambda_i^2}{d^2}\right)-\left(\frac{qN_A}{\varepsilon_{Si}}+\frac{6V_{sub}}{d^2}\right)\lambda_i^2 \qquad (3a)$$

where λ_i is characteristic length and is given as

$$\lambda_i=\sqrt{\frac{\gamma t_{ioxeff}d^2}{2(3\gamma t_{ioxeff}+2d)}} \qquad (3b)$$

Also $E_{Si}(x)=\left.\frac{d\phi_i(x,y)}{dx}\right|_{y=0}=\frac{d\phi_{Si}(x)}{dx}$ (4)

where various coefficients η_{i1} and η_{i2} are calculated for each region using equation (3a) and (4) and using the boundary conditions such that potential and electric field at x=0, L_{G1}, $L_{G1}+L_{G2}$ and $L_{G1}+L_{G2}+L_{G3}$ for y=0 are continuous. $E_{Si}(x)$ is the surface electric field distribution along the channel.

3. VARIOUS MOSFET STRUCTURES THAT CAN BE MODELED USING THE SAME MODEL

3.1. Previously existent MOSFET Structures

a) Single Material Gate (SMG) MOSFET - This is the conventional bulk MOSFET where the gate material is single, so the metal work function for all the three gates will be same (Table 1). Also there is a single oxide layer of SiO_2 and hence no oxide stack (Table2).

b) Straddle Gate Transistor [2] – Here there are two side gates and a central main gate. Hence the two side gates have same metal work function which is lower than the central gate (Table 1) and there is no oxide sack (Table 2).

c) Dual Material Gate (DMG) MOSFET [3,4] – Here in the gate region there are two different metals used and therefore any two consecutive metal work function will be same (Table 1). The oxide is single layer of SiO_2 and hence no oxide stack (Table 2).

d) Single Material Gate Stack (SIMGAS) MOSFET [5]– Here the gate is made of single material in the gate as in case of SMG , but having a uniform oxide stack in the oxide region and hence effective oxide thickness used (Table 2).

e) Dual Material Gate Stack (DUMGAS) MOSFET [6] – Here there are two different metals in the gate region as in DMG, but having a uniform

Number of gate materials	Conditions for metal work functions
Triple Material (3)	$\phi_{M1}>\phi_{M2}>\phi_{M3}$
Straddle Gate (3)	$\phi_{M1}<\phi_{M2}$ and $\phi_{M1}=\phi_{M3}$
Dual Material (2)	$\phi_{M1}>\phi_{M2}$ and $\phi_{M2}=\phi_{M3}$ or $\phi_{M1}>\phi_{M3}$ and $\phi_{M1}=\phi_{M2}$
Single Material (1)	$\phi_{M1}=\phi_{M2}=\phi_{M3}$

Table 1 Conditions required for modeling of gate materials to have different MOSFET structures

Possible MOSFET Structures	Region I	Region II	Region III
Dual Material Asymmetric Gate Stack (DMGASYMOX)	$t_{Ioxeff} = t_{ox} + t_k$ since $\varepsilon_k = \varepsilon_{ox}$	$t_{IIoxeff} = t_{ox} + t_k$ since $\varepsilon_k = \varepsilon_{ox}$	$t_{IIIoxeff} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_k} t_k$
Single Material Asymmetric Gate Stack (ASYMGAS) [7]			
Triple Material Gate Stack (TRIMGAS)	$t_{Ioxeff} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_k} t_k$	$t_{IIoxeff} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_k} t_k$	$t_{IIIoxeff} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_k} t_k$
Dual Material Gate Stack (DUMGAS) [6]			
Single Material Gate Stack (SIMGAS)			
Triple Material Gate (TMG)	$t_{Ioxeff} = t_{ox} + t_k$ since $\varepsilon_k = \varepsilon_{ox}$	$t_{IIoxeff} = t_{ox} + t_k$ since $\varepsilon_k = \varepsilon_{ox}$	$t_{IIIoxeff} = t_{ox} + t_k$ since $\varepsilon_k = \varepsilon_{ox}$
Dual Material Gate (DMG) [4]			
Single Material Gate (SMG)			
Straddle Gate [2]			

Table 2 Various possible MOSFET Structures obtained by modeling of Oxide Region

oxide stack in the oxide region and hence effective oxide thickness used (Table 2).

f) Asymmetric Gate Stack (ASYMGAS) MOSFET [7] – Also abbreviated as SMG-ASYMOX (SMG Asymmetric Oxide) MOSFET. Here the gate is of single material as in SMG and the oxide layer contains an asymmetric oxide stack towards the drain end.

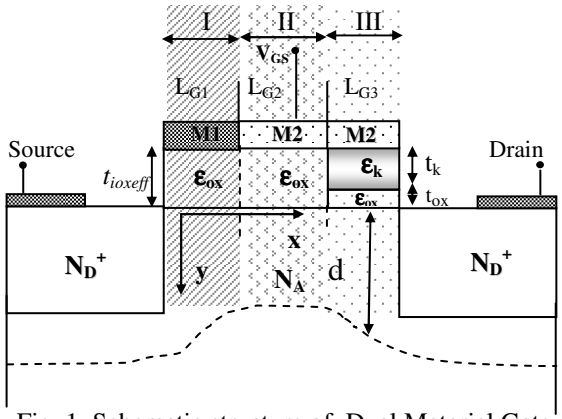

Fig. 1. Schematic structure of Dual Material Gate Asymmetric Oxide (DMGASYMOX) Stack MOSFET.

3.2 Certain possible MOSFET structures using the newly developed three region analysis

i. Triple Material Gate (TMG) MOSFET- Here the three gate regions will have different metal work functions such that it decreases from source to drain (Table 1) and there is no oxide stack in the oxide region (Table 2).

ii. Triple Material Gate Stack (TRIMGAS) MOSFET – Similar to the TMG structure this has three different metals in the gate region. It also has a uniform oxide stack in the oxide region (as seen in Fig.2).

iii. DMG - Asymmetric oxide (DMG-ASYMOX) MOSFET- Here there are two different metal work functions as in DMG but the oxide stack is asymmetric (as seen in Fig.1).

In this paper we have mainly emphasized on two new structures, namely, DMG-ASYMOX and TRIMGAS MOSFETs shown in Fig. 1 and 2 respectively.

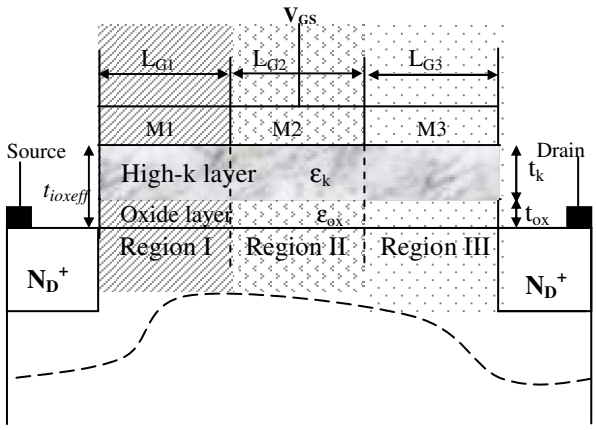

Fig.2 Schematic structure of the Triple Material Gate Stack (TRIMGAS) MOSFET

RESULTS AND DISCUSSION

Reduced short channel effects are monitored using the surface potential profile along the channel of a MOSFET. The positive offset voltage is the difference between the surface potential towards the drain side and towards the source side. Higher the positive offset voltage, higher is the barrier for increase of drain voltage at the source end and hence higher reduction of Drain Induced Barrier Lowering (DIBL). Thus by higher positive offset voltage we mean reduced SCEs. In Fig. 3 we see that a step is introduced at the interface of two different gate materials due to difference in metal work functions. Comparing SMG, DMG and TMG we may see the positive offset voltage of TMG is highest. Also the surface potential shows a slight increase at the interface of asymmetric oxide stack so positive offset of DMGASYMOX is higher than DMG. On introduction of symmetric oxide stack (TRIMGAS) the positive offset

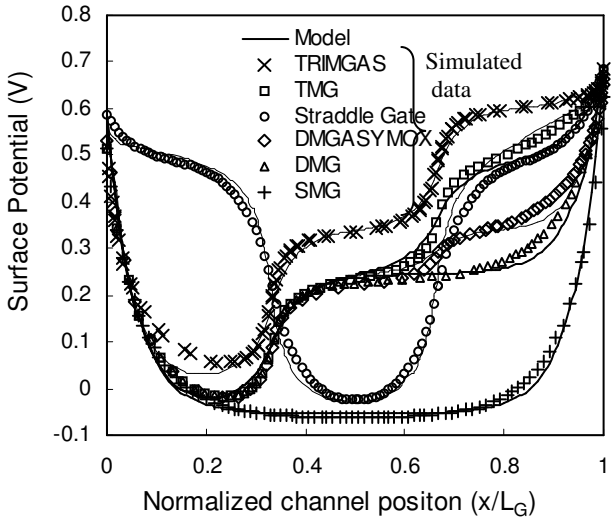

Fig 3 . Surface potential variation with normalized channel position for different structures

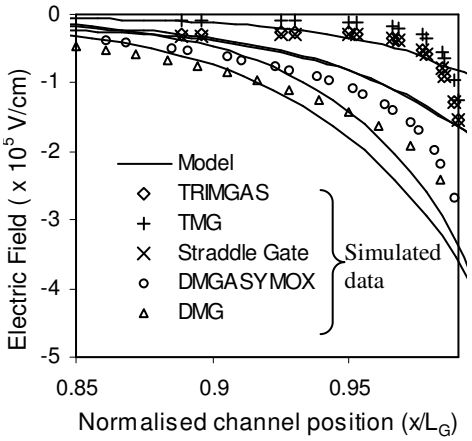

Fig 4 . Electric Field variation with normalized channel position for different structures at the drain end

voltage increases as compared to TMG , which is also higher than that of DMGASYMOX therefore indicative of maximum reduction of DIBL in TRIMGAS as compared to rest of the structures.

The electric field profile along the channel at the drain end gives us a measure to determine the hot electron effect. Lower the electric field at the drain end lower will be the hot electron effect. In Fig. 4 it is seen that the electric field at the drain end for DMGASYMOX is lower when compared to DMG. But TRIMGAS has least electric field as compared to rest of the structures. So maximum reduction of hot electron effect is achieved for TRIMGAS MOSFET structure.

CONCLUSION

In conclusion we may say that our TRIMGAS MOSFET with 3 different materials in the gate region and an oxide stack has maximum reduction of SCEs and hot electron effects. Thus TRIMGAS MOSFET proposed is a more reliable device for nanoscale regime. Our model results match well with the simulated data. Since, the three region model developed can be used for modeling a range of MOSFET structures as described in Section 3 and summarized in Table 1 and 2, by oxide and gate engineering, hence our model may be considered as a unified model.

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